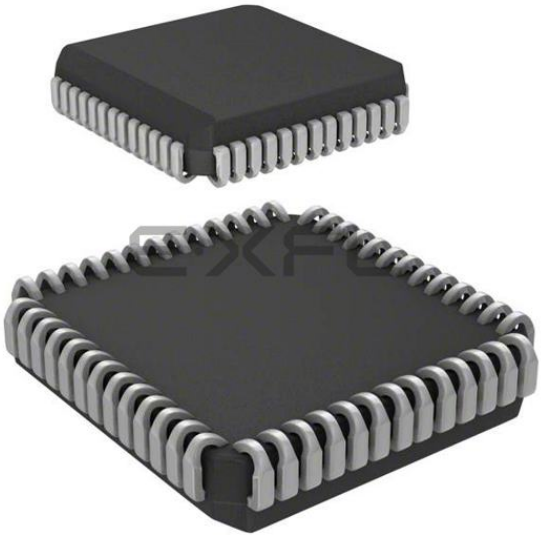

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11e1vfne3

Chapter 4
Central Processor Unit (CPU)

4.1 Introduction

Features of the M68HC11 Family include:

- Central processor unit (CPU) architecture
- Data types
- Addressing modes
- Instruction set
- Special operations such as subroutine calls and interrupts

The CPU is designed to treat all peripheral, input/output (I/O), and memory locations identically as addresses in the 64-Kbyte memory map. This is referred to as memory-mapped I/O. There are no special instructions for I/O that are separate from those used for memory. This architecture also allows accessing an operand from an external memory location with no execution time penalty.

4.2 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as if they were memory locations. The seven registers, discussed in the following paragraphs, are shown in Figure 4-1.

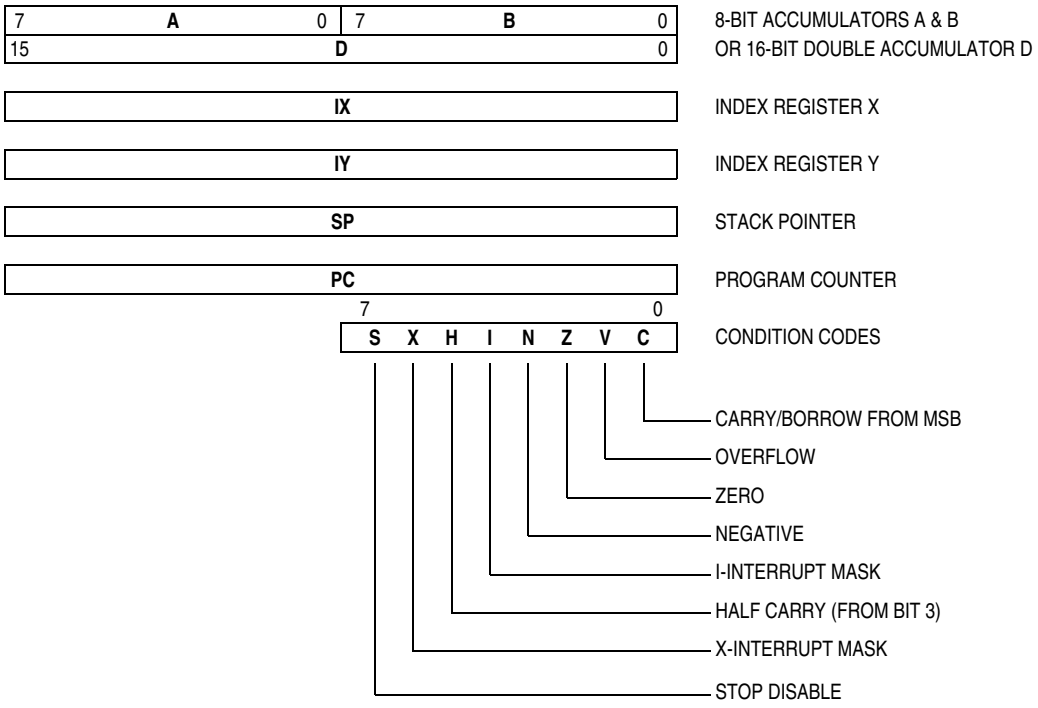


Figure 4-1. Programming Model

5.2.5 System Configuration Options Register

Address:	$1039							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME		CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal mode or at any time in special modes

= Unimplemented

Figure 5-2. System Configuration Options Register (OPTION)

ADPU — Analog-to-Digital Converter Power-Up Bit

Refer to Chapter 3 Analog-to-Digital (A/D) Converter.

CSEL — Clock Select Bit

Refer to Chapter 3 Analog-to-Digital (A/D) Converter.

IRQE — Configure $\overline{\text{IRQ}}$ for Edge-Sensitive-Only Operation Bit

0 = $\overline{\text{IRQ}}$ is configured for level-sensitive operation.
1 = $\overline{\text{IRQ}}$ is configured for edge-sensitive-only operation.

DLY — Enable Oscillator Startup Delay Bit

Refer to Chapter 2 Operating Modes and On-Chip Memory and Chapter 3 Analog-to-Digital (A/D) Converter.

CME — Clock Monitor Enable Bit

This control bit can be read or written at any time and controls whether or not the internal clock monitor circuit triggers a reset sequence when the system clock is slow or absent. When it is clear, the clock monitor circuit is disabled, and when it is set, the clock monitor circuit is enabled. Reset clears the CME bit.

0 = Clock monitor circuit disabled
1 = Slow or stopped clocks cause reset

Bit 2 — Unimplemented

Always reads 0

CR[1:0] — COP Timer Rate Select Bit

The internal E clock is first divided by 2^{15} before it enters the COP watchdog system. These control bits determine a scaling factor for the watchdog timer. See Table 5-1 for specific timeout settings.

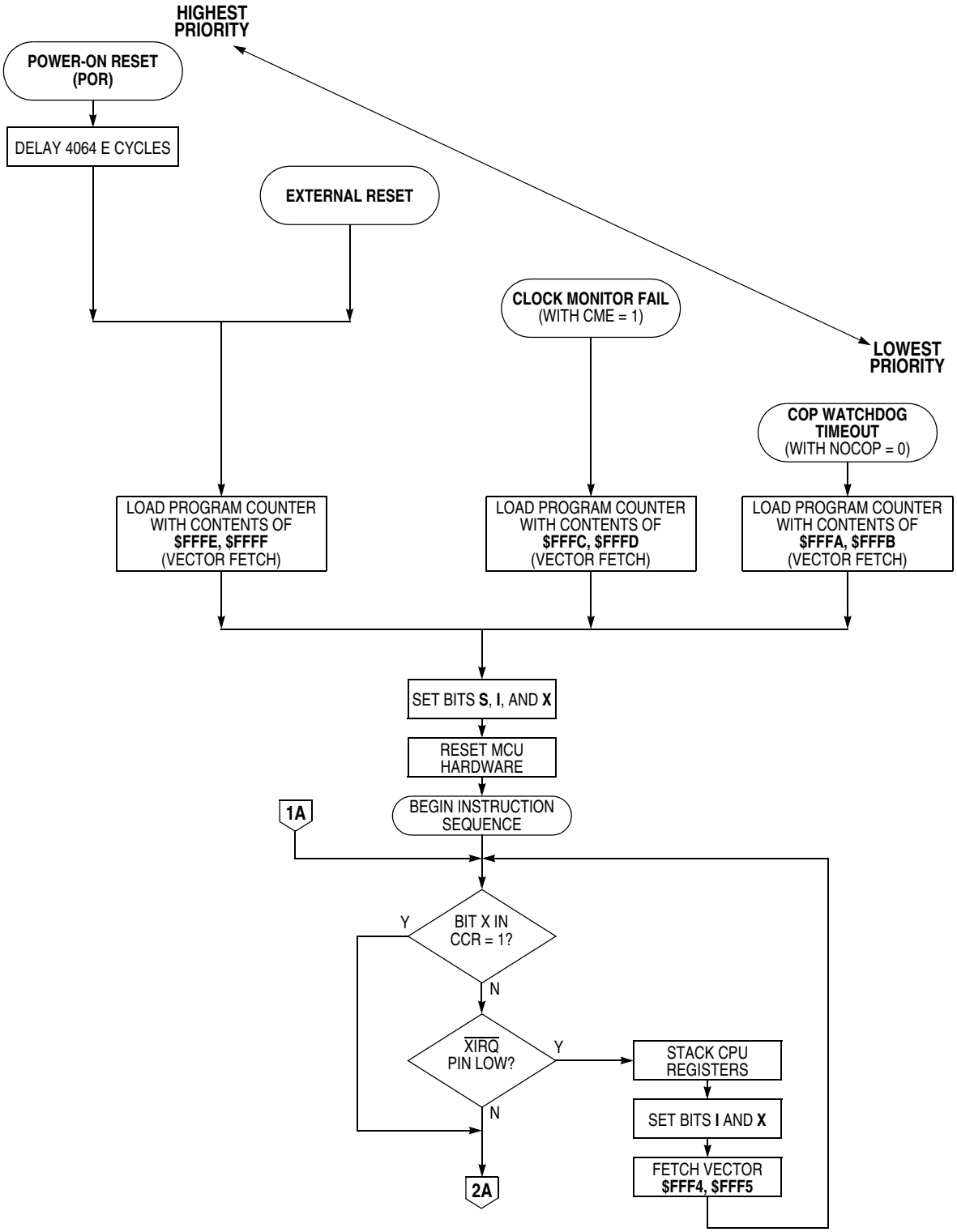


Figure 5-5. Processing Flow Out of Reset (Sheet 1 of 2)

masked), the MCU starts up, beginning with the stacking sequence leading to normal service of the $\overline{\text{XIRQ}}$ request. If X is set to 1 ($\overline{\text{XIRQ}}$ masked or inhibited), then processing continues with the instruction that immediately follows the STOP instruction, and no $\overline{\text{XIRQ}}$ interrupt service is requested or pending.

Because the oscillator is stopped in stop mode, a restart delay may be imposed to allow oscillator stabilization upon leaving stop. If the internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, the DLY control bit can be used to bypass this startup delay. The DLY control bit is set by reset and can be optionally cleared during initialization. If the DLY equal to 0 option is used to avoid startup delay on recovery from stop, then reset should not be used as the means of recovering from stop, as this causes DLY to be set again by reset, imposing the restart delay. This same delay also applies to power-on reset, regardless of the state of the DLY control bit, but does not apply to a reset while the clocks are running.

PORTCL is used in the handshake clearing mechanism. When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register. Reads of this register return the last value latched into PORTCL and clear STAF flag (following a read of PIOC with STAF set).

Address: $1007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

Figure 6-6. Port C Data Direction Register (DDRC)

DDRC[7:0] — Port C Data Direction Bits

In the 3-state variation of output handshake mode, clear the corresponding DDRC bits. Refer to Figure 10-13. 3-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer).

0 = Input
1 = Output

6.5 Port D

In all modes, port D bits [5:0] can be used either for general-purpose I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. During reset, port D pins PD[5:0] are configured as high-impedance inputs (DDRD bits cleared).

Address: $1008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	PD5	PD4	PD3	PD2	PD1	PD0
Reset:	—	—	I	I	I	I	I	I
Alternate Function:	—	—	PD5 $\overline{SS}$	PD4 SCK	PD3 MOSI	PD2 MISO	PD1 Tx	PD0 RxD

I = Indeterminate after reset

Figure 6-7. Port D Data Register (PORTD)

Address: $1009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:			DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6-8. Port D Data Direction Register (DDRD)

Bits [7:6] — Unimplemented

Always read 0

DDRD[5:0] — Port D Data Direction Bits

When DDRD bit 5 is 1 and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

7.5.2 Address-Mark Wakeup

The serial characters in this type of wakeup consist of seven (eight if M = 1) information bits and an MSB, which indicates an address character (when set to 1, or mark). The first character of each message is an addressing character (MSB = 1). All receivers in the system evaluate this character to determine if the remainder of the message is directed toward this particular receiver. As soon as a receiver determines that a message is not intended for it, the receiver activates the RWU function by using a software write to set the RWU bit. Because setting RWU inhibits receiver-related flags, there is no further software overhead for the rest of this message.

When the next message begins, its first character has its MSB set, which automatically clears the RWU bit and enables normal character reception. The first character whose MSB is set is also the first character to be received after wakeup because RWU gets cleared before the stop bit for that frame is serially received. This type of wakeup allows messages to include gaps of idle time, unlike the idle-line method, but there is a loss of efficiency because of the extra bit time for each character (address bit) required for all characters.

7.6 SCI Error Detection

Three error conditions – SCDR overrun, received bit noise, and framing – can occur during generation of SCI system interrupts. Three bits (OR, NF, and FE) in the serial communications status register (SCSR) indicate if one of these error conditions exists.

The overrun error (OR) bit is set when the next byte is ready to be transferred from the receive shift register to the SCDR and the SCDR is already full (RDRF bit is set). When an overrun error occurs, the data that caused the overrun is lost and the data that was already in SCDR is not disturbed. The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCDR.

The noise flag (NF) bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with FE equal to 1) followed by a read of the SCDR.

When no stop bit is detected in the received data character, the framing error (FE) bit is set. FE is set at the same time as the RDRF. If the byte received causes both framing and overrun errors, the processor only recognizes the overrun error. The framing error flag inhibits further transfer of data into the SCDR until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to 1) followed by a read of the SCDR.

7.7 SCI Registers

Five addressable registers are associated with the SCI:

- Four control and status registers:
  - Serial communications control register 1 (SCCR1)
  - Serial communications control register 2 (SCCR2)
  - Baud rate register (BAUD)
  - Serial communications status register (SCSR)
- One data register:
  - Serial communications data register (SCDR)

The SCI registers are the same for all M68HC11 E-series devices with one exception. The SCI system for MC68HC(7)11E20 contains an extra bit in the BAUD register that provides a greater selection of baud prescaler rates. Refer to 7.7.5 Baud Rate Register, Figure 7-8, and Figure 7-9.

7.7.1 Serial Communications Data Register

SCDR is a parallel register that performs two functions:

- The receive data register when it is read
- The transmit data register when it is written

Reads access the receive data buffer and writes access the transmit data buffer. Receive and transmit are double buffered.

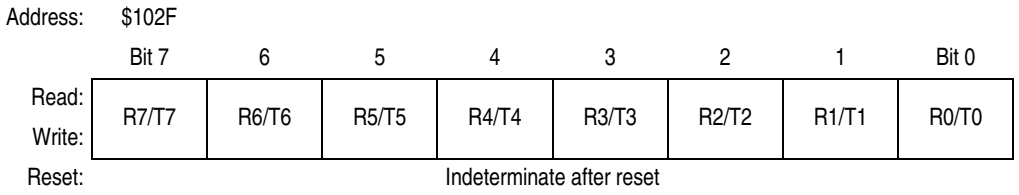


Figure 7-3. Serial Communications Data Register (SCDR)

7.7.2 Serial Communications Control Register 1

The SCCR1 register provides the control bits that determine word length and select the method used for the wakeup feature.

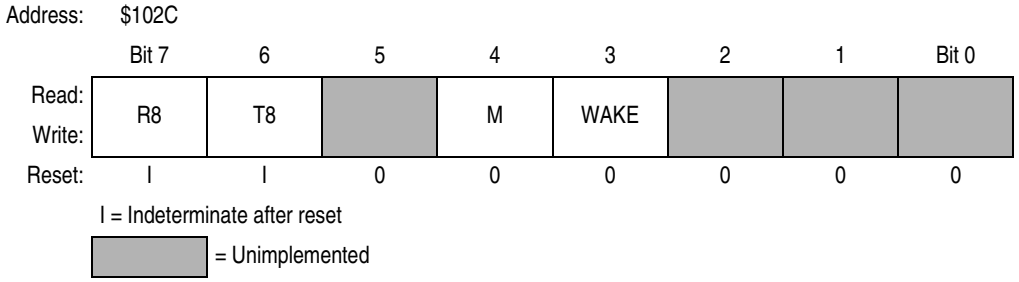


Figure 7-4. Serial Communications Control Register 1 (SCCR1)

R8 — Receive Data Bit 8

If M bit is set, R8 stores the ninth bit in the receive data character.

T8 — Transmit Data Bit 8

If M bit is set, T8 stores the ninth bit in the transmit data character.

Bit 5 — Unimplemented

Always reads 0

M — Mode Bit (select character format)

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle Bit

0 = Wakeup by IDLE line recognition
1 = Wakeup by address mark (most significant data bit set)

Bits [2:0] — Unimplemented

Always read 0

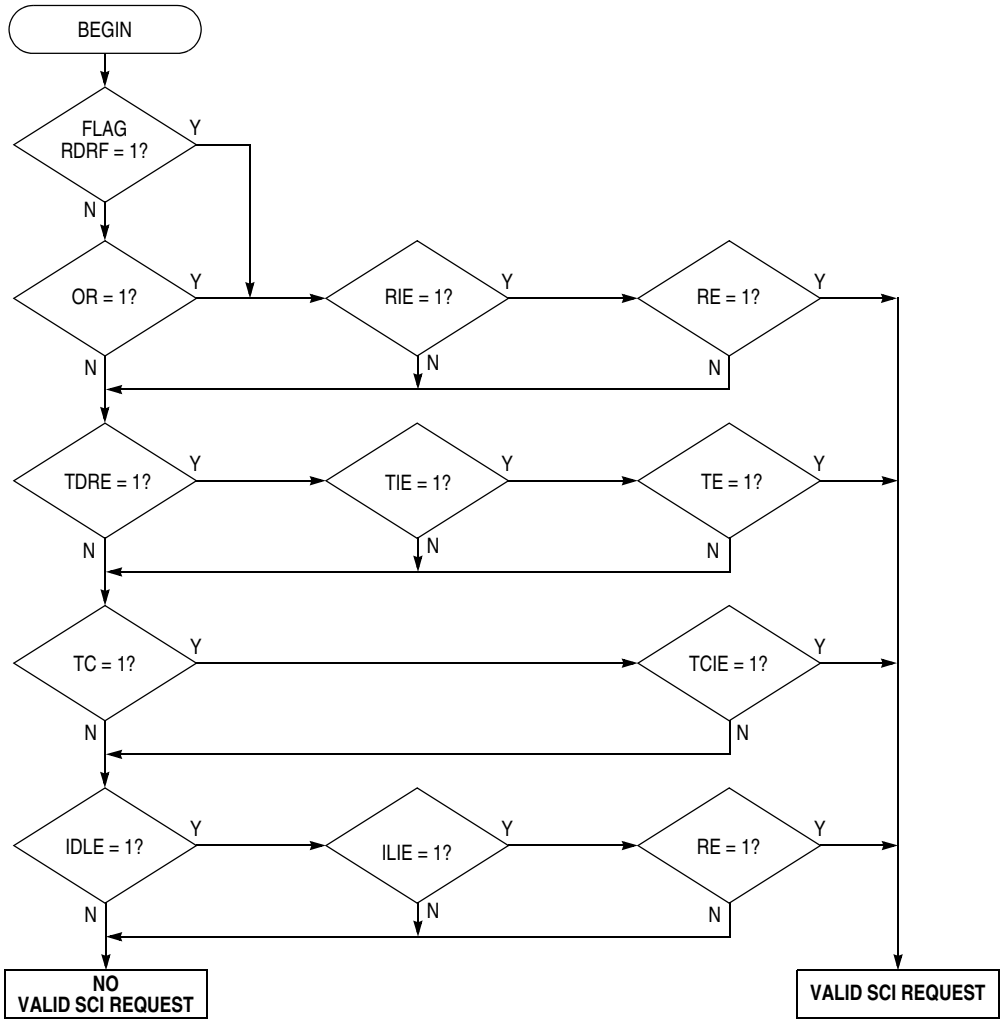


Figure 7-10. Interrupt Source Resolution Within SCI

FOC[1:5] — Force Output Comparison Bit

When the FOC bit associated with an output compare circuit is set, the output compare circuit immediately performs the action it is programmed to do when an output match occurs.

0 = Not affected
1 = Output x action occurs

Bits [2:0] — Unimplemented

Always read 0

9.4.3 Output Compare Mask Register

Use OC1M with OC1 to specify the bits of port A that are affected by a successful OC1 compare. The bits of the OC1M register correspond to PA[7:3].

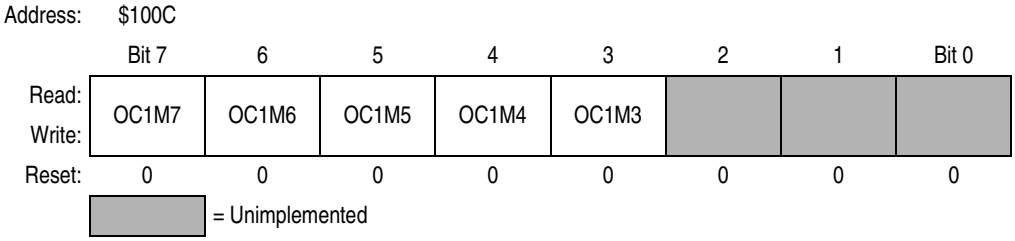


Figure 9-13. Output Compare 1 Mask Register (OC1M)

OC1M[7:3] — Output Compare Masks

0 = OC1 disabled
1 = OC1 enabled to control the corresponding pin of port A

Bits [2:0] — Unimplemented

Always read 0

9.4.4 Output Compare Data Register

Use this register with OC1 to specify the data that is to be stored on the affected pin of port A after a successful OC1 compare. When a successful OC1 compare occurs, a data bit in OC1D is stored in the corresponding bit of port A for each bit that is set in OC1M.

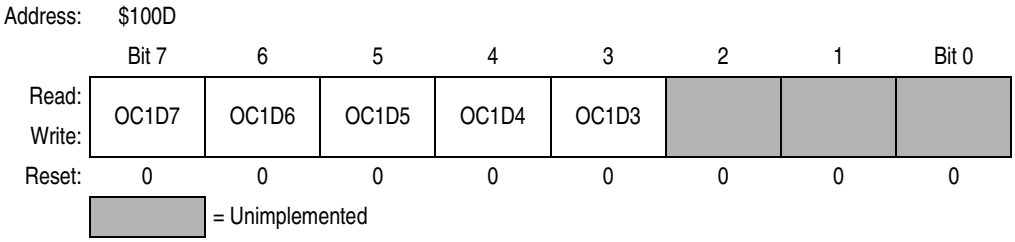


Figure 9-14. Output Compare 1 Data Register (OC1D)

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Unimplemented

Always read 0

9.4.5 Timer Counter Register

The 16-bit read-only TCNT register contains the prescaled value of the 16-bit timer. A full counter read addresses the most significant byte (MSB) first. A read of this address causes the least significant byte (LSB) to be latched into a buffer for the next CPU cycle so that a double-byte read returns the full 16-bit state of the counter at the time of the MSB read cycle.

Register name: Timer Counter Register (High) Address: $100E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Register name: Timer Counter Register (Low) Address: $100F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-15. Timer Counter Register (TCNT)

9.4.6 Timer Control Register 1

The bits of this register specify the action taken as a result of a successful OCx compare.

Address: $1020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
Reset:	0	0	0	0	0	0	0	0

Figure 9-16. Timer Control Register 1 (TCTL1)

OM[2:5] — Output Mode Bits

OL[2:5] — Output Level Bits

These control bit pairs are encoded to specify the action taken after a successful OCx compare. OC5 functions only if the I4/O5 bit in the PACTL register is clear. Refer to Table 9-3 for the coding.

Table 9-3. Timer Output Compare Actions

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

10.5 DC Electrical Characteristics

Characteristics[1]	Symbol	Min	Max	Unit
Output voltage[2] I_{Load} = ±±10.0 µA All outputs except XTAL All outputs except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OL}, V_{OH}	— V_{DD} –0.1	0.1 —	V
Output high voltage[2] I_{Load} = –0.8 mA, V_{DD} = 4.5 V All outputs except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OH}	V_{DD} –0.8	—	V
Output low voltage I_{Load} = 1.6 mA All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage All inputs except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	0.7 × V_{DD} 0.8 × V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage, all inputs	V_{IL}	V_{SS} –0.3	0.2 × V_{DD}	V
I/O ports, 3-state leakage V_{In} = V_{IH} or V_{IL} PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	I_{OZ}	—	±10	µA
Input leakage current[3] V_{In} = V_{DD} or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)	I_{In}	— —	±1 ±10	µA
RAM standby voltage, power down	V_{SB}	4.0	V_{DD}	V
RAM standby current, power down	I_{SB}	—	10	µA
Input capacitance PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{In}	— —	8 12	pF
Output load capacitance All outputs except PD[4:1] PD[4:1]	C_L	— —	90 100	pF

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted
2. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
3. Refer to 10.13 Analog-to-Digital Converter Characteristics and 10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics for leakage current for port E.

10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics

Characteristic[1]	Parameter[2]	Min	Absolute	Max	Unit
Resolution	Number of bits resolved by A/D converter	—	8	—	Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics	—	—	±1	LSB
Zero error	Difference between the output of an ideal and an actual for 0 input voltage	—	—	±1	LSB
Full scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	—	—	±1	LSB
Total unadjusted error	Maximum sum of non-linearity, zero error, and full-scale error	—	—	±1/2	LSB
Quantization error	Uncertainty because of converter resolution	—	—	±1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	—	—	±2	LSB
Conversion range	Analog input voltage range	V_{RL}	—	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	—	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} –0.1	—	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}	3.0	—	—	V
Conversion time	Total time to perform a single analog-to-digital conversion: E clock Internal RC oscillator	 — —	 32 —	 — t_{CYC}+ 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	—	Guaranteed	—	—
Zero input reading	Conversion result when $V_{In} = V_{RL}$	00	—	—	Hex
Full scale reading	Conversion result when $V_{In} = V_{RH}$	—	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling time: E clock Internal RC oscillator	 — —	 12 —	 — 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance during sample PE[7:0]	—	20 typical	—	pF
Input leakage	Input leakage on A/D pins PE[7:0] V_{RL}, V_{RH}	 — —	 — —	 400 1.0	 nA µA

1. V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤ E ≤ 2.0 MHz, unless otherwise noted
2. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.

10.17 Serial Peripheral Interface Timing Characteristics

Num	Characteristic[1]	Symbol	E9		E20		Unit
			Min	Max	Min	Max	
	Frequency of operation E clock	f_o	dc	3.0	dc	3.0	MHz
	E-clock period	t_{CYC}	333	—	333	—	ns
	Operating frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	f_o/32 dc	f_o/2 f_o	f_o/128 dc	f_o/2 f_o	MHz
1	Cycle time Master Slave	$t_{CYC(m)}$ $t_{CYC(s)}$	2 1	32 —	2 1	128 —	t_{CYC}
2	Enable lead time[2] Slave	$t_{lead(s)}$	1	—	1	—	t_{CYC}
3	Enable lag time[2] Slave	$t_{lag(s)}$	1	—	1	—	t_{CYC}
4	Clock (SCK) high time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	t_{CYC}–25 1/2 t_{CYC}–25	16 t_{CYC} —	t_{CYC}–25 1/2 t_{CYC}–25	64 t_{CYC} —	ns
5	Clock (SCK) low time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	t_{CYC}–25 1/2 t_{CYC}–25	16 t_{CYC} —	t_{CYC}–25 1/2 t_{CYC}–25	64 t_{CYC} —	ns
6	Data setup time (inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	30 30	— —	30 30	— —	ns
7	Data hold time (inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	30 30	— —	30 30	— —	ns
8	Slave access time CPHA = 0 CPHA = 1	t_a	0 0	40 40	0 0	40 40	ns
9	Disable time (hold time to high-impedance state) Slave	t_{dis}	—	50	—	50	ns
10	Data valid[3] (after enable edge)	t_v	—	50	—	50	ns
11	Data hold time (outputs) (after enable edge)	t_{ho}	0	—	0	—	ns

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, all timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted
2. Time to data active from high-impedance state
3. Assumes 200 pF load on SCK, MOSI, and MISO pins

Description	Temperature	Frequency	MC Order Number
20 Kbytes custom ROM	0°C to +70°°C	3 MHz	MC68HC11E20FN3
	–40°C to +85°C	2 MHz	MC68HC11E20CFN2
		3 MHz	MC68HC11E20CFN3
	–40°C to +105°C	2 MHz	MC68HC11E20VFN2
	–40°C to +125°C	2 MHz	MC68HC11E20MFN2

64-pin quad flat pack (QFP)

Custom ROM	0°C to +70°°C	3 MHz	MC68HC11E9FU3
	–40°C to +85°C	2 MHz	MC68HC11E9CFU2
		3 MHz	MC68HC11E9CFU3
	–40°C to +105°C	2 MHz	MC68HC11E9VFU2
	–40°C to +125°C	2 MHz	MC68HC11E9MFU2

64-pin quad flat pack (continued)

20 Kbytes Custom ROM	0°C to +70°°C	3 MHz	MC68HC11E20FU3
	–40°C to +85°C	2 MHz	MC68HC11E20CFU2
		3 MHz	MC68HC11E20CFU3
	–40°C to +105°C	2 MHz	MC68HC11E20VFU2
	–40°C to +125°C	2 MHz	MC68HC11E20MFU2

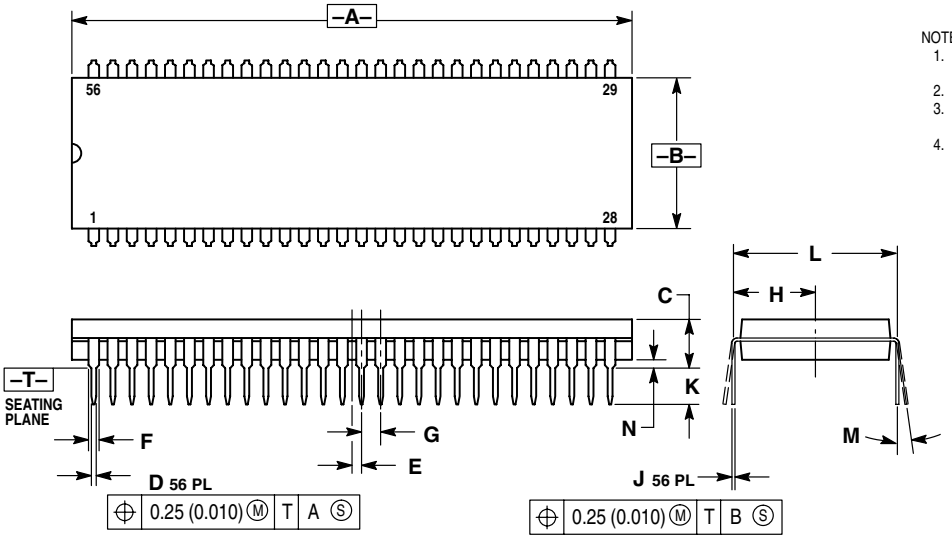
52-pin thin quad flat pack (10 mm x 10 mm)

Custom ROM	0°C to +70°°C	3 MHz	MC68HC11E9PB3
	–40°C to +85°C	2 MHz	MC68HC11E9CPB2
		3 MHz	MC68HC11E9CPB3
	–40°C to +105°C	2 MHz	MC68HC11E9VPB2
	–40°C to +125°C	2 MHz	MC68HC11E9MPB2

56-pin dual in-line package with 0.70-inch lead spacing (SDIP)

Custom ROM	0°C to +70°°C	3 MHz	MC68HC11E9B3
	–40°C to +85°C	2 MHz	MC68HC11E9CB2
		3 MHz	MC68HC11E9CB3
	–40°C to +105°C	2 MHz	MC68HC11E9VB2
	–40°C to +125°C	2 MHz	MC68HC11E9MB2

11.9 56-Pin Dual in-Line Package (Case 859)



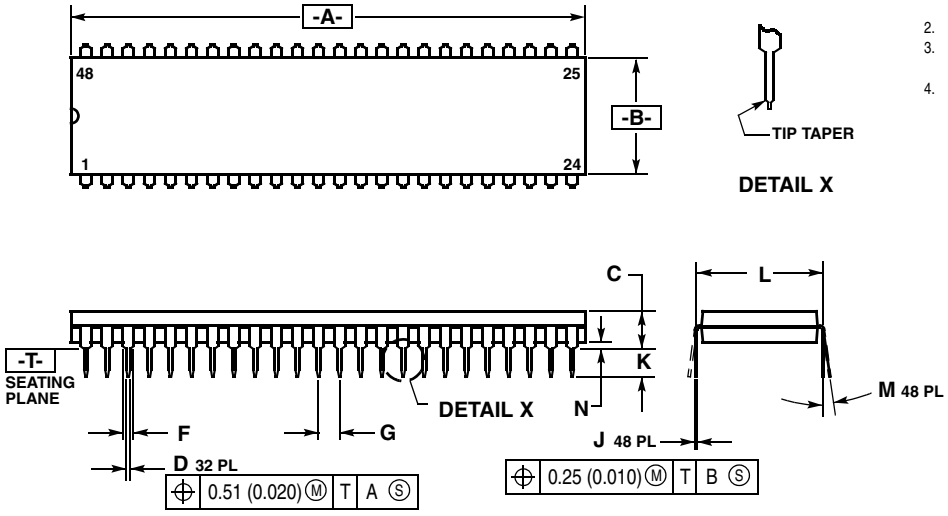
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.035	2.065	51.69	52.45
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
E	0.035 BSC		0.89 BSC	
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

11.10 48-Pin Plastic DIP (Case 767)

NOTE

The MC68HC811E2 is the only member of the E series that is offered in a 48-pin plastic dual in-line package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.415	2.445	61.34	62.10
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.55
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.070 BSC		1.79 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.150	2.92	3.81
L	0.600 BSC		15.24 BSC	
M	0×	15×	0×	15×
N	0.020	0.040	0.51	1.01

Appendix B
EVBU Schematic

Refer to Figure B-1 for a schematic diagram of the M68HC11EVBU Universal Evaluation Board. This diagram is included for reference only.

Freescale Semiconductor
Application Note

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M68HC11 Bootstrap Mode

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Introduction

The M68HC11 Family of MCUs (microcontroller units) has a bootstrap mode that allows a user-defined program to be loaded into the internal random-access memory (RAM) by way of the serial communications interface (SCI); the M68HC11 then executes this loaded program. The loaded program can do anything a normal user program can do as well as anything a factory test program can do because protected control bits are accessible in bootstrap mode. Although the bootstrap mode is a single-chip mode of operation, expanded mode resources are accessible because the mode control bits can be changed while operating in the bootstrap mode.

This application note explains the operation and application of the M68HC11 bootstrap mode. Although basic concepts associated with this mode are quite simple, the more subtle implications of these functions require careful consideration. Useful applications of this mode are overlooked due to an incomplete understanding of bootstrap mode. Also, common problems associated with bootstrap mode could be avoided by a more complete understanding of its operation and implications.

Topics discussed in this application note include:

- Basic operation of the M68HC11 bootstrap mode
- General discussion of bootstrap mode uses
- Detailed explanation of on-chip bootstrap logic
- Detailed explanation of bootstrap firmware
- Bootstrap firmware vs. EEPROM security
- Incorporating the bootstrap mode into a system
- Driving bootstrap mode from another M68HC11
- Driving bootstrap mode from a personal computer
- Common bootstrap mode problems
- Variations for specific versions of M68HC11
- Commented listings for selected M68HC11 bootstrap ROMs

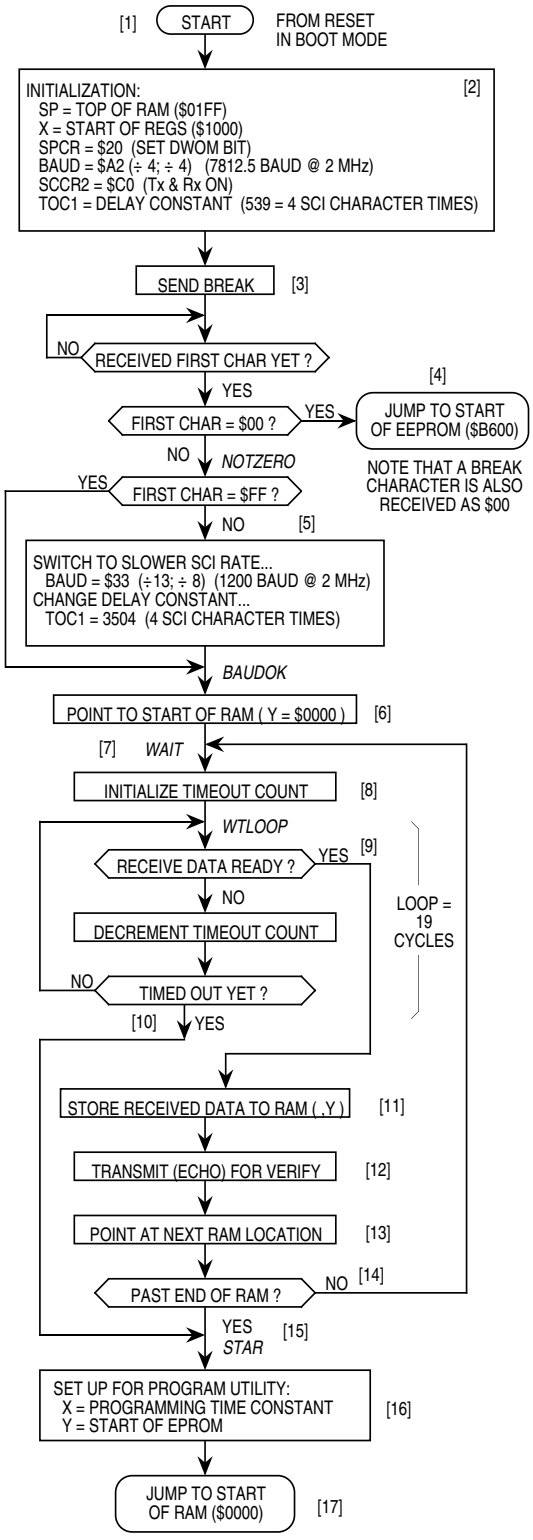

Figure 3. MC68HC711E9 Bootloader Flowchart

Bootloading a Program to Performa ROM Checksum

The bootloader ROM must be turned off before performing the checksum program. To remove the boot ROM from the memory map, clear the RBOOT bit in the HPRIO register. This is normally a write-protected bit that is 0, but in bootstrap mode it is reset to 1 and can be written. If the boot ROM is not disabled, the checksum routine will read the contents of the boot ROM rather than the user's mask ROM or EPROM at the same addresses.

Inherent Delays Caused by Double Buffering of SCI Data

This problem is troublesome in cases where one MCU is bootloading to another MCU.

Because of transmitter double buffering, there may be one character in the serial shifter as a new character is written into the transmit data register. In cases such as downloading in which this 2-character pipeline is kept full, a 2-character time delay occurs between when a character is written to the transmit data register and when that character finishes transmitting. A little more than one more character time delay occurs between the target MCU receiving the character and echoing it back. If the master MCU waits for the echo of each downloaded character before sending the next one, the download process takes about twice as long as it would if transmission is treated as a separate process or if verify data is ignored.

Boot ROM Variations

Different versions of the M68HC11 have different versions of the bootstrap ROM program. Table 3 summarizes the features of the boot ROMs in 16 members of the M68HC11 Family.

The boot ROMs for the MC68HC11F1, the MC68HC711K4, and the MC68HC11K4 allow additional choices of baud rates for bootloader communications. For the three new baud rates, the first character used to determine the baud rate is not $FF as it was in earlier M68HC11s. The intercharacter delay that terminates the variable-length download is also different for these new baud rates. Table 3 shows the synchronization characters, delay times, and baud rates as they relate to E-clock frequency.

Commented Boot ROM Listing

Listing 3. MC68HC711E9 Bootloader ROM contains a complete commented listing of the boot ROM program in the MC68HC711E9 version of the M68HC11. Other versions can be found in **Appendix B** of the *M68HC11 Reference Manual*.

Table 3. Bootloader Baud Rates

Sync Character	Timeout Delay	Baud Rates at E Clock =					
		2 MHz	2.1 MHz	3 MHz	3.15 MHz	4 MHz	4.2 MHz
$FF	4 characters	7812	8192	11,718	12,288	15,624	16,838
$FF	4 characters	1200	1260	1800	1890	2400	2520
$F0	4.9 characters	9600	10,080	14,400	15,120	19,200	20,160
$FD	17.3 characters	5208	5461	7812	8192	10,416	10,922
$FD	13 characters	3906	4096	5859	6144	7812	8192

Listing 3. MC68HC711E9 Bootloader ROM

```
                ****************************************************
                * BOOTLOADER FIRMWARE FOR 68HC711E9 - 21 Aug 89
                ****************************************************
                * Features of this bootloader are...
                *
                * Auto baud select between 7812.5 and 1200 (8 MHz)
                * 0 - 512 byte variable length download
                * Jump to EEPROM at $B600 if 1st download byte = $00
                * PROGRAM - Utility subroutine to program EPROM
                * UPLOAD - Utility subroutine to dump memory to host
                * Mask I.D. at $BFD4 = $71E9
                ****************************************************
                * Revision A -
                *
                * Fixed bug in PROGRAM routine where the first byte
                * programmed into the EPROM was not transmitted for
                * verify.
                * Also added to PROGRAM routine a skip of bytes
                * which were already programmed to the value desired.
                *
                * This new version allows variable length download
                * by quitting reception of characters when an idle
                * of at least four character times occurs
                *
                ****************************************************

                * EQUATES FOR USE WITH INDEX OFFSET = $1000
                *
0008            PORTD     EQU     $08
000E            TCNT      EQU     $0E
0016            TOC1      EQU     $16
0023            TFLG1     EQU     $23
                * BIT EQUATES FOR TFLG1
0080            OC1F      EQU     $80
                *
0028            SPCR      EQU     $28             (FOR DWOM BIT)
002B            BAUD      EQU     $2B
002D            SCCR2     EQU     $2D
002E            SCSR      EQU     $2E
002F            SCDAT     EQU     $2F
003B            PPROG     EQU     $3B
                * BIT EQUATES FOR PPROG
0020            ELAT      EQU     $20
0001            EPGM      EQU     $01
                *


                * MEMORY CONFIGURATION EQUATES
                *
B600            EEPMSTR   EQU     $B600           Start of EEPROM
B7FF            EEPMEND   EQU     $B7FF           End of EEPROM
                *
```