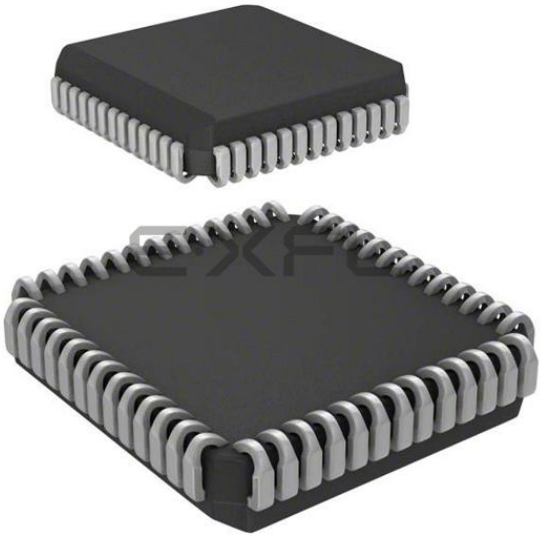

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	12KB (12K x 8)
Program Memory Type	OTP
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc711e9cfne3

Revision History

Date	Revision Level	Description	Page Number(s)
May, 2001	3.1	2.3.3.1 System Configuration Register — Addition to NOCOP bit description	44
		Added 10.21 EPROM Characteristics	175
June, 2001	3.2	10.21 EPROM Characteristics — For clarity, addition to note 2 following the table	175
December, 2001	3.3	7.7.2 Serial Communications Control Register 1 — SCCR1 bit 4 (M) description corrected	110
July, 2002	4	10.7 MC68L11E9/E20 DC Electrical Characteristics — Title changed to include the MC68L11E20	153
		10.8 MC68L11E9/E20 Supply Currents and Power Dissipation — Title changed to include the MC68L11E20	154
		10.10 MC68L11E9/E20 Control Timing — Title changed to include the MC68L11E20	157
		10.12 MC68L11E9/E20 Peripheral Port Timing — Title changed to include the MC68L11E20	163
		10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics — Title changed to include the MC68L11E20	167
		10.16 MC68L11E9/E20 Expansion Bus Timing Characteristics — Title changed to include the MC68L11E20	169
		10.18 MC68L11E9/E20 Serial Peirpheral Interface Characteristics — Title changed to include the MC68L11E20	172
		— Title changed to include the MC68L11E20	175
		11.4 Extended Voltage Device Ordering Information (3.0 Vdc to 5.5 Vdc) — Updated table to include MC68L1120	181
June, 2003	5	Format updated to current publications standards	Throughout
		1.4.6 Non-Maskable Interrupt (XIRQ/VPPE) — Added Caution note pertaining to EPROM programming of the MC68HC711E9 device only.	23
		6.4 Port C — Clarified description of DDRC[7:0] bits	100
		10.21 EPROM Characteristics — Added note pertaining to EPROM programming of the MC68HC711E9 device only.	175
July, 2005	5.1	Updated to meet Freescale identity guidelines.	Throughout

- Computer operating properly (COP) watchdog system
- 38 general-purpose input/output (I/O) pins:
  - 16 bidirectional I/O pins
  - 11 input-only pins
  - 11 output-only pins
- Several packaging options:
  - 52-pin plastic-leaded chip carrier (PLCC)
  - 52-pin windowed ceramic leaded chip carrier (CLCC)
  - 52-pin plastic thin quad flat pack, 10 mm x 10 mm (TQFP)
  - 64-pin quad flat pack (QFP)
  - 48-pin plastic dual in-line package (DIP), MC68HC811E2 only
  - 56-pin plastic shrink dual in-line package, .070-inch lead spacing (SDIP)

1.3 Structure

See Figure 1-1 for a functional diagram of the E-series MCUs. Differences among devices are noted in the table accompanying Figure 1-1.

1.4 Pin Descriptions

M68HC11 E-series MCUs are available packaged in:

- 52-pin plastic-leaded chip carrier (PLCC)
- 52-pin windowed ceramic leaded chip carrier (CLCC)
- 52-pin plastic thin quad flat pack, 10 mm x 10 mm (TQFP)
- 64-pin quad flat pack (QFP)
- 48-pin plastic dual in-line package (DIP), MC68HC811E2 only
- 56-pin plastic shrink dual in-line package, .070-inch lead spacing (SDIP)

Most pins on these MCUs serve two or more functions, as described in the following paragraphs. Refer to Figure 1-2, Figure 1-3, Figure 1-4, Figure 1-5, and Figure 1-6 which show the M68HC11 E-series pin assignments for the PLCC/CLCC, QFP, TQFP, SDIP, and DIP packages.

2.3.3.1 System Configuration Register

The system configuration register (CONFIG) consists of an EEPROM byte and static latches that control the startup configuration of the MCU. The contents of the EEPROM byte are transferred into static working latches during reset sequences. The operation of the MCU is controlled directly by these latches and not by CONFIG itself. In normal modes, changes to CONFIG do not affect operation of the MCU until after the next reset sequence. When programming, the CONFIG register itself is accessed. When the CONFIG register is read, the static latches are accessed. See 2.5.1 EEPROM and CONFIG Programming and Erasure for information on modifying CONFIG.

To take full advantage of the MCU's functionality, customers can program the CONFIG register in bootstrap mode. This can be accomplished by setting the mode pins to logic 0 and downloading a small program to internal RAM. For more information, Freescale application note AN1060 entitled M68HC11 Bootstrap Mode has been included at the back of this document. The downloadable talker will consist of:

- Bulk erase
- Byte programming
- Communication server

All of this functionality is provided by PCbug11 which can be found on the Freescale Web site at http://www.freescale.com. For more information on using PCbug11 to program an E-series device, Freescale engineering bulletin EB296 entitled Programming MC68HC711E9 Devices with PCbug11 and the M68HC11EVBU has been included at the back of this document.

NOTE

The CONFIG register on the 68HC11 is an EEPROM cell and must be programmed accordingly.

Operation of the CONFIG register in the MC68HC811E2 differs from other devices in the M68HC11 E series. See Figure 2-10 and Figure 2-11.

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:					NOSEC	NOCOP	ROMON	EEON
Write:								
Resets:								
Single chip:	0	0	0	0	U	U	1	U
Bootstrap:	0	0	0	0	U	U(L)	U	U
Expanded:	0	0	0	0	1	U	U	U
Test:	0	0	0	0	1	U(L)	U	U

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

Figure 2-10. System Configuration Register (CONFIG)

Table 2-4. RAM Mapping

RAM[3:0]	Address
0000	$0000–$0xFF
0001	$1000–$1xFF
0010	$2000–$2xFF
0011	$3000–$3xFF
0100	$4000–$4xFF
0101	$5000–$5xFF
0110	$6000–$6xFF
0111	$7000–$7xFF
1000	$8000–$8xFF
1001	$9000–$9xFF
1010	$A000–$AxFF
1011	$B000–$BxFF
1100	$C000–$CxFF
1101	$D000–$DxFF
1110	$E000–$ExFF
1111	$F000–$FxFF

Table 2-5. Register Mapping

REG[3:0]	Address
0000	$0000–$003F
0001	$1000–$103F
0010	$2000–$203F
0011	$3000–$303F
0100	$4000–$403F
0101	$5000–$503F
0110	$6000–$603F
0111	$7000–$703F
1000	$8000–$803F
1001	$9000–$903F
1010	$A000–$A03F
1011	$B000–$B03F
1100	$C000–$C03F
1101	$D000–$D03F
1110	$E000–$E03F
1111	$F000–$F03F

2.3.3.3 System Configuration Options Register

The 8-bit, special-purpose system configuration options register (OPTION) sets internal system configuration options during initialization. The time protected control bits, IRQE, DLY, and CR[1:0], can be written only once after a reset and then they become read-only. This minimizes the possibility of any accidental changes to the system configuration.

Address: $1039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME		CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time during special modes.

= Unimplemented

Figure 2-13. System Configuration Options Register (OPTION)

ADPU — Analog-to-Digital Converter Power-Up Bit

Refer to Chapter 3 Analog-to-Digital (A/D) Converter.

CSEL — Clock Select Bit

Selects alternate clock source for on-chip EEPROM charge pump. Refer to 2.5.1 EEPROM and CONFIG Programming and Erasure for more information on EEPROM use.

CSEL also selects the clock source for the A/D converter, a function discussed in Chapter 3 Analog-to-Digital (A/D) Converter.

2.4.1 Programming an Individual EPROM Address

- In this method, the MCU programs its own EPROM by controlling the PPROG register (EPROG in MC68HC711E20). Use these procedures to program the EPROM through the MCU with:
- The ROMON bit set in the CONFIG register
- The 12-volt nominal programming voltage present on the $\overline{\text{XIRQ}}/V_{PPE}$ pin
- The $\overline{\text{IRQ}}$ pin must be pulled high.

NOTE

Any operating mode can be used.

This example applies to all devices with EPROM/OTPROM except for the MC68HC711E20.

```
EPROG   LDAB    #$20
        STAB    $103B   Set ELAT bit in (EPGM = 0) to enable
                        EPROM latches.
        STAA    $0,X    Store data to EPROM address
        LDAB    #$21
        STAB    $103B   Set EPGM bit with ELAT = 1 to enable
                        EPROM programming voltage
        JSR     DLYEP   Delay 2-4 ms
        CLR     $103B   Turn off programming voltage and set
                        to READ mode
```

This example applies only to MC68HC711E20.

```
EPROG   LDAB    #$20
        STAB    $1036   Set ELAT bit (EPGM = 0) to enable
                        EPROM latches.
        STAA    $0,X    Store data to EPROM address
        LDAB    #$21
        STAB    $1036   Set EPGM bit with ELAT = 1 to enable
                        EPROM programming voltage
        JSR     DLYEP   Delay 2-4 ms
        CLR     $1036   Turn off programming voltage and set
                        to READ mode
```

2.4.2 Programming the EPROM with Downloaded Data

When using this method, the EPROM is programmed by software while in the special test or bootstrap modes. User-developed software can be uploaded through the SCI or a ROM-resident EPROM programming utility can be used. The 12-volt nominal programming voltage must be present on the $\overline{\text{XIRQ}}/V_{PPE}$ pin. To use the resident utility, bootload a 3-byte program consisting of a single jump instruction to $BF00. $BF00 is the starting address of a resident EPROM programming utility. The utility program sets the X and Y index registers to default values, then receives programming data from an external host, and puts it in EPROM. The value in IX determines programming delay time. The value in IY is a pointer to the first address in EPROM to be programmed (default = $D000).

When the utility program is ready to receive programming data, it sends the host the $FF character. Then it waits. When the host sees the $FF character, the EPROM programming data is sent, starting with the first location in the EPROM array. After the last byte to be programmed is sent and the corresponding verification data is returned, the programming operation is terminated by resetting the MCU.

For more information, Freescale application note AN1060 entitled M68HC11 Bootstrap Mode has been included at the back of this document.

3.3 A/D Converter Power-Up and Clock Select

Bit 7 of the OPTION register controls A/D converter power-up. Clearing ADPU removes power from and disables the A/D converter system. Setting ADPU enables the A/D converter system. Stabilization of the analog bias voltages requires a delay of as much as 100 µs after turning on the A/D converter. When the A/D converter system is operating with the MCU E clock, all switching and comparator operations are inherently synchronized to the main MCU clocks. This allows the comparator output to be sampled at relatively quiet times during MCU clock cycles. Since the internal RC oscillator is asynchronous to the MCU clock, there is more error attributable to internal system clock noise. A/D converter accuracy is reduced slightly while the internal RC oscillator is being used (CSEL = 1).

Address: $1039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME		CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

= Unimplemented

Figure 3-4. System Configuration Options Register (OPTION)

ADPU — A/D Power-Up Bit

0 = A/D powered down
1 = A/D powered up

CSEL — Clock Select Bit

0 = A/D and EEPROM use system E clock.
1 = A/D and EEPROM use internal RC clock.

IRQE — Configure $\overline{\text{IRQ}}$ for Edge-Sensitive Only Operation

Refer to Chapter 5 Resets and Interrupts.

DLY — Enable Oscillator Startup Delay Bit

0 = The oscillator startup delay coming out of stop is bypassed and the MCU resumes processing within about four bus cycles.
1 = A delay of approximately 4000 E-clock cycles is imposed as the MCU is started up from the stop power-saving mode. This delay allows the crystal oscillator to stabilize.

CME — Clock Monitor Enable Bit

Refer to Chapter 5 Resets and Interrupts.

Bit 2 — Not implemented

Always reads 0

CR[1:0] — COP Timer Rate Select Bits

Refer to Chapter 5 Resets and Interrupts and Chapter 9 Timing Systems.

When this control bit is clear, the four requested conversions are performed once to fill the four result registers. When this control bit is set, conversions are performed continuously with the result registers updated as data becomes available.

MULT — Multiple Channel/Single Channel Control Bit

When this bit is clear, the A/D converter system is configured to perform four consecutive conversions on the single channel specified by the four channel select bits CD:CA (bits [3:0] of the ADCTL register). When this bit is set, the A/D system is configured to perform a conversion on each of four channels where each result register corresponds to one channel.

NOTE

When the multiple-channel continuous scan mode is used, extra care is needed in the design of circuitry driving the A/D inputs. The charge on the capacitive DAC array before the sample time is related to the voltage on the previously converted channel. A charge share situation exists between the internal DAC capacitance and the external circuit capacitance. Although the amount of charge involved is small, the rate at which it is repeated is every 64 μs for an E clock of 2 MHz. The RC charging rate of the external circuit must be balanced against this charge sharing effect to avoid errors in accuracy. Refer to M68HC11 Reference Manual, Freescale document order number M68HC11RM/AD, for further information.

CD:CA — Channel Selects D:A Bits

Refer to Table 3-2. When a multiple channel mode is selected (MULT = 1), the two least significant channel select bits (CB and CA) have no meaning and the CD and CC bits specify which group of four channels is to be converted.

Table 3-2. A/D Converter Channel Selection

Channel Select Control Bits CD:CC:CB:CA	Channel Signal	Result in ADRx if MULT = 1
0000	AN0	ADR1
0001	AN1	ADR2
0010	AN2	ADR3
0011	AN3	ADR4
0100	AN4	ADR1
0101	AN5	ADR2
0110	AN6	ADR3
0111	AN7	ADR4
10XX	Reserved	—
1100	V_{RH}(1)	ADR1
1101	V_{RL}(1)	ADR2
1110	(V_{RH})/2(1)	ADR3
1111	Reserved(1)	ADR4

1. Used for factory testing

3.10 A/D Converter Result Registers

These read-only registers hold an 8-bit conversion result. Writes to these registers have no effect. Data in the A/D converter result registers is valid when the CCF flag in the ADCTL register is set, indicating a conversion sequence is complete. If conversion results are needed sooner, refer to Figure 3-3, which shows the A/D conversion sequence diagram.

Register name: Analog-to-Digital Converter Result Register 1 Address: $1031

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Indeterminate after reset							

Register name: Analog-to-Digital Converter Result Register 2 Address: $1032

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Indeterminate after reset							

Register name: Analog-to-Digital Converter Result Register 3 Address: $1033

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Indeterminate after reset							

Register name: Analog-to-Digital Converter Result Register 4 Address: $1034

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Indeterminate after reset							

= Unimplemented

Figure 3-6. Analog-to-Digital Converter Result Registers (ADR1–ADR4)

4.4 Opcodes and Operands

The M68HC11 Family of microcontrollers uses 8-bit opcodes. Each opcode identifies a particular instruction and associated addressing mode to the CPU. Several opcodes are required to provide each instruction with a range of addressing capabilities. Only 256 opcodes would be available if the range of values were restricted to the number able to be expressed in 8-bit binary numbers.

A 4-page opcode map has been implemented to expand the number of instructions. An additional byte, called a prebyte, directs the processor from page 0 of the opcode map to one of the other three pages. As its name implies, the additional byte precedes the opcode.

A complete instruction consists of a prebyte, if any, an opcode, and zero, one, two, or three operands. The operands contain information the CPU needs for executing the instruction. Complete instructions can be from one to five bytes long.

4.5 Addressing Modes

Six addressing modes can be used to access memory:

- Immediate
- Direct
- Extended
- Indexed
- Inherent
- Relative

These modes are detailed in the following paragraphs. All modes except inherent mode use an effective address. The effective address is the memory address from which the argument is fetched or stored or the address from which execution is to proceed. The effective address can be specified within an instruction, or it can be calculated.

4.5.1 Immediate

In the immediate addressing mode, an argument is contained in the byte(s) immediately following the opcode. The number of bytes following the opcode matches the size of the register or memory location being operated on. There are 2-, 3-, and 4- (if prebyte is required) byte immediate instructions. The effective address is the address of the byte following the instruction.

4.5.2 Direct

In the direct addressing mode, the low-order byte of the operand address is contained in a single byte following the opcode, and the high-order byte of the address is assumed to be $00. Addresses $00–$FF are thus accessed directly, using 2-byte instructions. Execution time is reduced by eliminating the additional memory access required for the high-order address byte. In most applications, this 256-byte area is reserved for frequently referenced data. In M68HC11 MCUs, the memory map can be configured for combinations of internal registers, RAM, or external memory to occupy these addresses.

Table 4-2. Instruction Set (Sheet 7 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
TSTA	Test A for Zero or Minus	A – 0	A INH	4D	—	2	—	—	—	—	Δ	Δ	0	0
TSTB	Test B for Zero or Minus	B – 0	B INH	5D	—	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 ⇒ IX	INH	30	—	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 ⇒ IY	INH	18 30	—	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 ⇒ SP	INH	35	—	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 ⇒ SP	INH	18 35	—	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E	—	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX ⇒ D, D ⇒ IX	INH	8F	—	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY ⇒ D, D ⇒ IY	INH	18 8F	—	4	—	—	—	—	—	—	—	—

Cycle

* Infinity or until reset occurs

** 12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (14 + n total).

Operands

`dd` = 8-bit direct address ($0000–$00FF) (high byte assumed to be $00)
`ff` = 8-bit positive offset $00 (0) to $FF (255) (is added to index)
`hh` = High-order byte of 16-bit extended address
`ii` = One byte of immediate data
`jj` = High-order byte of 16-bit immediate data
`kk` = Low-order byte of 16-bit immediate data
`ll` = Low-order byte of 16-bit extended address
`mm` = 8-bit mask (set bits to be affected)
`rr` = Signed relative offset $80 (–128) to $7F (+127)
(offset relative to address following machine code offset byte))

Operators

( ) Contents of register shown inside parentheses
⇐ Is transferred to
⇑ Is pulled from stack
⇓ Is pushed onto stack
• Boolean AND
\+ Arithmetic addition symbol except where used as inclusive-OR symbol in Boolean formula
⊕ Exclusive-OR
* Multiply
: Concatenation
– Arithmetic subtraction symbol or negation symbol (two's complement)

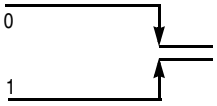
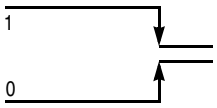
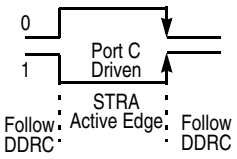
Condition Codes

— Bit not changed
0 Bit always cleared
1 Bit always set
Δ Bit cleared or set, depending on operation
↓ Bit can be cleared, cannot become set

6.8 Parallel I/O Control Register

The parallel handshake functions are available only in the single-chip operating mode. PIOC is a read/write register except for bit 7, which is read only. Table 6-2 shows a summary of handshake operations.

Table 6-2. Parallel I/O Control

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port B	Port C
Simple strobed mode	Read PIOC with STAF = 1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to PORTB
Full-input hand-shake mode	Read PIOC with STAF = 1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full-output hand-shake mode	Read PIOC with STAF = 1 then write PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level; follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

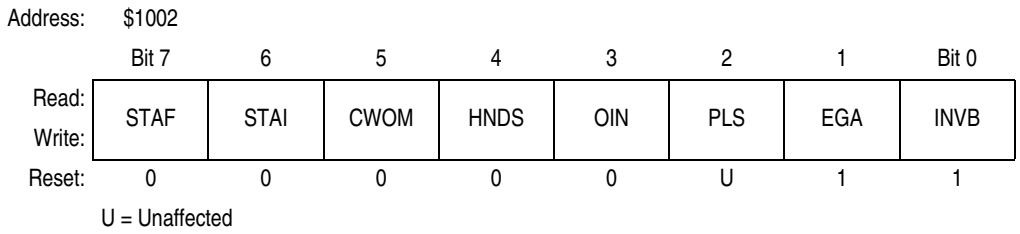


Figure 6-10. Parallel I/O Control Register (PIOC)

STAF — Strobe A Interrupt Status Flag

STAF is set when the selected edge occurs on strobe A. This bit can be cleared by a read of PIOC with STAF set followed by a read of PORTCL (simple strobed or full input handshake mode) or a write to PORTCL (output handshake mode).

0 = No edge on strobe A
1 = Selected edge on strobe A

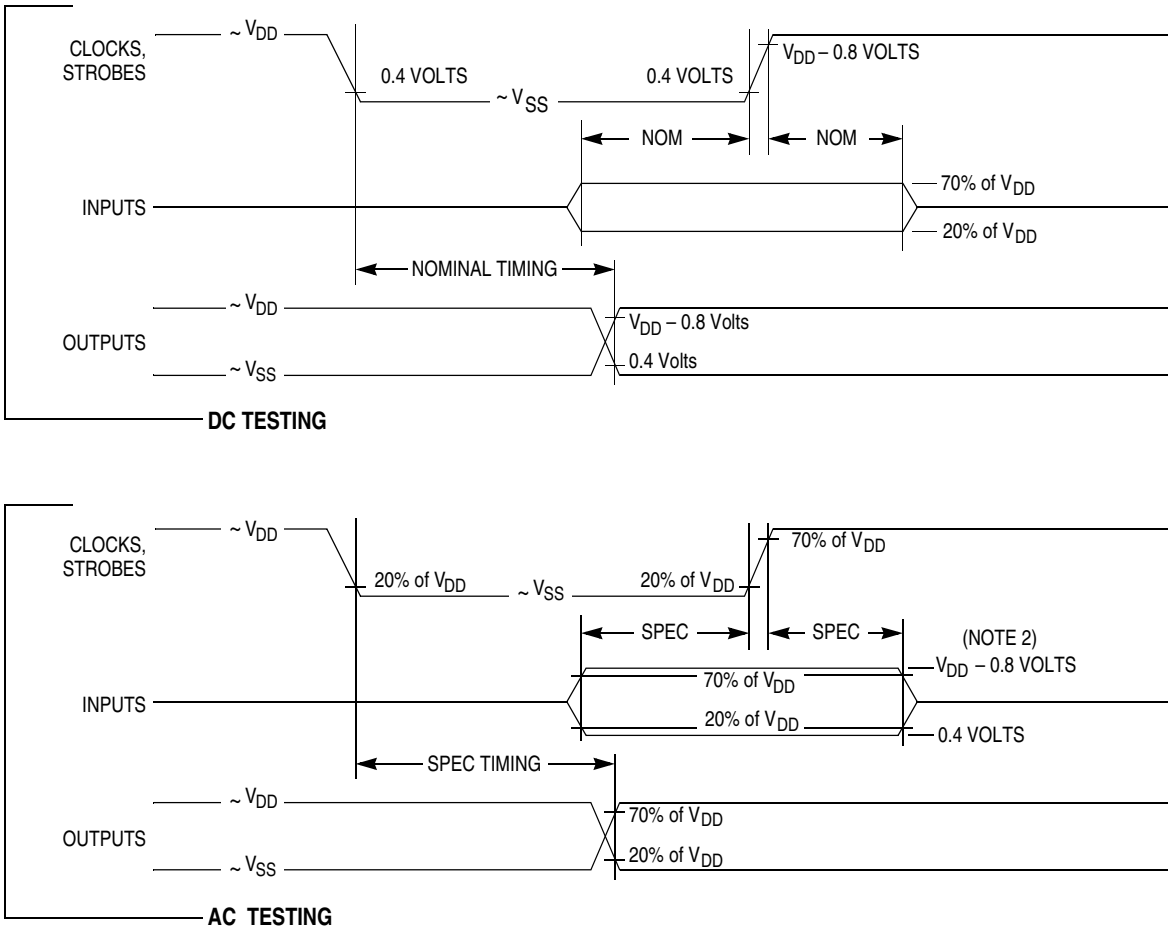
STAI — Strobe A Interrupt Enable Mask Bit

0 = STAF does not request interrupt
1 = STAF requests interrupt

10.5 DC Electrical Characteristics

Characteristics[1]	Symbol	Min	Max	Unit
Output voltage[2] I_{Load} = ±±10.0 µA All outputs except XTAL All outputs except XTAL, $\overline{RESET}$, and MODA	V_{OL}, V_{OH}	— V_{DD} –0.1	0.1 —	V
Output high voltage[2] I_{Load} = –0.8 mA, V_{DD} = 4.5 V All outputs except XTAL, $\overline{RESET}$, and MODA	V_{OH}	V_{DD} –0.8	—	V
Output low voltage I_{Load} = 1.6 mA All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage All inputs except $\overline{RESET}$ $\overline{RESET}$	V_{IH}	$0.7 \times V_{DD}$ $0.8 \times V_{DD}$	V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage, all inputs	V_{IL}	V_{SS} –0.3	$0.2 \times V_{DD}$	V
I/O ports, 3-state leakage $V_{In} = V_{IH}$ or V_{IL} PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$	I_{OZ}	—	±10	µA
Input leakage current[3] $V_{In} = V_{DD}$ or V_{SS} PA[2:0], $\overline{IRQ}$, $\overline{XIRQ}$ MODB/V_{STBY} ($\overline{XIRQ}$ on EPROM-based devices)	I_{In}	— —	±1 ±10	µA
RAM standby voltage, power down	V_{SB}	4.0	V_{DD}	V
RAM standby current, power down	I_{SB}	—	10	µA
Input capacitance PA[2:0], PE[7:0], $\overline{IRQ}$, $\overline{XIRQ}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$	C_{In}	— —	8 12	pF
Output load capacitance All outputs except PD[4:1] PD[4:1]	C_L	— —	90 100	pF

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
3. Refer to 10.13 Analog-to-Digital Converter Characteristics and 10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics for leakage current for port E.



Notes:
1. Full test loads are applied during all dc electrical tests and ac timing measurements.
2. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} – 0.8 volts while timing measurements are taken at 20% and 70% of V_{DD} points.

Figure 10-1. Test Methods

10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics

Characteristic[1]	Parameter[2]	Min	Absolute	Max	Unit
Resolution	Number of bits resolved by A/D converter	—	8	—	Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics	—	—	±1	LSB
Zero error	Difference between the output of an ideal and an actual for 0 input voltage	—	—	±1	LSB
Full scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	—	—	±1	LSB
Total unadjusted error	Maximum sum of non-linearity, zero error, and full-scale error	—	—	±1/2	LSB
Quantization error	Uncertainty because of converter resolution	—	—	±1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	—	—	±2	LSB
Conversion range	Analog input voltage range	V_{RL}	—	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	—	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} –0.1	—	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}	3.0	—	—	V
Conversion time	Total time to perform a single analog-to-digital conversion: E clock Internal RC oscillator	 — —	 32 —	 — t_{CYC}+ 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	—	Guaranteed	—	—
Zero input reading	Conversion result when $V_{In} = V_{RL}$	00	—	—	Hex
Full scale reading	Conversion result when $V_{In} = V_{RH}$	—	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling time: E clock Internal RC oscillator	 — —	 12 —	 — 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance during sample PE[7:0]	—	20 typical	—	pF
Input leakage	Input leakage on A/D pins PE[7:0] V_{RL}, V_{RH}	 — —	 — —	 400 1.0	 nA µA

1. V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤ E ≤ 2.0 MHz, unless otherwise noted
2. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.

Description	CONFIG	Temperature	Frequency	MC Order Number
52-pin windowed ceramic leaded chip carrier (CLCC)				
EPROM	$0F	–40°C to +85°C	2 MHz	MC68HC711E9CFS2
			3 MHz	MC68HC711E9CFS3
		–40°C to +105°C	2 MHz	MC68HC711E9VFS2
		–40°C to +125°C	2 MHz	MC68HC711E9VFS2
20 Kbytes EPROM	$0F	0°C o +70°°C	3 MHz	MC68HC711E20FS3
		–40°C to +85°C	2 MHz	MC68HC711E20CFS2
			3 MHz	MC68HC711E20CFS3
		–40°C to +105°C	2 MHz	MC68HC711E20VFS2
		–40°C to +125°C	2 MHz	MC68HC711E20MFS2
48-pin dual in-line package (DIP) — MC68HC811E2 only				
No ROM, 2 Kbytes EEPROM	$FF	0°C to +70°°C	2 MHz	MC68HC811E2P2
		–40°C to +85°C	2 MHz	MC68HC811E2CP2
		–40°C to +105°C	2 MHz	MC68HC811E2VP2
		–40°C to +125°C	2 MHz	MC68HC811E2MP2
56-pin dual in-line package with 0.70-inch lead spacing (SDIP)				
BUFFALO ROM	$0F	–40°C to +85°C	2 MHz	MC68HC11E9BCB2
			3 MHz	MC68HC11E9BCB3
No ROM	$0D	–40°C to +85°C	2 MHz	MC68HC11E1CB2
			3 MHz	MC68HC11E1CB3
		–40°C to +105°C	2 MHz	MC68HC11E1VB2
		–40°C to +125°C	2 MHz	MC68HC11E1MB2
No ROM, no EEPROM	$0C	–40°C to +85°C	2 MHz	MC68HC11E0CB2
			3 MHz	MC68HC11E0CB3
		–40°C to +105°C	2 MHz	MC68HC11E0VB2
		–40°C to +125°C	2 MHz	MC68HC11E0MB2

11.3 Custom ROM Device Ordering Information

Description	Temperature	Frequency	MC Order Number
52-pin plastic leaded chip carrier (PLCC)			
Custom ROM	0°C to +70°°C	3 MHz	MC68HC11E9FN3
	–40°C to +85°C	2 MHz	MC68HC11E9CFN2
		3 MHz	MC68HC11E9CFN3
	–40°C to +105°C	2 MHz	MC68HC11E9VFN2
	–40°C to +125°C	2 MHz	MC68HC11E9MFN2

The alternate vector locations are achieved by simply driving address bit A14 low during all vector fetches if SMOD = 1. For special test mode, the alternate vector locations assure that the reset vector can be fetched from external memory space so the test system can control MCU operation. In special bootstrap mode, the small boot ROM is enabled in the memory map by RBOOT = 1 so the reset vector will be fetched from this ROM and the bootloader firmware will control MCU operation.

RBOOT is reset to 1 in bootstrap mode to enable the small boot ROM. In the other three modes, RBOOT is reset to 0 to keep the boot ROM out of the memory map. While in special test mode, SMOD = 1, which allows the RBOOT control bit to be written to 1 by software to enable the boot ROM for testing purposes.

Boot ROM Firmware

The main program in the boot ROM is the bootloader, which is automatically executed as a result of resetting the MCU in bootstrap mode. Some newer versions of the M68HC11 Family have additional utility programs that can be called from a downloaded program. One utility is available to program EPROM or OTP versions of the M68HC11. A second utility allows the contents of memory locations to be uploaded to a host computer. In the MC68HC711K4 boot ROM, a section of code is used by Freescale for stress testing the on-chip EEPROM. These test and utility programs are similar to self-test ROM programs in other MCUs except that the boot ROM does not use valuable space in the normal memory map.

Bootstrap firmware is also involved in an optional EEPROM security function on some versions of the M68HC11. This EEPROM security feature prevents a software pirate from seeing what is in the on-chip EEPROM. The secured state is invoked by programming the no security (NOSEC) EEPROM bit in the CONFIG register. Once this NOSEC bit is programmed to 0, the MCU will ignore the mode A pin and always come out of reset in normal single-chip mode or special bootstrap mode, depending on the state of the mode B pin. Normal single-chip mode is the usual way a secured part would be used. Special bootstrap mode is used to disengage the security function (only after the contents of EEPROM and RAM have been erased). Refer to the *M68HC11 Reference Manual*, Freescale document order number M68HC11RM/AD, for additional information on the security mode and complete listings of the boot ROMs that support the EEPROM security functions.

Automatic Selection of Baud Rate

The bootloader program in the MC68HC711E9 accommodates either of two baud rates.

- The higher of these baud rates (7812 baud at a 2-MHz E-clock rate) is used in systems that operate from a binary frequency crystal such as 2^{23} Hz (8.389 MHz). At this crystal frequency, the baud rate is 8192 baud, which was used extensively in automotive applications.
- The second baud rate available to the M68HC11 bootloader is 1200 baud at a 2-MHz E-clock rate. Some of the newest versions of the M68HC11, including the MC68HC11F1 and MC68HC117K4, accommodate other baud rates using the same differentiation technique explained here. Refer to the reference numbers in square brackets in Figure 2 during the following explanation.

NOTE

Software can change some aspects of the memory map after reset.

```
 52 D000           EPRMSTR  EQU    $D000          Start of EPROM
 53 FFFF           EPRMEND  EQU    $FFFF          End of EPROM
 54                *
 55 0000           RAMSTR   EQU    $0000
 56 01FF           RAMEND   EQU    $01FF
 57
 58                * DELAY CONSTANTS
 59                *
 60 0DB0           DELAYS   EQU    3504           Delay at slow baud
 61 021B           DELAYF   EQU    539            Delay at fast baud
 62                *
 63 1068           PROGDEL  EQU    4200           2 ms programming delay
 64                *                       At 2.1 MHz
 65
 66                ************************************************
 67 BF00                     ORG    $BF00
 68                ************************************************
 69
 70                * Next two instructions provide a predictable place
 71                * to call PROGRAM and UPLOAD even if the routines
 72                * change size in future versions.
 73                *
 74 BF00 7EBF13     PROGRAM  JMP    PRGROUT        EPROM programming utility
 75 BF03           UPLOAD   EQU    *              Upload utility
 76
 77                ************************************************
 78                * UPLOAD - Utility subroutine to send data from
 79                * inside the MCU to the host via the SCI interface.
 80                * Prior to calling UPLOAD set baud rate, turn on SCI
 81                * and set Y=first address to upload.
 82                * Bootloader leaves baud set, SCI enabled, and
 83                * Y pointing at EPROM start ($D000) so these default
 84                * values do not have to be changed typically.
 85                * Consecutive locations are sent via SCI in an
 86                * infinite loop. Reset stops the upload process.
 87                ************************************************
 88 BF03 CE1000             LDX    #$1000         Point to internal registers
 89 BF06 18A600   UPLOOP    LDAA   0,Y            Read byte
 90 BF09 1F2E80FC           BRCLR  SCSR,X $80 *   Wait for TDRE
 91 BF0D A72F               STAA   SCDAT,X        Send it
 92 BF0F 1808               INY
 93 BF11 20F3               BRA    UPLOOP         Next...
 94
 95                ************************************************
 96                * PROGRAM - Utility subroutine to program EPROM.
 97                * Prior to calling PROGRAM set baud rate, turn on SCI
 98                * set X=2ms prog delay constant, and set Y=first
 99                * address to program. SP must point to RAM.
100                * Bootloader leaves baud set, SCI enabled, X=4200
101                * and Y pointing at EPROM start ($D000) so these
102                * default values don't have to be changed typically.
103                * Delay constant in X should be equivalent to 2 ms
104                *  at 2.1 MHz X=4200; at 1 MHz X=2000.
105                * An external voltage source is required for EPROM
106                * programming.
```

Step 6

Erase the CONFIG to allow programming of NOSEC bit (bit 3). It is also recommended to program the EEPROM at this point before programming the CONFIG register. Refer to the engineering bulletin *Programming MC68HC811E2 Devices with PCbug11 and the M68HC711E9PGMR*, Freescale document number EB184.

At the PCbug11command prompt, type: EEPROM ERASE BULK 103F

Step 7

You are now ready to enable the security feature on the MCHC811E2.

At the PCbug11 command prompt, type: MS 103F 05

The value $05 assumes the EEPROM is to be mapped from $0800 to $0FFF.

Step 8

After the programming operation is complete, verifying the CONFIG on the MCHC811E2 is not possible because in bootstrap mode the default value is always forced.

Step 9

The part is now in secure mode and whatever code you loaded into EEPROM will be erased if you tried to bring the microcontroller up in either expanded mode or bootstrap mode. The microcontroller will work properly in the secure mode only in single chip mode.

NOTE

If the part is placed in bootstrap mode or expanded mode, the code in EEPROM and RAM will be erased the microcontroller can be reused.

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