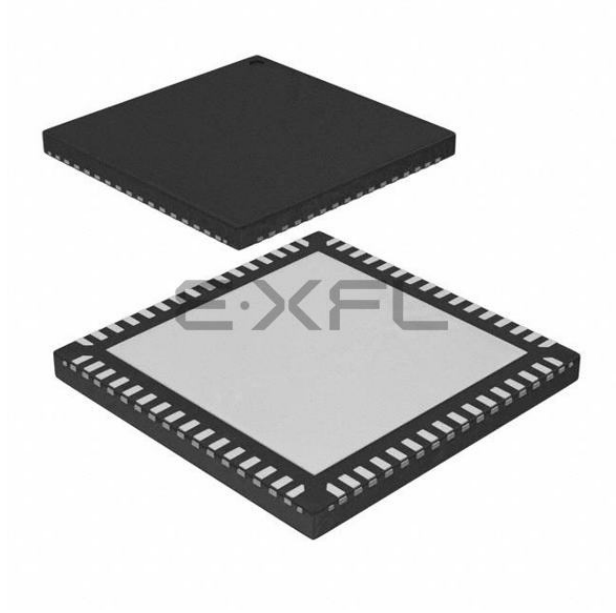

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SCI, SPI, UART/USART, USB |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.63V |
| Data Converters | A/D 20x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsaml21j18a-mut |

  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz internal oscillator (OSC32K)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 51 programmable I/O pins
- Easy migration from SAM D family
- Packages
  - 64-pin TQFP, QFN, WLCSP
  - 48-pin TQFP, QFN
  - 32-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

# 1. Description

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 40KB of SRAM. The SAM L21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM L21 devices provide the following features: In-system programmable Flash, 16-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 51 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC) where each TC/TCC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, the third TCC can operate in 16-bit mode. The series provide one full-speed USB 2.0 embedded host and device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, $I^2C$ up to 3.4MHz, SMBus, PMBus, and LIN slave; up to twenty channel 1MSPS 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two 12-bit 1MSPS DACs, two analog comparators with window mode, three independent cascadable OPAMPs supporting internal connection with others analog features, Peripheral Touch Controller supporting up to 192 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L21 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L21 devices have two software-selectable performance levels (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency. To further minimize consumption, specifically leakage dissipation, the SAM L21 devices utilizes power domain gating technique with retention to turn off some logic area while keeping its logic state. This technique is fully handled by hardware.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM L21 devices are supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

## 2. Configuration Summary

| | SAM L21J | SAM L21G | SAM L21E |
|---|---|---|---|
| Pins | 64 | 48 | 32 |
| General Purpose I/O-pins (GPIOs) | 51 | 37 | 25 |
| Flash | 256/128/64KB | 256/128/64KB | 256/128/64/32KB |
| Flash RWW section | 8/4/2KB | 8/4/2KB | 8/4/2/1KB |
| System SRAM | 32/16/8KB | 32/16/8KB | 32/16/8/4KB |
| Low Power SRAM | 8/8/4KB | 8/8/4KB | 8/8/4/2KB |
| Timer Counter (TC) instances(1) | 5 | 3 | 3 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Timer Counter for Control (TCC) instances | 3 | 3 | 3 |
| Waveform output channels per TCC | 8/4/2 | 8/4/2 | 6/4/2 |
| DMA channels | 16 | 16 | 16 |
| USB interface | 1 | 1 | 1 |
| AES engine | 1 | 1 | 1 |
| Configurable Custom Logic (CCL) (LUTs) | 4 | 4 | 4 |
| True Random Generator (TRNG) | 1 | 1 | 1 |
| Serial Communication Interface (SERCOM) instances | 6 | 6 | 6 |
| Analog-to-Digital Converter (ADC) channels | 20 | 14 | 10 |
| Analog Comparators (AC) | 2 | 2 | 2 |
| Digital-to-Analog Converter (DAC) channels | 2 | 2 | 2 |
| Operational Amplifier (OPAMP) | 3 | 3 | 3 |

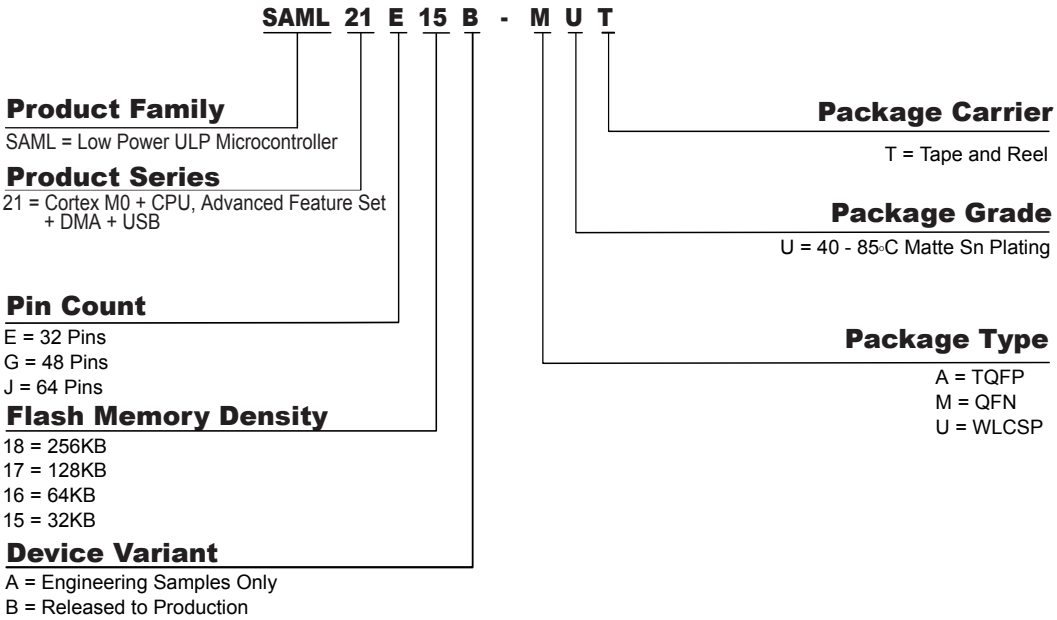
| | SAM L21J | SAM L21G | SAM L21E |
|---|---|---|---|
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or<br>two 16-bit values | One 32-bit value or<br>two 16-bit values | One 32-bit value or<br>two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance (2) | 169 (13x13) | 81 (9x9) | 42 (7x6) |
| Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only) (3) | 16 | 10 | 7 |
| Maximum CPU frequency | 48MHz | | |
| Packages | QFN<br>TQFP<br>WLCSP(4) | QFN<br>TQFP | QFN<br>TQFP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K)<br>0.4-32MHz crystal oscillator (XOSC)<br>32.768kHz internal oscillator (OSC32K)<br>32KHz ultra-low-power internal oscillator (OSCULP32K)<br>16/12/8/4MHz high-accuracy internal oscillator (OSC16M)<br>48MHz Digital Frequency Locked Loop (DFLL48M)<br>96MHz Fractional Digital Phased Locked Loop (FDPLL96M) | | |
| Event System channels | 12 | 12 | 12 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

**Note:**

1. For SAM L21E and SAM L21G, only TC0, TC1 and TC4 are available.
2. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. Refer to *Multiplexed Signals* for details. The number in the Configuration Summary is the maximum number of channels that can be obtained.

3. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.
4. WLCSP parts are programmed with a specific SPI bootloader. Refer to Application Note AT09002 for details.

# 3. Ordering Information




**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

## 3.1. SAM L21J

**Table 3-1. SAM L21J Ordering Codes**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML21J16B-AUT | 64K | 8K | TQFP64 | Tape & Reel |
| ATSAML21J16B-MUT | | | QFN64 | |
| ATSAML21J17B-AUT | 128K | 16K | TQFP64 | Tape & Reel |
| ATSAML21J17B-MUT | | | QFN64 | |
| ATSAML21J17B-UUT | | | WLCSP64 | |
| ATSAML21J18B-AUT | 256K | 32K | TQFP64 | Tape & Reel |
| ATSAML21J18B-MUT | | | QFN64 | |
| ATSAML21J18B-UUT | | | WLCSP64 | |

## 3.2. SAM L21G

**Table 3-2. SAM L21G Ordering Codes**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML21G16B-AUT | 64K | 8K | TQFP48 | Tape & Reel |
| ATSAML21G16B-MUT | | | QFN48 | |
| ATSAML21G17B-AUT | 128K | 16K | TQFP48 | Tape & Reel |
| ATSAML21G17B-MUT | | | QFN48 | |
| ATSAML21G18B-AUT | 256K | 32K | TQFP48 | Tape & Reel |
| ATSAML21G18B-MUT | | | QFN48 | |

## 3.3. SAM L21E

**Table 3-3. SAM L21E**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML21E15B-AUT | 32K | 4K | TQFP32 | Tape & Reel |
| ATSAML21E15B-MUT | | | QFN32 | |
| ATSAML21E16B-AUT | 64K | 8K | TQFP32 | Tape & Reel |
| ATSAML21E16B-MUT | | | QFN32 | |
| ATSAML21E17B-AUT | 128K | 16K | TQFP32 | Tape & Reel |
| ATSAML21E17B-MUT | | | QFN32 | |
| ATSAML21E18B-AUT | 256K | 32K | TQFP32 | Tape & Reel |
| ATSAML21E18B-MUT | | | QFN32 | |

## 3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L21 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

**Table 3-4. SAM L21 Device Identification Values**

| DEVSEL (DID[7:0]) | Device |
|---|---|
| 0x00 | SAML21J18A |
| 0x01 | SAML21J17A |
| 0x02 | SAML21J16A |
| 0x03-0x04 | Reserved |
| 0x05 | SAML21G18A |

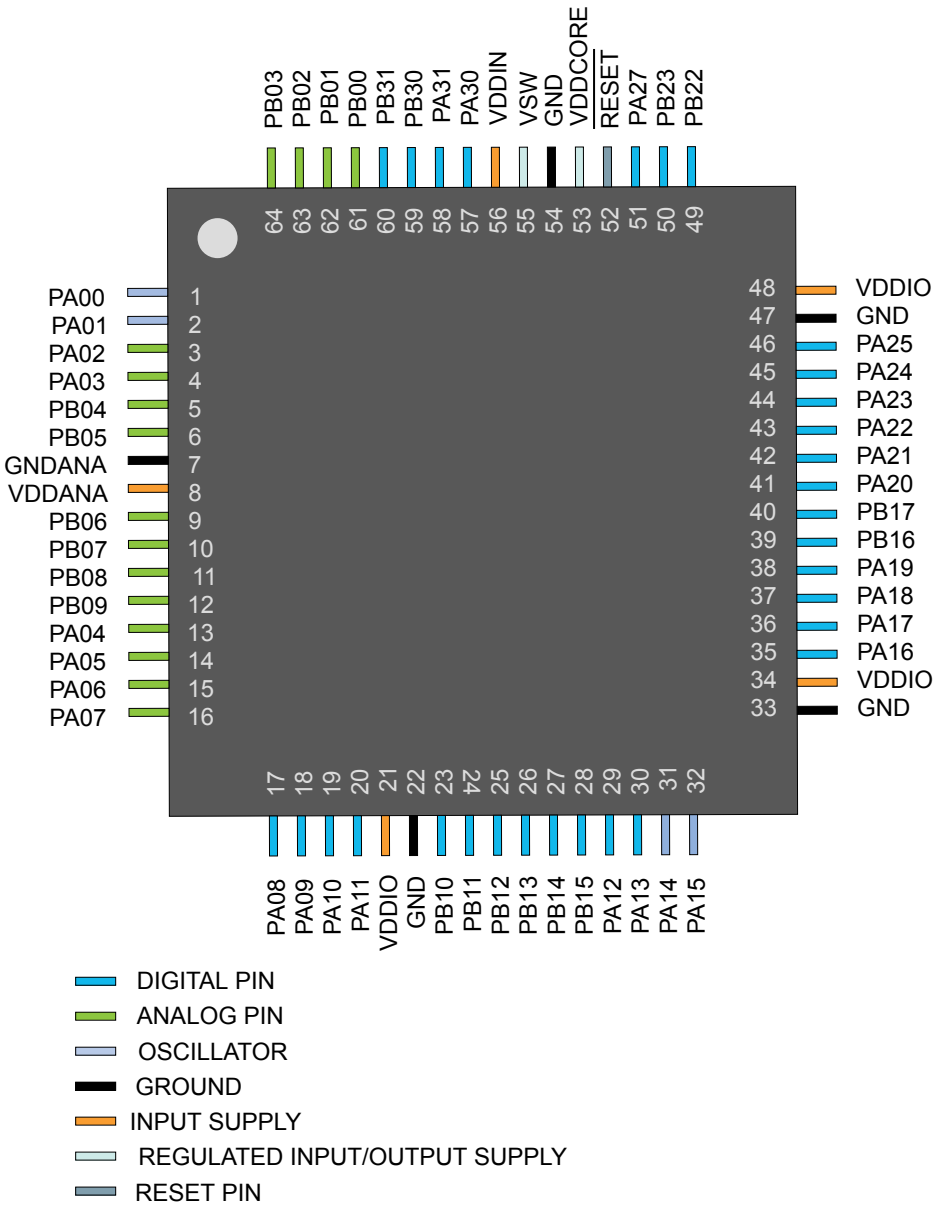
| DEVSEL (DID[7:0]) | Device |
|---|---|
| 0x06 | SAML21G17A |
| 0x07 | SAML21G16A |
| 0x08-0x09 | Reserved |
| 0x0A | SAML21E18A |
| 0x0B | SAML21E17A |
| 0x0C | SAML21E16A |
| 0x0D | SAML21E15A |
| 0x0E | Reserved |
| 0x0F | SAML21J18B |
| 0x10 | SAML21J17B |
| 0x11 | SAML21J16B |
| 0x12-0x13 | Reserved |
| 0x14 | SAML21G18B |
| 0x15 | SAML21G17B |
| 0x16 | SAML21G16B |
| 0x17-0x18 | Reserved |
| 0x19 | SAML21E18B |
| 0x1A | SAML21E17B |
| 0x1B | SAML21E16B |
| 0x1C | SAML21E15B |
| 0x1D-0xFF | Reserved |

**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

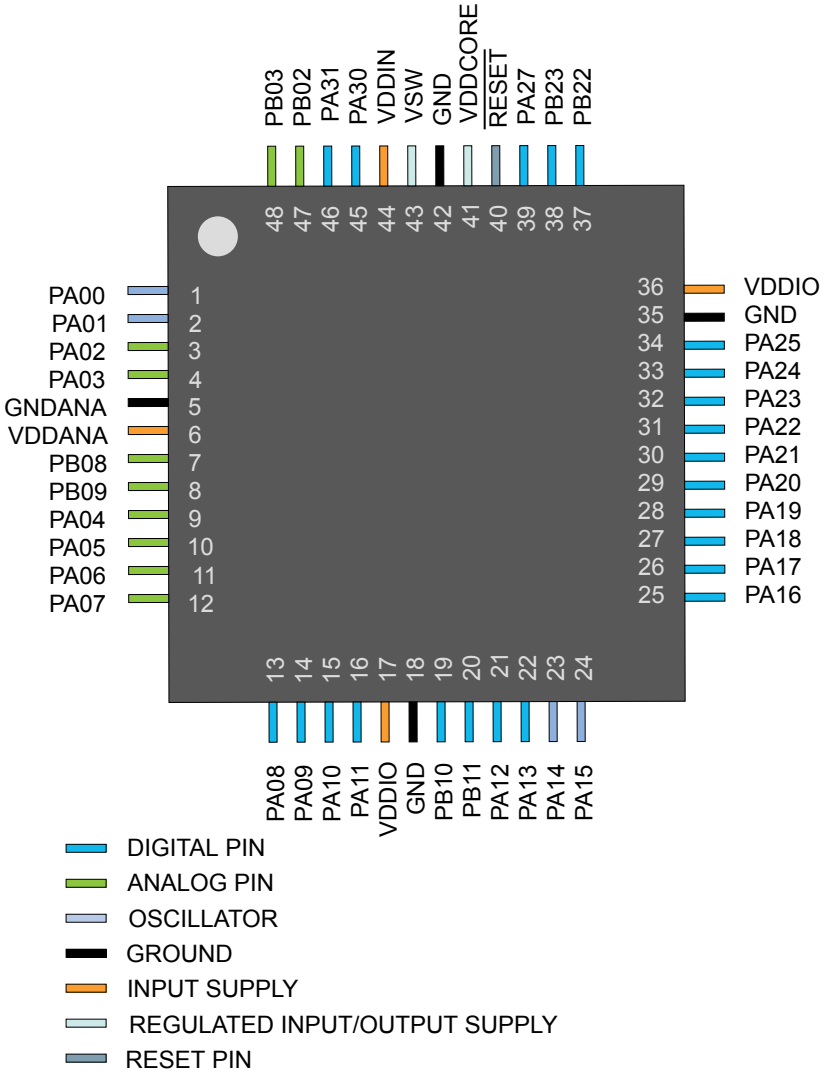
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

# 5. Pinout

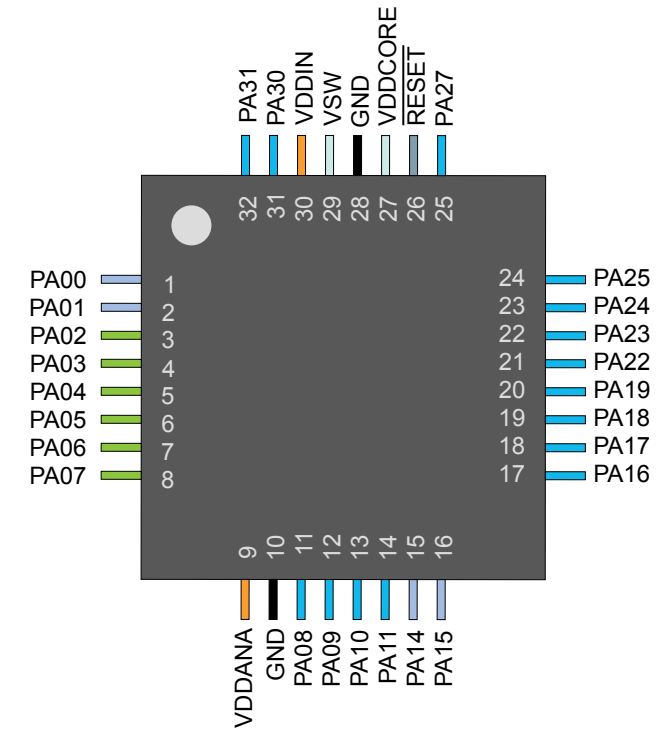
## 5.1. SAM L21J



## 5.3. SAM L21G


PB03
PB02
PA31
PA30
VDDIN
VSW
GND
VDDCORE
RESET
PA27
PB23
PB22
48
47
46
45
44
43
42
41
40
39
38
37
PA00
PA01
PA02
PA03
GNDANA
VDDANA
PB08
PB09
PA04
PA05
PA06
PA07
1
2
3
4
5
6
7
8
9
10
11
12
36
35
34
33
32
31
30
29
28
27
26
25
VDDIO
GND
PA25
PA24
PA23
PA22
PA21
PA20
PA19
PA18
PA17
PA16
13
14
15
16
17
18
19
20
21
22
23
24
PA08
PA09
PA10
PA11
VDDIO
GND
PB10
PB11
PA12
PA13
PA14
PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED INPUT/OUTPUT SUPPLY
RESET PIN

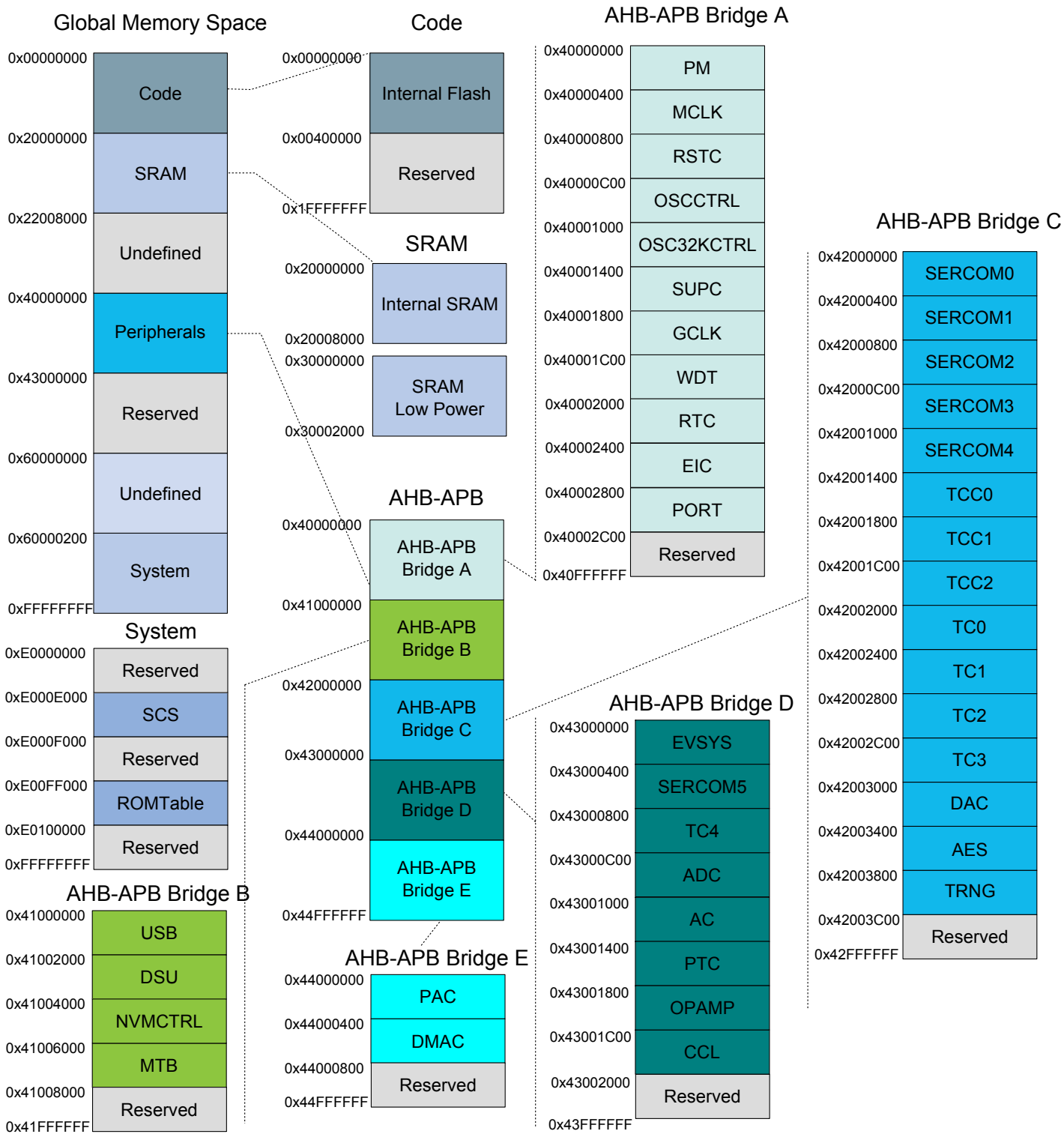
## 5.4. SAM L21E




- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED INPUT/OUTPUT SUPPLY
- RESET PIN

# 6. Product Mapping

**Figure 6-1. Atmel SAM L21 Product Mapping**



# 7. Processor and Architecture

## 7.1. Cortex M0+ Processor

The Atmel SAM L21 implements the ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

### 7.1.1. Cortex M0+ Configuration

**Table 7-1. Cortex M0+ Configuration in Atmel SAM L21**

| Features | Cortex M0+ options | Atmel SAM L21 configuration |
|---|---|---|
| Interrupts | External interrupts 0-32 | 29 |
| Data endianness | Little-endian or big-endian | Little-endian |
| SysTick timer | Present or absent | Present |
| Number of watchpoint comparators | 0, 1, 2 | 2 |
| Number of breakpoint comparators | 0, 1, 2, 3, 4 | 4 |
| Halting debug support | Present or absent | Present |
| Multiplier | Fast or small | Fast (single cycle) |
| Single-cycle I/O port | Present or absent | Present |
| Wake-up interrupt controller | Supported or not supported | Not supported |
| Vector Table Offset Register | Present or absent | Present |
| Unprivileged/Privileged support | Present or absent | Absent - All software run in privileged mode only |
| Memory Protection Unit | Not present or 8-region | Not present |
| Reset all registers | Present or absent | Absent |
| Instruction fetch width | 16-bit only or mostly 32-bit | 32-bit |

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory including Flash memory and RAM
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores

#### 7.1.1.1. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)

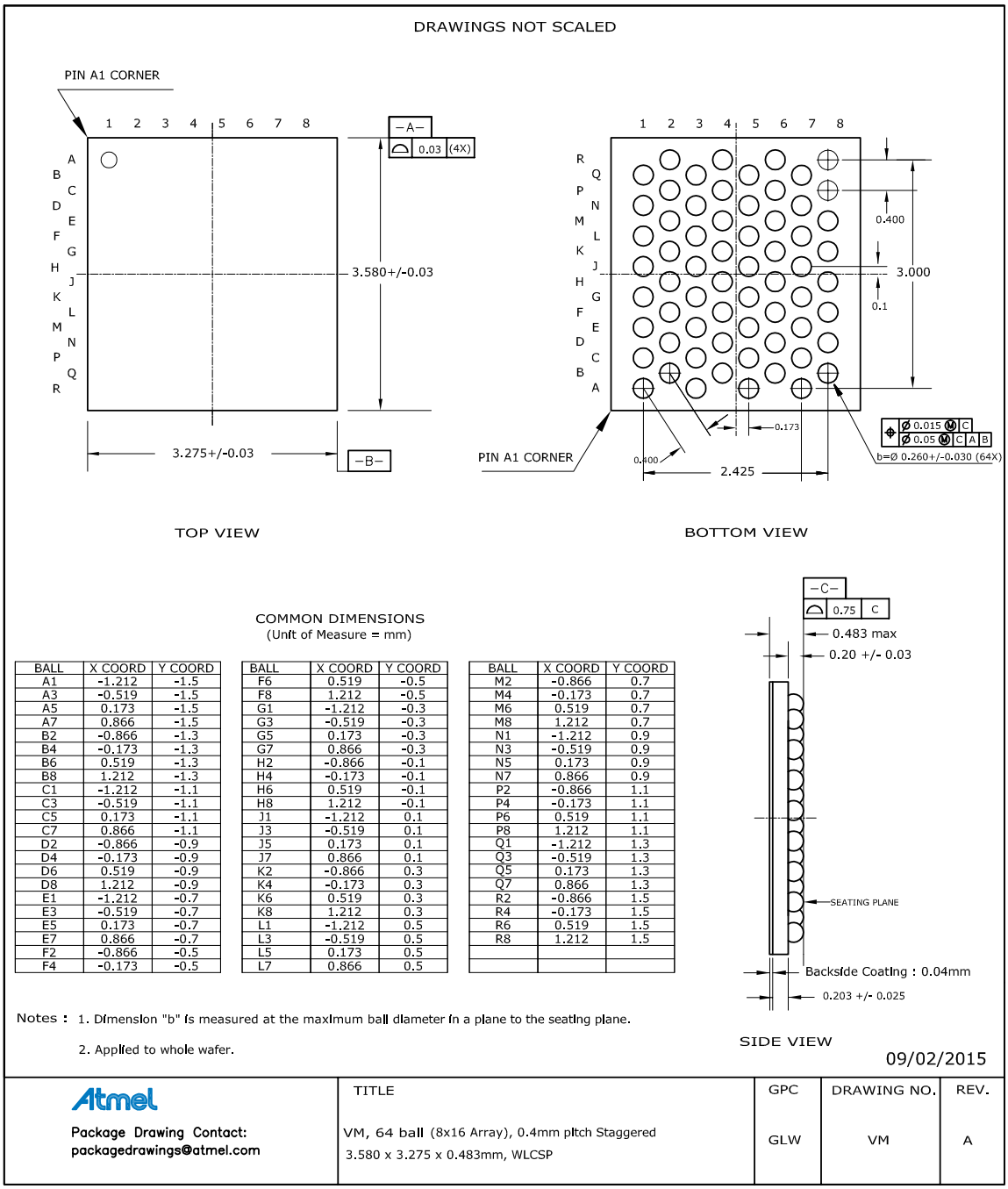
| LP SRAM Port Connection | Port ID | Connection Type | QoS | default QoS |
|---|---|---|---|---|
| H2LBRIDGEM - HS to LP bus matrix AHB to AHB bridge | 2 | Bus Matrix | 0x44000924(1), bits[1:0] | 0x2 |
| DMAC - Direct Memory Access Controller - Data Access | 1 | Bus Matrix | IP-QOSCTRL.DQOS | 0x2 |

**Note:**

1. Using 32-bit access only.

## 8.2. Package Drawings

### 8.2.1. 64-Ball WLCSP




| BALL | X COORD | Y COORD |
|---|---|---|
| A1 | -1.212 | -1.5 |
| A3 | -0.519 | -1.5 |
| A5 | 0.173 | -1.5 |
| A7 | 0.866 | -1.5 |
| B2 | -0.866 | -1.3 |
| B4 | -0.173 | -1.3 |
| B6 | 0.519 | -1.3 |
| B8 | 1.212 | -1.3 |
| C1 | -1.212 | -1.1 |
| C3 | -0.519 | -1.1 |
| C5 | 0.173 | -1.1 |
| C7 | 0.866 | -1.1 |
| D2 | -0.866 | -0.9 |
| D4 | -0.173 | -0.9 |
| D6 | 0.519 | -0.9 |
| D8 | 1.212 | -0.9 |
| E1 | -1.212 | -0.7 |
| E3 | -0.519 | -0.7 |
| E5 | 0.173 | -0.7 |
| E7 | 0.866 | -0.7 |
| F2 | -0.866 | -0.5 |
| F4 | -0.173 | -0.5 |

| BALL | X COORD | Y COORD |
|---|---|---|
| F6 | 0.519 | -0.5 |
| F8 | 1.212 | -0.5 |
| G1 | -1.212 | -0.3 |
| G3 | -0.519 | -0.3 |
| G5 | 0.173 | -0.3 |
| G7 | 0.866 | -0.3 |
| H2 | -0.866 | -0.1 |
| H4 | -0.173 | -0.1 |
| H6 | 0.519 | -0.1 |
| H8 | 1.212 | -0.1 |
| J1 | -1.212 | 0.1 |
| J3 | -0.519 | 0.1 |
| J5 | 0.173 | 0.1 |
| J7 | 0.866 | 0.1 |
| K2 | -0.866 | 0.3 |
| K4 | -0.173 | 0.3 |
| K6 | 0.519 | 0.3 |
| K8 | 1.212 | 0.3 |
| L1 | -1.212 | 0.5 |
| L3 | -0.519 | 0.5 |
| L5 | 0.173 | 0.5 |
| L7 | 0.866 | 0.5 |

| BALL | X COORD | Y COORD |
|---|---|---|
| M2 | -0.866 | 0.7 |
| M4 | -0.173 | 0.7 |
| M6 | 0.519 | 0.7 |
| M8 | 1.212 | 0.7 |
| N1 | -1.212 | 0.9 |
| N3 | -0.519 | 0.9 |
| N5 | 0.173 | 0.9 |
| N7 | 0.866 | 0.9 |
| P2 | -0.866 | 1.1 |
| P4 | -0.173 | 1.1 |
| P6 | 0.519 | 1.1 |
| P8 | 1.212 | 1.1 |
| Q1 | -1.212 | 1.3 |
| Q3 | -0.519 | 1.3 |
| Q5 | 0.173 | 1.3 |
| Q7 | 0.866 | 1.3 |
| R2 | -0.866 | 1.5 |
| R4 | -0.173 | 1.5 |
| R6 | 0.519 | 1.5 |
| R8 | 1.212 | 1.5 |

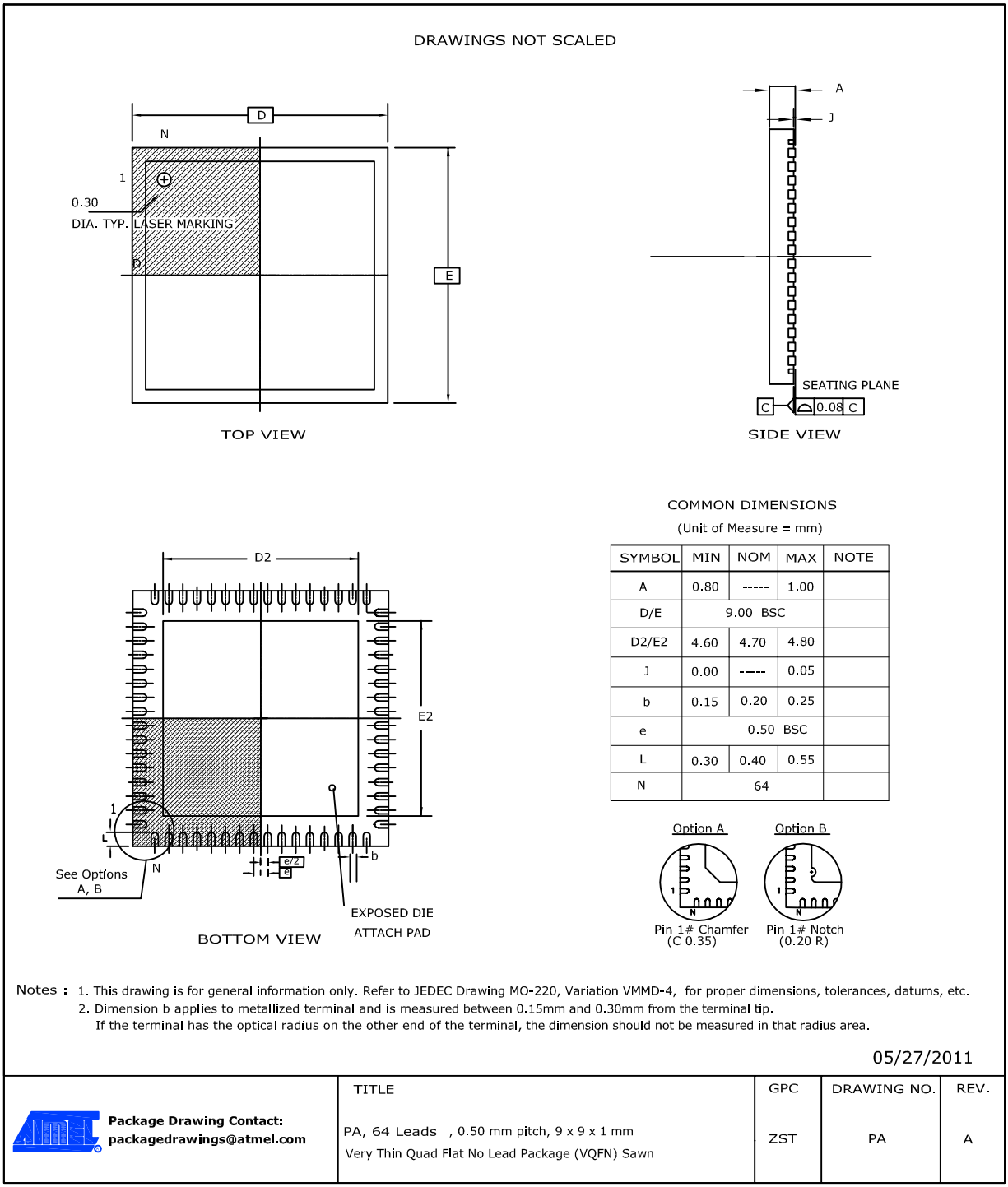
**Table 8-2. Device and Package Maximum Weight**

| | |
|---|---|
| 10 | mg |

**Table 8-3. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL1 |

### 8.2.3. 64 pin QFN




| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | ----- | 1.00 | |
| D/E | | 9.00 BSC | | |
| D2/E2 | 4.60 | 4.70 | 4.80 | |
| J | 0.00 | ----- | 0.05 | |
| b | 0.15 | 0.20 | 0.25 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.55 | |
| N | | 64 | | |

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-8. Device and Package Maximum Weight**

| | |
|---|---|
| 200 | mg |

**Table 8-9. Package Charateristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

### 8.2.6. 32 pin TQFP

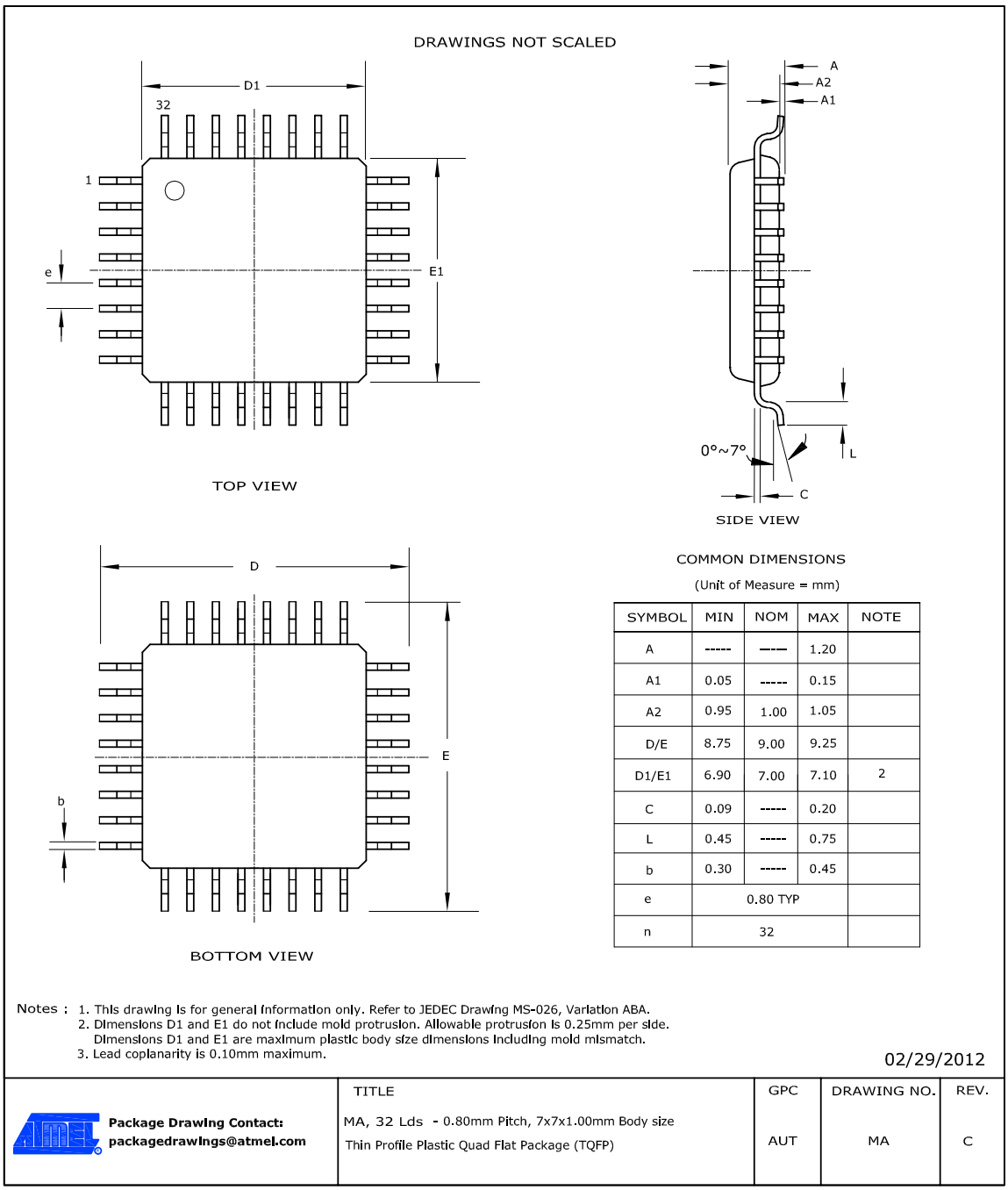



**Table 8-17. Device and Package Maximum Weight**

| | |
|---|---|
| 100 | mg |

**Table 8-18. Package Charateristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

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