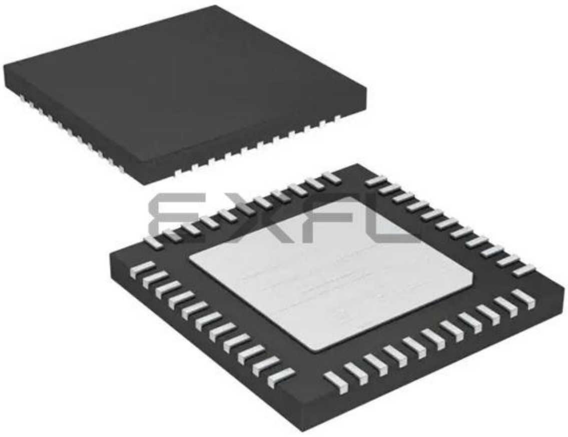
Microchip Technology - PIC18LF4480-I/ML Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4480-i-ml

TABLE 1-3: PIC18F4480/4580 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/$\overline{\text{RD}}$/AN5	8	25	25			
RE0				I/O	ST	Digital I/O.
$\overline{\text{RD}}$				I	TTL	Read control for Parallel Slave Port (see also $\overline{\text{WR}}$ and $\overline{\text{CS}}$ pins).
AN5				I	Analog	Analog Input 5.
RE1/$\overline{\text{WR}}$/AN6/C1OUT	9	26	26			
RE1				I/O	ST	Digital I/O.
$\overline{\text{WR}}$				I	TTL	Write control for Parallel Slave Port (see $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins).
AN6				I	Analog	Analog Input 6.
C1OUT				O	TTL	Comparator 1 output.
RE2/$\overline{\text{CS}}$/AN7/C2OUT	10	27	27			
RE2				I/O	ST	Digital I/O.
$\overline{\text{CS}}$				I	TTL	Chip select control for Parallel Slave Port (see related $\overline{\text{RD}}$ and $\overline{\text{WR}}$).
AN7				I	Analog	Analog Input 7.
C2OUT				O	TTL	Comparator 2 output.
RE3	—	—	—	—	—	See $\overline{\text{MCLR}}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
NC	—	13	12, 13, 33, 34	—	—	No connect.

Legend: TTL	= TTL compatible input	CMOS	= CMOS compatible input or output
ST	= Schmitt Trigger input with CMOS levels	I	= Input
O	= Output	P	= Power
I^2C	= I^2C™/SMBus input buffer		

3.7.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 3-2) controls several aspects of the device clock's operation, both in full-power operation and in power-managed modes.

The System Clock Select bits, SCS<1:0>, select the clock source. The available clock sources are the primary clock (defined by the FOSC<3:0> Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator block. The clock source changes immediately after one or more of the bits is written to, following a brief clock transition interval. The SCS bits are cleared on all forms of Reset.

The Internal Oscillator Frequency Select bits, IRCF<2:0>, select the frequency output of the internal oscillator block to drive the device clock. The choices are the INTRC source, the INTOSC source (8 MHz) or one of the frequencies derived from the INTOSC postscaler (31 kHz to 4 MHz). If the internal oscillator block is supplying the device clock, changing the states of these bits will have an immediate change on the internal oscillator's output. On device Resets, the default output frequency of the internal oscillator block is set at 1 MHz.

When an output frequency of 31 kHz is selected (IRCF<2:0> = `000`), users may choose which internal oscillator acts as the source. This is done with the INTSRC bit in the OSCTUNE register (OSCTUNE<7>). Setting this bit selects INTOSC as a 31.25 kHz clock source by enabling the divide-by-256 output of the INTOSC postscaler. Clearing INTSRC selects INTRC (nominally 31 kHz) as the clock source.

This option allows users to select the tunable and more precise INTOSC as a clock source, while maintaining power savings with a very low clock speed. Regardless of the setting of INTSRC, INTRC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor.

The OSTS, IOFS and T1RUN bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer (OST) has timed out and the primary clock is providing the device clock in primary clock modes. The IOFS bit indicates when the internal oscillator block has stabilized and is providing the device clock in RC Clock modes. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the clock or the internal oscillator block has just started and is not yet stable.

The IDLEN bit determines if the device goes into Sleep mode or one of the Idle modes when the `SLEEP` instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 4.0 "Power-Managed Modes"**.

Note 1: The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source when executing a `SLEEP` instruction will be ignored.

2: It is recommended that the Timer1 oscillator be operating and stable before executing the `SLEEP` instruction, or a very long delay may occur while the Timer1 oscillator starts.

3.7.2 OSCILLATOR TRANSITIONS

PIC18F2480/2580/4480/4580 devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 4.1.2 "Entering Power-Managed Modes"**.

4.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode where the primary clock source is not stopped; and
- the primary clock source is not any of the LP, XT, HS or HSPLL modes.

In these instances, the primary clock source either does not require an oscillator start-up delay, since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (RC, EC and INTIO Oscillator modes). However, a fixed delay of interval, TCSD, following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 4-2: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Clock Source Before Wake-up	Clock Source After Wake-up	Exit Delay	Clock Ready Status bit (OSCCON)
Primary Device Clock (PRI_IDLE mode)	LP, XT, HS	TCSD[2]	OSTS
	HSPLL		
	EC, RC		
	INTRC[1]		—
	INTOSC[3]		IOFS
T1OSC or INTRC[1]	LP, XT, HS	TOST[4]	OSTS
	HSPLL	TOST + t_{rc}[4]	
	EC, RC	TCSD[2]	
	INTRC[1]		—
	INTOSC[3]	TIOBST[5]	IOFS
INTOSC[3]	LP, XT, HS	TOST[5]	OSTS
	HSPLL	TOST + t_{rc}[4]	
	EC, RC	TCSD[2]	
	INTRC[1]		—
	INTOSC[3]	None	IOFS
None (Sleep mode)	LP, XT, HS	TOST[4]	OSTS
	HSPLL	TOST + t_{rc}[4]	
	EC, RC	TCSD[2]	
	INTRC[1]		—
	INTOSC[3]	TIOBST[5]	IOFS

Note 1: In this instance, refers specifically to the 31 kHz INTRC clock source.

2: TCSD (parameter 38) is a required delay when waking from Sleep and all Idle modes and runs concurrently with any other required delays (see **Section 4.4 "Idle Modes"**).

3: Includes both the INTOSC 8 MHz source and postscaler derived frequencies.

4: TOST is the Oscillator Start-up Timer (parameter 32). t_{rc} is the PLL Lock-out Timer (parameter F12); it is also designated as TPLL.

5: Execution continues during TIOBST (parameter 39), the INTOSC stabilization period.

TABLE 5-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices				Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
B4D4[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4D3[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4D2[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4D1[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4D0[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4DLC[6]	2480	2580	4480	4580	-xxx xxxx	-uuu uuuu	-uuu uuuu
B4EIDL[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4EIDH[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4SIDL[6]	2480	2580	4480	4580	xxxx x-xx	uuuu u-uu	uuuu u-uu
B4SIDH[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B4CON[6]	2480	2580	4480	4580	0000 0000	0000 0000	uuuu uuuu
B3D7[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D6[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D5[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D4[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D3[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D2[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D1[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3D0[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3DLC[6]	2480	2580	4480	4580	-xxx xxxx	-uuu uuuu	-uuu uuuu
B3EIDL[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3EIDH[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3SIDL[6]	2480	2580	4480	4580	xxxx x-xx	uuuu u-uu	uuuu u-uu
B3SIDH[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B3CON[6]	2480	2580	4480	4580	0000 0000	0000 0000	uuuu uuuu
B2D7[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B2D6[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B2D5[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B2D4[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B2D3[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu
B2D2[6]	2480	2580	4480	4580	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 5-3 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: This register reads all '0's until ECAN™ technology is set up in Mode 1 or Mode 2.

10.5 RCON Register

The RCON register contains flag bits which are used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the IPEN bit which enables interrupt priorities.

REGISTER 10-13: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1(1)	U-0	R/W-1	R-1	R-1	R/W-0(2)	R/W-0
IPEN	SBOREN	—	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 **SBOREN:** BOR Software Enable bit(1)
For details of bit operation, see Register 5-1.

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **$\overline{\text{RI}}$:** RESET Instruction Flag bit
For details of bit operation, see Register 5-1.

bit 3 **$\overline{\text{TO}}$:** Watchdog Time-out Flag bit
For details of bit operation, see Register 5-1.

bit 2 **$\overline{\text{PD}}$:** Power-Down Detection Flag bit
For details of bit operation, see Register 5-1.

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit(2)
For details of bit operation, see Register 5-1.

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
For details of bit operation, see Register 5-1.

Note 1: If SBOREN is enabled, its Reset state is ‘1’; otherwise, it is ‘0’.

2: The actual Reset value of $\overline{\text{POR}}$ is determined by the type of device Reset. See Register 5-1 for additional information.

TABLE 11-7: PORTD I/O SUMMARY

Pin Name	Function	I/O	TRIS	Buffer	Description
RD0/PSP0/ C1IN+	RD0	OUT	0	DIG	LATD<0> data output.
		IN	1	ST	PORTD<0> data input.
	PSP0	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<0> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<0> control when enabled).
	C1IN+	IN	1	ANA	Comparator 1 Positive Input B. Default on POR. This analog input overrides the digital input (read as clear – low level).
RD1/PSP1/ C1IN-	RD1	OUT	0	DIG	LATD<1> data output.
		IN	1	ST	PORTD<1> data input.
	PSP1	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<1> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<1> control when enabled).
	C1IN-	IN	1	ANA	Comparator 1 negative input. Default on POR. This analog input overrides the digital input (read as clear – low level).
RD2/PSP2/ C2IN+	RD2	OUT	0	DIG	LATD<2> data output.
		IN	1	ST	PORTD<2> data input.
	PSP2	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<2> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<2> control when enabled).
	C2IN+	IN	1	ANA	Comparator 2 positive input. Default on POR. This analog input overrides the digital input (read as clear – low level).
RD3/PSP3/ C2IN-	RD3	OUT	0	DIG	LATD<3> data output.
		IN	1	ST	PORTD<3> data input.
	PSP3	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<3> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<3> control when enabled).
	C2IN-	IN	1	ANA	Comparator 2 negative input. Default input on POR. This analog input overrides the digital input (read as clear – low level).
RD4/PSP4/ ECCP1/P1A	RD4	OUT	0	DIG	LATD<4> data output.
		IN	1	ST	PORTD<4> data input.
	PSP4	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<4> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<4> control when enabled).
	ECCP1	OUT	0	DIG	ECCP1 compare output.
		IN	1	ST	ECCP1 capture input.
	P1A	OUT	0	DIG	ECCP1 Enhanced PWM output, Channel A.
RD5/PSP5/ P1B	RD5	OUT	0	DIG	LATD<5> data output.
		IN	1	ST	PORTD<5> data input.
	PSP5	OUT	X	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<5> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<5> control when enabled).
	P1B	OUT	0	DIG	ECCP1 Enhanced PWM output, Channel B.
RD6/PSP6/ P1C	RD6	OUT	0	DIG	LATD<6> data output.
		IN	1	ST	PORTD<6> data input.
	PSP6	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<6> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<6> control when enabled).
	P1C	OUT	0	DIG	ECCP1 Enhanced PWM output, Channel C.
RD7/PSP7/ P1D	RD7	OUT	0	DIG	LATD<7> data output.
		IN	1	ST	PORTD<7> data input.
	PSP7	OUT	x	DIG	Parallel Slave Port (PSP) data output (overrides the TRIS<7> control when enabled).
		IN	x	TTL	Parallel Slave Port (PSP) data input (overrides the TRIS<7> control when enabled).
	P1D	OUT	0	DIG	ECCP1 Enhanced PWM output, channel D.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input

NOTES:

14.0 TIMER2 MODULE

The Timer2 module timer incorporates the following features:

- 8-Bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSP module

The module is controlled through the T2CON register (Register 14-1), which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 14-1.

14.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (FOSC/4). A 2-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options; these are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>). The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 14.2 "Timer2 Interrupt"**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 14-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **T2OUTPS<3:0>**: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON**: Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>**: Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

NOTES:

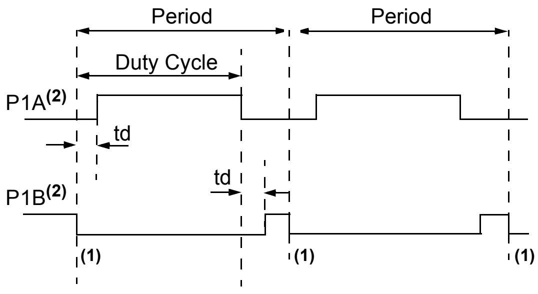
17.4.4 HALF-BRIDGE MODE

In the Half-Bridge Output mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the P1A pin, while the complementary PWM output signal is output on the P1B pin (Figure 17-4). This mode can be used for half-bridge applications, as shown in Figure 17-5, or for full-bridge applications where four power switches are being modulated with two PWM signals.

In Half-Bridge Output mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of bits, PDC<6:0>, sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 17.4.6 "Programmable Dead-Band Delay"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORTD<4> and PORTD<5> data latches, the TRISD<4> and TRISD<5> bits must be cleared to configure P1A and P1B as outputs.

FIGURE 17-4: HALF-BRIDGE PWM OUTPUT

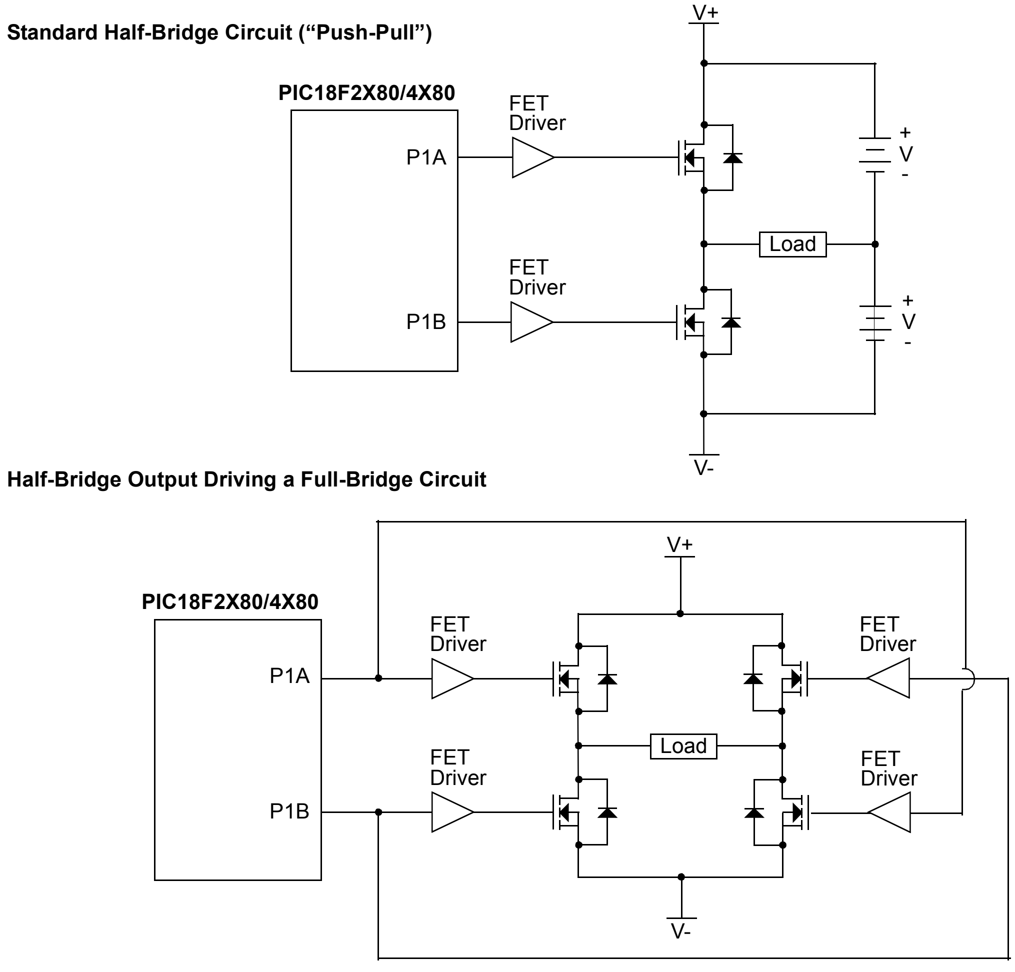


td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.

FIGURE 17-5: EXAMPLES OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



18.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit (SSPCON1<4>).

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from Sleep.

18.3.7 SLAVE SELECT SYNCHRONIZATION

The $\overline{SS}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the $\overline{SS}$ pin to function as an input. The data latch must be high. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When the SPI is in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = `0100`), the SPI module will reset if the $\overline{SS}$ pin is set to V_{DD}.
2:	If the SPI is used in Slave mode with CKE set, then the $\overline{SS}$ pin control must be enabled.

When the SPI module resets, the bit counter is forced to '`0`'. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 18-4: SLAVE SYNCHRONIZATION WAVEFORM

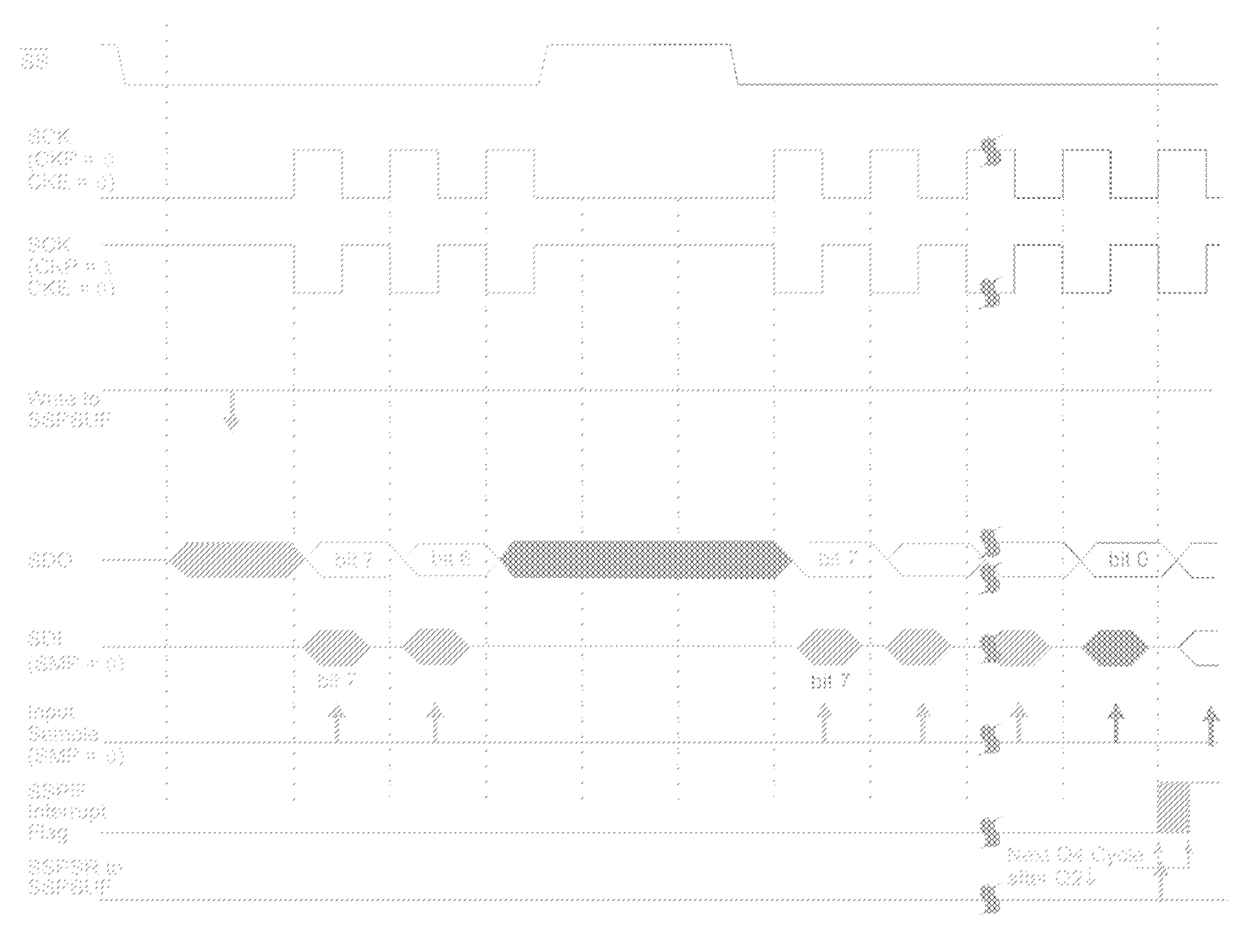
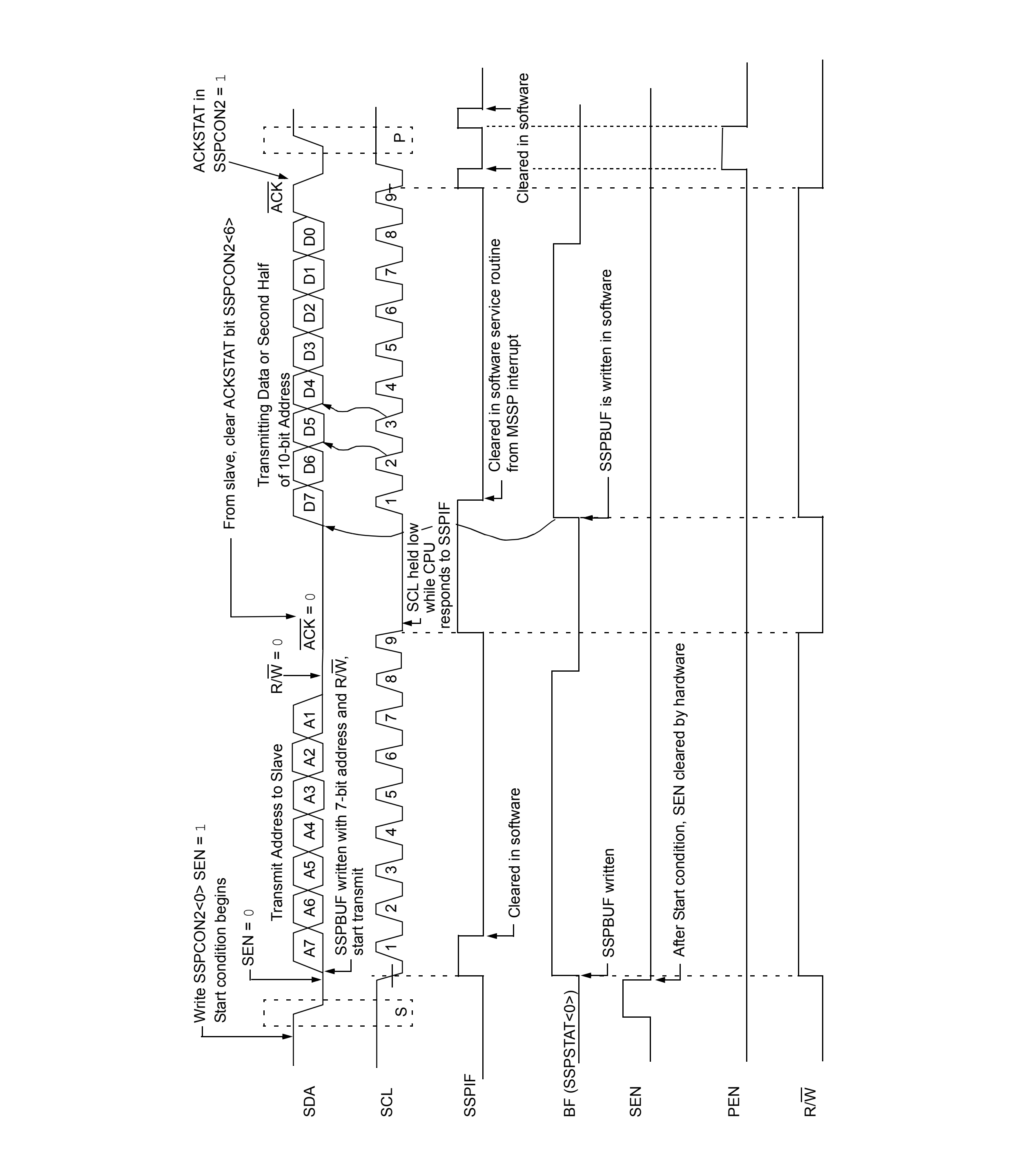


FIGURE 18-21: I²C™ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



18.4.17.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL is sampled low at the beginning of the Start condition (Figure 18-26).

b) SCL is sampled low before SDA is asserted low (Figure 18-27).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

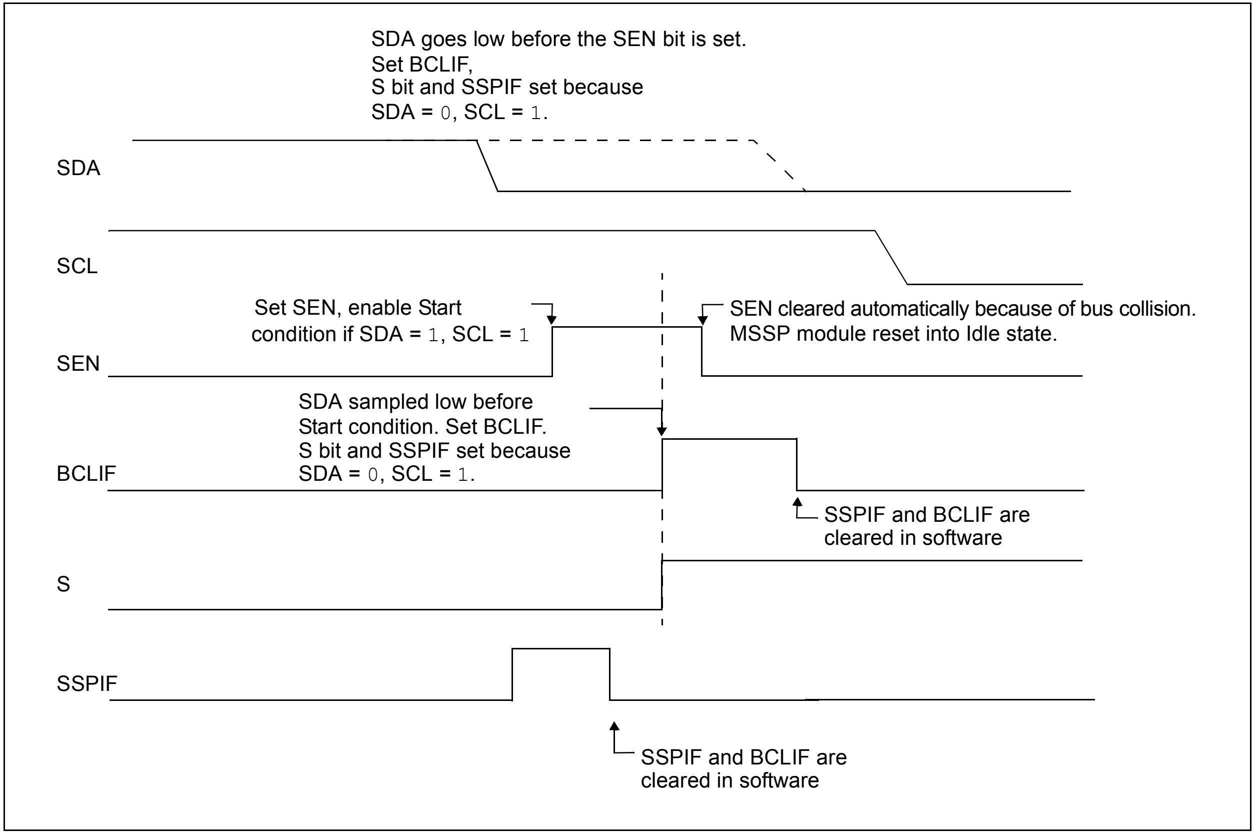
- the Start condition is aborted,
- the BCLIF flag is set; and
- the MSSP module is reset to its Idle state (Figure 18-26)

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data ‘1’ during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 18-28). If, however, a ‘1’ is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to 0 and during this time, if the SCL pins are sampled as ‘0’, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 18-26: BUS COLLISION DURING START CONDITION (SDA ONLY)


SDA goes low before the SEN bit is set.
Set BCLIF,
S bit and SSPIF set because
SDA = 0, SCL = 1.
SDA
SCL
Set SEN, enable Start
condition if SDA = 1, SCL = 1
SEN cleared automatically because of bus collision.
MSSP module reset into Idle state.
SEN
SDA sampled low before
Start condition. Set BCLIF.
S bit and SSPIF set because
SDA = 0, SCL = 1.
BCLIF
SSPIF and BCLIF are
cleared in software
S
SSPIF
SSPIF and BCLIF are
cleared in software

19.4.2 EUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep or any Idle mode and bit, SREN, which is a “don’t care” in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep or any Idle mode, then a word may be received while in this low-power mode. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the chip from the low-power mode. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
2. If interrupts are desired, set enable bit, RCIE.
3. If 9-bit reception is desired, set bit, RX9.
4. To enable reception, set enable bit, CREN.
5. Flag bit, RCIF, will be set when reception is complete. An interrupt will be generated if enable bit, RCIE, was set.
6. Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG register.
8. If any error occurred, clear the error by clearing bit, CREN.
9. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 19-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP[1]	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	57
RCREG	EUSART Receive Register								57
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	57
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	57
SPBRGH	EUSART Baud Rate Generator Register High Byte								57
SPBRG	EUSART Baud Rate Generator Register Low Byte								57

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used for synchronous slave reception.

Note 1: Reserved in PIC18F2X80 devices; always maintain these bits clear.

EXAMPLE 24-1: CHANGING TO CONFIGURATION MODE

```
    ; Request Configuration mode.
    MOVLW   B’10000000’                   ; Set to Configuration Mode.
    MOVWF   CANCON
    ; A request to switch to Configuration mode may not be immediately honored.
    ; Module will wait for CAN bus to be idle before switching to Configuration Mode.
    ; Request for other modes such as Loopback, Disable etc. may be honored immediately.
    ; It is always good practice to wait and verify before continuing.
ConfigWait:
    MOVF    CANSTAT, W                    ; Read current mode state.
    ANDLW   B’10000000’                   ; Interested in OPMODE bits only.
    TSTFSZ  WREG                          ; Is it Configuration mode yet?
    BRA     ConfigWait                    ; No. Continue to wait...
    ; Module is in Configuration mode now.
    ; Modify configuration registers as required.
    ; Switch back to Normal mode to be able to communicate.
```

EXAMPLE 24-2: WIN AND ICODE BITS USAGE IN INTERRUPT SERVICE ROUTINE TO ACCESS TX/RX BUFFERS

```
    ; Save application required context.
    ; Poll interrupt flags and determine source of interrupt
    ; This was found to be CAN interrupt
    ; TempCANCON and TempCANSTAT are variables defined in Access Bank low
    MOVFF   CANCON, TempCANCON            ; Save CANCON.WIN bits
                                          ; This is required to prevent CANCON
                                          ; from corrupting CAN buffer access
                                          ; in-progress while this interrupt
                                          ; occurred
    MOVFF   CANSTAT, TempCANSTAT          ; Save CANSTAT register
                                          ; This is required to make sure that
                                          ; we use same CANSTAT value rather
                                          ; than one changed by another CAN
                                          ; interrupt.
    MOVF    TempCANSTAT, W                ; Retrieve ICODE bits
    ANDLW   B’00001110’
    ADDWF   PCL, F                        ; Perform computed GOTO
                                          ; to corresponding interrupt cause
    BRA     NoInterrupt                   ; 000 = No interrupt
    BRA     ErrorInterrupt                ; 001 = Error interrupt
    BRA     TXB2Interrupt                 ; 010 = TXB2 interrupt
    BRA     TXB1Interrupt                 ; 011 = TXB1 interrupt
    BRA     TXB0Interrupt                 ; 100 = TXB0 interrupt
    BRA     RXB1Interrupt                 ; 101 = RXB1 interrupt
    BRA     RXB0Interrupt                 ; 110 = RXB0 interrupt
                                          ; 111 = Wake-up on interrupt
WakeupInterrupt
    BCF     PIR3, WAKIF                   ; Clear the interrupt flag
    ;
    ; User code to handle wake-up procedure
    ;
    ;
    ; Continue checking for other interrupt source or return from here
    …
NoInterrupt
    …                                     ; PC should never vector here. User may
                                          ; place a trap such as infinite loop or pin/port
                                          ; indication to catch this error.
```

24.2.6 CAN INTERRUPT REGISTERS

The registers in this section are the same as described in **Section 10.0 “Interrupts”**. They are duplicated here for convenience.

REGISTER 24-56: PIR3: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 3

Mode 0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IRXIF	WAKIF	ERRIF	TXB2IF	TXB1IF[1]	TXB0IF[1]	RXB1IF	RXB0IF

Mode 1,2	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IRXIF	WAKIF	ERRIF	TXBnIF	TXB1IF[1]	TXB0IF[1]	RXBnIF	FIFOWMIF
	bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IRXIF:** CAN Bus Error Message Received Interrupt Flag bit
1 = An invalid message has occurred on the CAN bus
0 = No invalid message on CAN bus

bit 6 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = Activity on CAN bus has occurred
0 = No activity on CAN bus

bit 5 **ERRIF:** CAN Module Error Interrupt Flag bit
1 = An error has occurred in the CAN module (multiple sources; refer to **Section 24.15.6 “Error Interrupt”**)
0 = No CAN module errors

bit 4 When CAN is in Mode 0:
TXB2IF: CAN Transmit Buffer 2 Interrupt Flag bit
1 = Transmit Buffer 2 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 2 has not completed transmission of a message
When CAN is in Mode 1 or 2:
TXBnIF: Any Transmit Buffer Interrupt Flag bit
1 = One or more transmit buffers have completed transmission of a message and may be reloaded
0 = No transmit buffer is ready for reload

bit 3 **TXB1IF:** CAN Transmit Buffer 1 Interrupt Flag bit[1]
1 = Transmit Buffer 1 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 1 has not completed transmission of a message

bit 2 **TXB0IF:** CAN Transmit Buffer 0 Interrupt Flag bit[1]
1 = Transmit Buffer 0 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 0 has not completed transmission of a message

bit 1 When CAN is in Mode 0:
RXB1IF: CAN Receive Buffer 1 Interrupt Flag bit
1 = Receive Buffer 1 has received a new message
0 = Receive Buffer 1 has not received a new message
When CAN is in Mode 1 or 2:
RXBnIF: Any Receive Buffer Interrupt Flag bit
1 = One or more receive buffers has received a new message
0 = No receive buffer has received a new message

bit 0 When CAN is in Mode 0:
RXB0IF: CAN Receive Buffer 0 Interrupt Flag bit
1 = Receive Buffer 0 has received a new message
0 = Receive Buffer 0 has not received a new message
When CAN is in Mode 1:
Unimplemented: Read as ‘0’
When CAN is in Mode 2:
FIFOWMIF: FIFO Watermark Interrupt Flag bit
1 = FIFO high watermark is reached
0 = FIFO high watermark is not reached

Note 1: In CAN Mode 1 and 2, these bits are forced to ‘0’.

MOVLW Move Literal to W

Syntax:	MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → W
Status Affected:	None
Encoding:	`0000` `1110` `kkkk` `kkkk`
Description:	The eight-bit literal ‘k’ is loaded into W.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal ‘k’	Process Data	Write to W

Example: `MOVLW 5Ah`

After Instruction

W	=	5Ah

MOVWF Move W to f

Syntax:	MOVWF f {,a}
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]
Operation:	(W) → f
Status Affected:	None
Encoding:	`0110` `111a` `ffff` `ffff`
Description:	Move data from W to register ‘f’. Location ‘f’ can be anywhere in the 256-byte bank. If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 26.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write register ‘f’

Example: `MOVWF REG, 0`

Before Instruction

W	=	4Fh
REG	=	FFh

After Instruction

W	=	4Fh
REG	=	4Fh

TBLWT Table Write

Syntax: TBLWT (*; *+; *-; +*)

Operands: None

Operation:
if TBLWT*,
(TABLAT) → Holding Register,
TBLPTR – No Change;
if TBLWT*+,
(TABLAT) → Holding Register,
(TBLPTR) + 1 → TBLPTR;
if TBLWT*-,
(TABLAT) → Holding Register,
(TBLPTR) – 1 → TBLPTR;
if TBLWT+*,
(TBLPTR) + 1 → TBLPTR,
(TABLAT) → Holding Register;

Status Affected: None

Encoding:

`0000`	`0000`	`0000`	`11nn`
			`nn=0 *`
			`=1 *+`
			`=2 *-`
			`=3 +*`

Description: This instruction uses the 3 LSBs of the TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to **Section 7.0 “Flash Program Memory”** for additional details on programming Flash memory.)

The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-MBtye address range. The LSb of the TBLPTR selects which byte of the program memory location to access.

TBLPTR[0] = `0`: Least Significant Byte of Program Memory Word
TBLPTR[0] = `1`: Most Significant Byte of Program Memory Word

The `TBLWT` instruction can modify the value of TBLPTR as follows:

- no change
- post-increment
- post-decrement
- pre-increment

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read TABLAT)	No operation	No operation (Write to Holding Register)

TBLWT Table Write (Continued)

Example 1: `TBLWT *+;`

Before Instruction

TABLAT	=	55h
TBLPTR	=	00A356h
HOLDING REGISTER (00A356h)	=	FFh

After Instructions (table write completion)

TABLAT	=	55h
TBLPTR	=	00A357h
HOLDING REGISTER (00A356h)	=	55h

Example 2: `TBLWT +*;`

Before Instruction

TABLAT	=	34h
TBLPTR	=	01389Ah
HOLDING REGISTER (01389Ah)	=	FFh
HOLDING REGISTER (01389Bh)	=	FFh

After Instruction (table write completion)

TABLAT	=	34h
TBLPTR	=	01389Bh
HOLDING REGISTER (01389Ah)	=	FFh
HOLDING REGISTER (01389Bh)	=	34h

CALLW Subroutine Call Using WREG

Syntax:	CALLW
Operands:	None
Operation:	(PC + 2) → TOS, (W) → PCL, (PCLATH) → PCH, (PCLATU) → PCU
Status Affected:	None
Encoding:	0000 0000 0001 0100
Description	First, the return address (PC + 2) is pushed onto the return stack. Next, the contents of W are written to PCL; the existing value is discarded. Then, the contents of PCLATH and PCLATU are latched into PCH and PCU, respectively. The second cycle is executed as a `NOP` instruction while the new next instruction is fetched. Unlike `CALL`, there is no option to update W, STATUS or BSR.
Words:	1
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read WREG	Push PC to stack	No operation
No operation	No operation	No operation	No operation

Example: `HERE CALLW`

```
Before Instruction
    PC      =   address (HERE)
    PCLATH  =   10h
    PCLATU  =   00h
    W       =   06h
After Instruction
    PC      =   001006h
    TOS     =   address (HERE + 2)
    PCLATH  =   10h
    PCLATU  =   00h
    W       =   06h
```

MOVSF Move Indexed to f

Syntax:	MOVSF $[z_s]$, f_d
Operands:	$0 \le z_s \le 127$ $0 \le f_d \le 4095$
Operation:	$((\text{FSR2}) + z_s) \rightarrow f_d$
Status Affected:	None

Encoding:				
1st word (source)	1110	1011	0zzz	zzzz_s
2nd word (destin.)	1111	ffff	ffff	ffff_d

Description:	The contents of the source register are moved to destination register 'f_d'. The actual address of the source register is determined by adding the 7-bit literal offset 'z_s' in the first word to the value of FSR2. The address of the destination register is specified by the 12-bit literal 'f_d' in the second word. Both addresses can be anywhere in the 4096-byte data space (000h to FFFh). The `MOVSF` instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register. If the resultant source address points to an indirect addressing register, the value returned will be 00h.
Words:	2
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Determine source addr	Determine source addr	Read source reg
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: `MOVSF [05h], REG2`

```
Before Instruction
    FSR2        =   80h
    Contents
    of 85h      =   33h
    REG2        =   11h
After Instruction
    FSR2        =   80h
    Contents
    of 85h      =   33h
    REG2        =   33h
```

28.3 DC Characteristics: PIC18F2480/2580/4480/4580 (Industrial) PIC18LF2480/2580/4480/4580 (Industrial) (Continued)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
D080		I/O Ports	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	VOH	**Output High Voltage**[3]				
D090		I/O Ports	VDD – 0.7	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	VDD – 0.7	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
		Capacitive Loading Specs on Output Pins				
D100	COSC2	OSC2 Pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O Pins and OSC2 (in RC mode)	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCL, SDA	—	400	pF	I²C™ Specification

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.