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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4480-i-pt

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4.0 POWER-MANAGED MODES

PIC18F2480/2580/4480/4580 devices offer a total of seven operating modes for more efficient power management. These modes provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery-powered devices).

There are three categories of power-managed modes:

- Run modes
- Idle modes
- Sleep mode

These categories define which portions of the device are clocked, and sometimes, what speed. The Run and Idle modes may use any of the three available clock sources (primary, secondary or internal oscillator block); the Sleep mode does not use a clock source.

The power-managed modes include several power-saving features offered on previous PIC[®] devices. One is the clock switching feature, offered in other PIC18 devices, allowing the controller to use the Timer1 oscillator in place of the primary oscillator. Also included is the Sleep mode, offered by all PIC devices, where all device clocks are stopped.

4.1 Selecting Power-Managed Modes

Selecting a power-managed mode requires two decisions: if the CPU is to be clocked or not and the selection of a clock source. The IDLEN bit (OSCCON<7>) controls CPU clocking, while the SCS<1:0> bits (OSCCON<1:0>) select the clock source. The individual modes, bit settings, clock sources and affected modules are summarized in Table 4-1.

4.1.1 CLOCK SOURCES

The SCS<1:0> bits allow the selection of one of three clock sources for power-managed modes. They are:

- The primary clock, as defined by the FOSC<3:0> Configuration bits
- The secondary clock (the Timer1 oscillator)
- The internal oscillator block (for RC modes)

4.1.2 ENTERING POWER-MANAGED MODES

Switching from one power-managed mode to another begins by loading the OSCCON register. The SCS<1:0> bits select the clock source and determine which Run or Idle mode is to be used. Changing these bits causes an immediate switch to the new clock source, assuming that it is running. The switch may also be subject to clock transition delays. These are discussed in **Section 4.1.3 "Clock Transitions and Status Indicators"** and subsequent sections.

Entry to the power-managed Idle or Sleep modes is triggered by the execution of a SLEEP instruction. The actual mode that results depends on the status of the IDLEN bit.

Depending on the current mode and the mode being switched to, a change to a power-managed mode does not always require setting all of these bits. Many transitions may be done by changing the oscillator select bits, or changing the IDLEN bit, prior to issuing a SLEEP instruction. If the IDLEN bit is already configured correctly, it may only be necessary to perform a SLEEP instruction to switch to the desired mode.

			ODLO			
Mada	OSCC	ON<7,1:0>	Module Clocking			
wode	IDLEN ⁽¹⁾	SCS<1:0>	CPU	Peripherals		
Sleep	0	N/A	Off	Off	None – All clocks are disabled	
PRI_RUN	N/A	00	Clocked	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC, INTRC ⁽²⁾ : This is the normal full-power execution mode.	
SEC_RUN	N/A	01	Clocked	Clocked	Secondary – Timer1 Oscillator	
RC_RUN	N/A	lx	Clocked	Clocked	Internal Oscillator Block ⁽²⁾	
PRI_IDLE	1	00	Off	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC	
SEC_IDLE	1	01	Off	Clocked	Secondary – Timer1 Oscillator	
RC_IDLE	1	1x	Off	Clocked	Internal Oscillator Block ⁽²⁾	

TABLE 4-1: POWER-MANAGED MODES

Note 1: IDLEN reflects its value when the **SLEEP** instruction is executed.

2: Includes INTOSC and INTOSC postscaler, as well as the INTRC source.

4.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. The INTOSC multiplexer may be used to select a higher clock frequency, by modifying the IRCF bits, before executing the SLEEP instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value or the INTSRC bit is set, the INTOSC output is enabled. The IOFS bit becomes set, after the INTOSC output becomes stable, after an interval of TIOBST (parameter 39, Table 28-10). Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value, or INTSRC was set before the SLEEP instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the IOFS bit will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TCSD following the wake event, the CPU begins executing code being clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

4.5 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see Section 4.2 "Run Modes", Section 4.3 "Sleep Mode" and Section 4.4 "Idle Modes").

4.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode or the Sleep mode to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see Section 10.0 "Interrupts").

A fixed delay of interval, TCSD, following the wake event is required when leaving Sleep and Idle modes. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

4.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see Section 4.2 "Run Modes" and Section 4.3 "Sleep Mode"). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see Section 25.2 "Watchdog Timer (WDT)").

The WDT timer and postscaler are cleared by executing a SLEEP or CLRWDT instruction, the loss of a currently selected clock source (if the Fail-Safe Clock Monitor is enabled) and modifying the IRCF bits in the OSCCON register if the internal oscillator block is the device clock source.

4.5.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code. If the internal oscillator block is the new clock source, the IOFS bit is set instead.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator if the new clock source is the primary clock. Exit delays are summarized in Table 4-2.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see **Section 25.3 "Two-Speed Start-up"**) or Fail-Safe Clock Monitor (see **Section 25.4 "Fail-Safe Clock Monitor**") is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTOSC multiplexer driven by the internal oscillator block. Execution is clocked by the internal oscillator block until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

5.6 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on a Power-on Reset and unchanged by all other Resets. The other registers are forced to a "Reset state" depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, RI, TO, PD, POR and BOR, are set or cleared differently in different Reset situations, as indicated in Table 5-3. These bits are used in software to determine the nature of the Reset.

Table 5-4 describes the Reset states for all of the Special Function Registers. These are categorized by Power-on and Brown-out Resets, Master Clear and WDT Resets and WDT wake-ups.

TABLE 5-3:STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR
RCON REGISTER

Condition	Program	RCON Register						STKPTR Register	
Condition	Counter ⁽¹⁾	SBOREN	RI	то	PD	POR	BOR	STKFUL	STKUNF
Power-on Reset	0000h	1	1	1	1	0	0	0	0
RESET Instruction	0000h	u (2)	0	u	u	u	u	u	u
Brown-out Reset	0000h	u (2)	1	1	1	u	0	u	u
MCLR Reset during Power-Managed Run modes	0000h	_ບ (2)	u	1	u	u	u	u	u
MCLR Reset during Power-Managed Idle modes and Sleep mode	0000h	ս (2)	u	1	0	u	u	u	u
WDT Time-out during Full Power or Power-Managed Run modes	0000h	u (2)	u	0	u	u	u	u	u
MCLR Reset during Full-Power 000 execution		_ບ (2)	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)	0000h	u (2)	u	u	u	u	u	1	u
Stack Underflow Reset (STVREN = 1)	Stack Underflow Reset 0000h (STVREN = 1)		u	u	u	u	u	u	1
Stack Underflow Error (not an 0000h actual Reset, STVREN = 0)		u (2)	u	u	u	u	u	u	1
WDT Time-out during Power-Managed Idle or Sleep modes	PC + 2	ս (2)	u	0	0	u	u	u	u
Interrupt Exit from Power-Managed modes	PC + 2	u (2)	u	u	0	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (008h or 0018h).

2: Reset state is '1' for POR and unchanged for all other Resets when software BOR is enabled (BOREN<1:0> Configuration bits = 01 and SBOREN = 1); otherwise, the Reset state is '0'.

Register	Applicable Devices		Power-on Reset Brown-out Rese	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	, Wake-up via WDT or Interrupt		
RXF3SIDL	2480	2580	4480	4580	xxx- x-xx	uuu- u-uu	uuu- u-uu
RXF3SIDH	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
RXF2EIDL	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
RXF2EIDH	2480	2580	4480	4580	XXXX XXXX	սսսս սսսս	սսսս սսսս
RXF2SIDL	2480	2580	4480	4580	xxx- x-xx	uuu- u-uu	uuu- u-uu
RXF2SIDH	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	սսսս սսսս
RXF1EIDL	2480	2580	4480	4580	XXXX XXXX	սսսս սսսս	սսսս սսսս
RXF1EIDH	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
RXF1SIDL	2480	2580	4480	4580	xxx- x-xx	uuu- u-uu	uuu- u-uu
RXF1SIDH	2480	2580	4480	4580	XXXX XXXX	սսսս սսսս	սսսս սսսս
RXF0EIDL	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
RXF0EIDH	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
RXF0SIDL	2480	2580	4480	4580	xxx- x-xx	uuu- u-uu	uuu- u-uu
RXF0SIDH	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D7 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D6 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D5 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D4 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D3 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D2 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	นนนน นนนน
B5D1 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	սսսս սսսս
B5D0 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	นนนน นนนน	սսսս սսսս
B5DLC ⁽⁶⁾	2480	2580	4480	4580	-xxx xxxx	-uuu uuuu	-uuu uuuu
B5EIDL ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	uuuu uuuu	սսսս սսսս
B5EIDH ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	uuuu uuuu	սսսս սսսս
B5SIDL ⁽⁶⁾	2480	2580	4480	4580	XXXX X-XX	uuuu u-uu	uuuu u-uu
B5SIDH ⁽⁶⁾	2480	2580	4480	4580	XXXX X-XX	uuuu u-uu	uuuu u-uu
B5CON ⁽⁶⁾	2480	2580	4480	4580	0000 0000	0000 0000	นนนน นนนน
B4D7 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	uuuu uuuu	սսսս սսսս
B4D6 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	սսսս սսսս	սսսս սսսս
B4D5 ⁽⁶⁾	2480	2580	4480	4580	XXXX XXXX	uuuu uuuu	սսսս սսսս

TABLE 5-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 5-3 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: This register reads all '0's until ECAN[™] technology is set up in Mode 1 or Mode 2.

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
TOSU	Top-of-Stack Upper Byte (TOS<20:16>)									55, 68
TOSH	Top-of-Stack H	ligh Byte (TOS	6<15:8>)						0000 0000	55, 68
TOSL	Top-of-Stack L	ow Byte (TOS	<7:0>)						0000 0000	55, 68
STKPTR	STKFUL	STKFUL STKUNF — Return Stack Pointer							00-0 0000	55, 69
PCLATU	— — bit 21 ⁽¹⁾ Holding Register for PC<20:16>								0 0000	55, 68
PCLATH	Holding Regis	ter for PC<15:	8>						0000 0000	55, 68
PCL	PC Low Byte (PC<7:0>)								0000 0000	55, 68
TBLPTRU	—	_	bit 21	Program Me	mory Table Poi	nter Upper Byte (TBLPTR<20:10	S>)	00 0000	55, 109
TBLPTRH	Program Merr	ory Table Poir	iter High Byte	(TBLPTR<15	:8>)				0000 0000	55, 109
TBLPTRL	Program Merr	nory Table Poir	ter Low Byte	(TBLPTR<7:0	>)				0000 0000	55, 109
TABLAT	Program Merr	ory Table Latc	h						0000 0000	55, 109
PRODH	Product Regis	ter High Byte							XXXX XXXX	55, 117
PRODL	Product Regis	ter Low Byte							XXXX XXXX	55, 117
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	55, 121
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP	1111 -1-1	55, 122
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	_	INT2IF	INT1IF	11-0 0-00	55, 123
INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)							N/A	55, 96	
POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)							ster)	N/A	55, 97
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)						N/A	55, 97		
PREINC0	Uses contents of FSR0 to address data memory - value of FSR0 pre-incremented (not a physical register)							N/A	55, 97	
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register), value of FSR0 offset by W							ter), value of	N/A	55, 97
FSR0H	—		—	_	Indirect Data I	Memory Address	Pointer 0 High		xxxx	55, 96
FSR0L	Indirect Data I	Memory Addre	ss Pointer 0 L	ow Byte					XXXX XXXX	55, 96
WREG	Working Register								XXXX XXXX	55
INDF1	Uses contents	of FSR1 to ac	ldress data m	emory – value	of FSR1 not ch	nanged (not a ph	ysical register)		N/A	55, 96
POSTINC1	Uses contents	of FSR1 to ac	ldress data m	emory – value	of FSR1 post-i	ncremented (not	a physical regi	ster)	N/A	55, 97
POSTDEC1	Uses contents	of FSR1 to ac	ldress data m	emory – value	of FSR1 post-	decremented (no	t a physical reg	ister)	N/A	55, 97
PREINC1	Uses contents	of FSR1 to ac	ldress data m	emory – value	of FSR1 pre-in	cremented (not a	a physical regis	ter)	N/A	55, 97
PLUSW1	Uses contents FSR1 offset by	s of FSR1 to ac y W	ldress data m	emory – value	of FSR1 pre-ir	cremented (not a	a physical regis	ter), value of	N/A	55, 97
FSR1H	_		—	_	Indirect Data I	Memory Address	Pointer 1 High		xxxx	55, 96
FSR1L	Indirect Data Memory Address Pointer 1 Low Byte								XXXX XXXX	55, 96
BSR	_		—	_	Bank Select R	Register			0000	56, 73
INDF2	Uses contents	of FSR2 to ac	dress data m	emory – value	of FSR2 not ch	nanged (not a ph	ysical register)		N/A	56, 96
POSTINC2	Uses contents	of FSR2 to ac	ldress data m	emory – value	of FSR2 post-i	ncremented (not	a physical regi	ster)	N/A	56, 97
POSTDEC2	Uses contents of FSR2 to address data memory – value of FSR2 post-decremented (not a physical register)							ister)	N/A	56, 97
PREINC2	Uses contents	of FSR2 to ac	ldress data m	emory – value	of FSR2 pre-in	cremented (not a	a physical regis	ter)	N/A	56, 97
PLUSW2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register), value of FSR2 offset by W								N/A	56, 97

TABLE 6-2:	REGISTER FILE SUMMARY	(PIC18F2480/2580/4480/4580)
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Legend: x = unknown, u = unchanged, – = unimplemented, q = value depends on condition

Note 1: Bit 21 of the PC is only available in Test mode and Serial Programming modes.

2: The SBOREN bit is only available when CONFIG2L<1:0> = 01; otherwise, it is disabled and reads as '0'. See Section 5.4 "Brown-out Reset (BOR)".

3: These registers and/or bits are not implemented on PIC18F2X80 devices and are read as '0'. Reset values are shown for PIC18F4X80 devices; individual unimplemented bits should be interpreted as '--'.

4: The PLLEN bit is only available in specific oscillator configuration; otherwise, it is disabled and reads as '0'. See Section 3.6.4 "PLL in INTOSC Modes".

5: The RE3 bit is only available when Master Clear Reset is disabled (CONFIG3H<7> = 0); otherwise, RE3 reads as '0'. This bit is read-only.

6: RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

7: CAN bits have multiple functions depending on the selected mode of the CAN module.

8: This register reads all '0's until the ECAN™ technology is set up in Mode 1 or Mode 2.

9: These registers are available on PIC18F4X80 devices only.

7.2.2 TABLAT – TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

7.2.3 TBLPTR – TABLE POINTER REGISTER

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the user ID and the Configuration bits.

The Table Pointer, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations are shown in Table 7-1. These operations on the TBLPTR only affect the low-order 21 bits.

7.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes and erases of the Flash program memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory into TABLAT.

When a TBLWT is executed, the five LSbs of the Table Pointer register (TBLPTR<4:0>) determine which of the 32 program memory holding registers is written to. When the timed write to program memory begins (via the WR bit), the 16 MSbs of the TBLPTR (TBLPTR<21:6>) determine which program memory block of 32 bytes is written to. For more detail, see **Section 7.5 "Writing to Flash Program Memory"**.

When an erase of program memory is executed, the 16 MSbs of the Table Pointer register (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 7-3 describes the relevant boundaries of TBLPTR based on Flash program memory operations.

TABLE 7-1: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS

Example	Operation on Table Pointer					
TBLRD* TBLWT*	TBLPTR is not modified					
TBLRD*+ TBLWT*+	TBLPTR is incremented after the read/write					
TBLRD*- TBLWT*-	TBLPTR is decremented after the read/write					
TBLRD+* TBLWT+*	TBLPTR is incremented before the read/write					

FIGURE 7-3: TABLE POINTER BOUNDARIES BASED ON OPERATION



8.0 DATA EEPROM MEMORY

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, that is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space, but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Four SFRs are used to read and write to the data EEPROM, as well as the program memory. They are:

- EECON1
- EECON2
- EEDATA
- EEADR

The data EEPROM allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and the EEADR register holds the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer; it will vary with voltage and temperature, as well as from chip to chip. Please refer to parameter D122 (Table 28-1 in **Section 28.0 "Electrical Characteristics"**) for exact limits.

8.1 EEADR Register

The EEADR register is used to address the data EEPROM for read and write operations. The 8-bit range of the register can address a memory range of 256 bytes (00h to FFh).

8.2 EECON1 and EECON2 Registers

Access to the data EEPROM is controlled by two registers: EECON1 and EECON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The EECON1 register (Register 8-1) is the control register for data and program memory access. Control bit, EEPGD, determines if the access will be to program or data EEPROM memory. When clear, operations will access the data EEPROM memory. When set, program memory is accessed.

Control bit, CFGS, determines if the access will be to the Configuration registers or to program memory/data EEPROM memory. When set, subsequent operations access Configuration registers. When CFGS is clear, the EEPGD bit selects either program Flash or data EEPROM memory.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WREN bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note:	During normal operation, the WRERR is						
	read as '1'. This can indicate that a write						
	operation was prematurely terminated by						
	a Reset, or a write operation was						
	attempted improperly.						

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation.

Note:	The EEIF interrupt flag bit (PIR2<4>) is set					
	when the write is complete. It must be					
	cleared in software.					

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (EEPGD = 1). Program memory is read using table read instructions. See **Section 7.1 "Table Reads** and **Table Writes"** regarding table reads.

The EECON2 register is not a physical register. It is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

10.0 INTERRUPTS

The PIC18F2480/2580/4480/4580 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high-priority level or a low-priority level. The high-priority interrupt vector is at 000008h and the low-priority interrupt vector is at 000018h. High-priority interrupts will interrupt any low-priority interrupts that may be in progress.

There are ten registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2, PIR3
- PIE1, PIE2, PIE3
- IPR1, IPR2, IPR3

It is recommended that the Microchip header files supplied with MPLAB[®] IDE be used for the symbolic bit names in these registers. This allows the assembler/ compiler to automatically take care of the placement of these bits within the specified register.

Each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- Priority bit to select high priority or low priority

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h, depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC[®] mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INT-CON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High-priority interrupt sources can interrupt a lowpriority interrupt. Low-priority interrupts are not processed while high-priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INTx pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

Note: Do not use the MOVFF instruction to modify any of the Interrupt Control registers while any interrupt is enabled. Doing so may cause erratic microcontroller behavior.

13.2 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 13-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 High Byte Buffer register. This provides the user with the ability to accurately read all 16 bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, has become invalid due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H Buffer register. The Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 High Byte Buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

13.3 Timer1 Oscillator

An on-chip crystal oscillator circuit is incorporated between pins, T1OSI (input) and T1OSO (amplifier output). It is enabled by setting the Timer1 Oscillator Enable bit, T1OSCEN (T1CON<3>). The oscillator is a low-power circuit rated for 32 kHz crystals. It will continue to run during all power-managed modes. The circuit for a typical LP oscillator is shown in Figure 13-3. Table 13-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

FIGURE 13-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



TABLE 13-1: CAPACITOR SELECTION FOR THE TIMER OSCILLATOR⁽¹⁻⁴⁾

Osc Type	Freq	C1	C2
LP	32 kHz	27 pF	27 pF

- Note 1: Microchip suggests these values as a starting point in validating the oscillator circuit.
 - 2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - **4:** Capacitor values are for design guidance only.

13.3.1 USING TIMER1 AS A CLOCK SOURCE

The Timer1 oscillator is also available as a clock source in power-managed modes. By setting the clock select bits, SCS<1:0> (OSCCON<1:0>), to '01', the device switches to SEC_RUN mode; both the CPU and peripherals are clocked from the Timer1 oscillator. If the IDLEN bit (OSCCON<7>) is cleared and a SLEEP instruction is executed, the device enters SEC_IDLE mode. Additional details are available in **Section 4.0 "Power-Managed Modes"**.

Whenever the Timer1 oscillator is providing the clock source, the Timer1 system clock status flag, T1RUN (T1CON<6>), is set. This can be used to determine the controller's current clocking mode. It can also indicate the clock source being currently used by the Fail-Safe Clock Monitor. If the Clock Monitor is enabled and the Timer1 oscillator fails while providing the clock, polling the T1RUN bit will indicate whether the clock is being provided by the Timer1 oscillator or another source.

13.3.2 LOW-POWER TIMER1 OPTION

The Timer1 oscillator can operate at two distinct levels of power consumption based on device configuration. When the LPT1OSC Configuration bit is set, the Timer1 oscillator operates in a low-power mode. When LPT1OSC is not set, Timer1 operates at a higher power level. Power consumption for a particular mode is relatively constant, regardless of the device's operating mode. The default Timer1 configuration is the higher power mode.

As the low-power Timer1 mode tends to be more sensitive to interference, high noise environments may cause some oscillator instability. The low-power option is, therefore, best suited for low noise applications where power conservation is an important design consideration.

14.0 TIMER2 MODULE

The Timer2 module timer incorporates the following features:

- 8-Bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- · Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSP module

The module is controlled through the T2CON register (Register 14-1), which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 14-1.

14.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (Fosc/4). A 2-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options; these are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>). The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 14.2 "Timer2 Interrupt**").

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset (Power-on Reset, MCLR Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 14-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unkno

Unimplemented: Read as 0
T2OUTPS<3:0>: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale
TMR2ON: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off
T2CKPS<1:0>: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	57
TXREG	EUSART T	ransmit Reg	jister						57
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	57
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	—	WUE	ABDEN	57
SPBRGH	3RGH EUSART Baud Rate Generator Register High Byte								
SPBRG	EUSART E	aud Rate G	enerator Re	gister Low	Byte				57

TABLE 19-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Reserved in PIC18F2X80 devices; always maintain these bits clear.

20.6 A/D Conversions

Figure 20-3 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 20-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT<2:0> bits are set to '010' and selecting a 4 TAD acquisition time before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

FIGURE 20-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)



FIGURE 20-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



REGISTER 24-42: RXMnSIDL: RECEIVE ACCEPTANCE MASK n STANDARD IDENTIFIER MASK REGISTERS, LOW BYTE [0 \leq n \leq 1]

R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x
SID2	SID1	SID0		EXIDEN ⁽¹⁾	_	EID17	EID16
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7-5 SID<2:0>: Standard Identifier Mask bits or Extended Identifier Mask bits (EID<20:18>) bit 4 Unimplemented: Read as '0' bit 3 Mode 0: Unimplemented: Read as '0' Mode 1, 2: EXIDEN: Extended Identifier Filter Enable Mask bit ⁽¹⁾ 1 = Messages selected by the EXIDEN bit in RXFnSIDL will be accepted 0 = Both standard and extended identifier messages will be accepted							
bit 2	Unimplemen	ted: Read as '	כי				
bit 1-0	EID<17:16>:	Extended Iden	tifier Mask bits	6			

Note 1: This bit is available in Mode 1 and 2 only.

REGISTER 24-43: RXMnEIDH: RECEIVE ACCEPTANCE MASK n EXTENDED IDENTIFIER MASK REGISTERS, HIGH BYTE [0 \leq n \leq 1]

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 EID<15:8>: Extended Identifier Mask bits

REGISTER 24-44: RXMnEIDL: RECEIVE ACCEPTANCE MASK n EXTENDED IDENTIFIER MASK REGISTERS, LOW BYTE [0 \leq n \leq 1]

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 EID<7:0>: Extended Identifier Mask bits

24.15.6.1 Receiver Overflow

An overflow condition occurs when the MAB has assembled a valid received message (the message meets the criteria of the acceptance filters) and the receive buffer associated with the filter is not available for loading of a new message. The associated RXBnOVFL bit in the COMSTAT register will be set to indicate the overflow condition. This bit must be cleared by the MCU.

24.15.6.2 Receiver Warning

The receive error counter has reached the MCU warning limit of 96.

24.15.6.3 Transmitter Warning

The transmit error counter has reached the MCU warning limit of 96.

24.15.6.4 Receiver Bus Passive

This will occur when the device has gone to the errorpassive state because the receive error counter is greater or equal to 128.

24.15.6.5 Transmitter Bus Passive

This will occur when the device has gone to the errorpassive state because the transmit error counter is greater or equal to 128.

24.15.6.6 Bus-Off

The transmit error counter has exceeded 255 and the device has gone to bus-off state.

REGISTER 25-14: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	_	—	—	_	SWDTEN ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1	Unimplemented: Read as '0'
bit 0	SWDTEN: Software Controlled Watchdog Timer Enable bit ⁽¹⁾
	1 = Watchdog Timer is on
	0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WDTEN, is enabled.

TABLE 25-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
RCON	IPEN	SBOREN	_	RI	TO	PD	POR	BOR	54
WDTCON	_	_	_	_	_	_	_	SWDTEN	56

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

25.5.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits internal and external writes to data EEPROM. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

25.5.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is readable only. WRTC can only be written via ICSP or an external programmer.

25.6 ID Locations

Eight memory locations (20000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions or during program/verify. The ID locations can be read when the device is code-protected.

25.7 In-Circuit Serial Programming

PIC18F2480/2580/4480/4580 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

25.8 In-Circuit Debugger

When the DEBUG Configuration bit is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB[®] IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 25-4 shows which resources are required by the background debugger.

TABLE 25-4: DEBUGGER RESOURCES

I/O pins:	RB6, RB7
Stack:	2 levels
	-

Note: Memory resources listed in MPLAB[®] IDE.

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP/RE3, VDD, Vss, RB7 and RB6. This will interface to the In-Circuit debugger module available from Microchip or one of the third party development tool companies.

25.9 Single-Supply ICSP Programming

The LVP Configuration bit enables Single-Supply ICSP Programming (formerly known as *Low-Voltage ICSP Programming* or *LVP*). When Single-Supply Programming is enabled, the microcontroller can be programmed without requiring high voltage being applied to the MCLR/VPP/RE3 pin, but the RB5/KBI1/ PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

While programming using <u>Single-Supply</u> Programming, VDD is applied to the $\overline{MCLR/VPP/RE3}$ pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

- Note 1: High-voltage programming is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.
 - 2: While in Low-Voltage ICSP Programming mode, the RB5 pin can no longer be used as a general purpose I/O pin and should be held low during normal operation.
 - 3: When using Low-Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 5 in the TRISB register must be cleared to disable the pull-up on RB5 and ensure the proper operation of the device.
 - 4: If the device Master Clear is disabled, verify that either of the following is done to ensure proper entry into ICSP mode:
 - a) disable Low-Voltage Programming (CONFIG4I<2> = 0); or
 - b) make certain that RB5/PGM is held low during entry into ICSP.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared. RB5/KB11/PGM then becomes available as the digital I/O pin, RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the MCLR/ VPP/RE3 pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a block erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a block erase is required. If a block erase is to be performed when using Low-Voltage Programming, the device must be supplied with VDD of 4.5V to 5.5V.



TABLE 28-18: I²C[™] BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Мах	Units	Conditions	
90	TSU:STA	Start Condition	100 kHz mode	4700	_	ns	Only relevant for Repeated	
		Setup Time	400 kHz mode	600			Start condition	
91	THD:STA	Start Condition	100 kHz mode	4000		ns	After this period, the first	
		Hold Time	400 kHz mode	600	_		clock pulse is generated	
92	Tsu:sto	Stop Condition	100 kHz mode	4700		ns		
		Setup Time	400 kHz mode	600				
93	THD:STO	Stop Condition	100 kHz mode	4000	_	ns		
		Hold Time	400 kHz mode	600				

FIGURE 28-17: I²C[™] BUS DATA TIMING



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