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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp204-e-ml

1.0   DEVICE OVERVIEW

> **Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device specific information for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0088	—	DMA4IF	PMPIF	—	—	—	—	—	—	—	—	DMA3IF	C1IF[(1)]	C1RXIF[(1)]	SPI2IF	SPI2EIF	0000
IFS3	008A	—	RTCIF	DMA5IF	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	C1TXIF[(1)]	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	DMA4IE	PMPIE	—	—	—	—	—	—	—	—	DMA3IE	C1IE[(1)]	C1RXIE[(1)]	SPI2IE	SPI2EIE	0000
IEC3	009A	—	RTCIE	DMA5IE	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	C1TXIE[(1)]	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	00AC	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	IC8IP<2:0>			—	IC7IP<2:0>			—	—	—	—	—	INT1IP<2:0>			4404
IPC6	00B0	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	00B2	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	00B4	—	C1IP<2:0>[(1)]			—	C1RXIP<2:0>[(1)]			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	00B6	—	—	—	—	—	—	—	—	—	—	—	—	—	DMA3IP<2:0>			0004
IPC11	00BA	—	—	—	—	—	DMA4IP<2:0>			—	PMPIP<2:0>			—	—	—	—	0440
IPC15	00C2	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	—	—	—	0440
IPC16	00C4	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	00C6	—	—	—	—	—	C1TXIP<2:0>[(1)]			—	DMA7IP<2:0>			—	DMA6IP<2:0>			0444
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							4444

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Interrupts disabled on devices without ECAN™ modules.

TABLE 4-35: **FUNDAMENTAL ADDRESSING MODES SUPPORTED**

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.5.3 MOVE (MOV) INSTRUCTION

Move instructions provide a greater degree of addressing flexibility than other instructions. In addition to the Addressing modes supported by most MCU instructions, MOV instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

> **Note:** For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

REGISTER 5-2: **NVMKEY: NONVOLATILE MEMORY KEY REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7-0   **NVMKEY<7:0>:** Key Register (write-only) bits

TABLE 7-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
0	0x000004	0x000104	Reserved
1	0x000006	0x000106	Oscillator Failure
2	0x000008	0x000108	Address Error
3	0x00000A	0x00010A	Stack Error
4	0x00000C	0x00010C	Math Error
5	0x00000E	0x00010E	DMA Error
6-7	0x000010-0x000012	0x000110-0x000112	Reserved
8	0x000014	0x000114	INT0 – External Interrupt 0
9	0x000016	0x000116	IC1 – Input Capture 1
10	0x000018	0x000118	OC1 – Output Compare 1
11	0x00001A	0x00011A	T1 – Timer1
12	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	0x00001E	0x00011E	IC2 – Input Capture 2
14	0x000020	0x000120	OC2 – Output Compare 2
15	0x000022	0x000122	T2 – Timer2
16	0x000024	0x000124	T3 – Timer3
17	0x000026	0x000126	SPI1E – SPI1 Error
18	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	0x00002A	0x00012A	U1RX – UART1 Receiver
20	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	0x00002E	0x00012E	ADC1 – ADC 1
22	0x000030	0x000130	DMA1 – DMA Channel 1
23	0x000032	0x000132	Reserved
24	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	0x000038	0x000138	CM – Comparator Interrupt
27	0x00003A	0x00013A	CN – Change Notification Interrupt
28	0x00003C	0x00013C	INT1 – External Interrupt 1
29	0x00003E	0x00013E	Reserved
30	0x000040	0x000140	IC7 – Input Capture 7
31	0x000042	0x000142	IC8 – Input Capture 8
32	0x000044	0x000144	DMA2 – DMA Channel 2
33	0x000046	0x000146	OC3 – Output Compare 3
34	0x000048	0x000148	OC4 – Output Compare 4
35	0x00004A	0x00014A	T4 – Timer4
36	0x00004C	0x00014C	T5 – Timer5
37	0x00004E	0x00014E	INT2 – External Interrupt 2
38	0x000050	0x000150	U2RX – UART2 Receiver
39	0x000052	0x000152	U2TX – UART2 Transmitter
40	0x000054	0x000154	SPI2E – SPI2 Error
41	0x000056	0x000156	SPI2 – SPI2 Transfer Done
42	0x000058	0x000158	C1RX – ECAN1 RX Data Ready
43	0x00005A	0x00015A	C1 – ECAN1 Event
44	0x00005C	0x00015C	DMA3 – DMA Channel 3
45-52	0x00005E-0x00006C	0x00015E-0x00016C	Reserved
53	0x00006E	0x00016E	PMP – Parallel Master Port
54	0x000070	0x000170	DMA – DMA Channel 4

REGISTER 7-9:   IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	C1TXIF[1]	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7   **Unimplemented:** Read as '0'

bit 6   **C1TXIF:** ECAN1 Transmit Data Request Interrupt Flag Status bit[1]

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5   **DMA7IF:** DMA Channel 7 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4   **DMA6IF:** DMA Channel 6 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3   **CRCIF:** CRC Generator Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2   **U2EIF:** UART2 Error Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1   **U1EIF:** UART1 Error Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0   **Unimplemented:** Read as '0'

Note 1:   Interrupts disabled on devices without ECAN™ modules.

REGISTER 7-27:   IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CRCIP<2:0>			—	U2EIP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1EIP<2:0>			—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **CRCIP<2:0>:** CRC Generator Error Interrupt Flag Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **U2EIP<2:0>:** UART2 Error Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **U1EIP<2:0>:** UART1 Error Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3-0   **Unimplemented:** Read as '0'

10.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2 to 4 cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific PIC MCU variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

REGISTER 11-7:   RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	OCFAR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5   **Unimplemented:** Read as '0'

bit 4-0   **OCFAR<4:0>:** Assign Output Compare A (OCFA) to the corresponding RPn pin
                11111 = Input tied to Vss
                11001 = Input tied to RP25
                •
                •
                •
                00001 = Input tied to RP1
                00000 = Input tied to RP0

19.4 ECAN Resources

Many useful resources related to ECAN are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
> http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315

19.4.1   KEY RESOURCES

- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70185)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

19.5 ECAN Control Registers

REGISTER 19-1: **CiCTRL1: ECAN™ CONTROL REGISTER 1**

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	—	REQOP<2:0>		
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit	r = Bit is Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13   **CSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12   **ABAT:** Abort All Pending Transmissions bit

1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11   **Reserved:** Do not use

bit 10-8   **REQOP<2:0>:** Request Operation Mode bits

000 = Set Normal Operation mode
001 = Set Disable mode
010 = Set Loopback mode
011 = Set Listen Only Mode
100 = Set Configuration mode
101 = Reserved
110 = Reserved
111 = Set Listen All Messages mode

bit 7-5   **OPMODE<2:0>:** Operation Mode bits

000 = Module is in Normal Operation mode
001 = Module is in Disable mode
010 = Module is in Loopback mode
011 = Module is in Listen Only mode
100 = Module is in Configuration mode
101 = Reserved
110 = Reserved
111 = Module is in Listen All Messages mode

bit 4   **Unimplemented:** Read as '0'

bit 3   **CANCAP:** CAN Message Receive Timer Capture Event Enable bit

1 = Enable input capture based on CAN message receive
0 = Disable CAN capture

bit 2-1   **Unimplemented:** Read as '0'

bit 0   **WIN:** SFR Map Window Select bit

1 = Use filter window
0 = Use buffer window

REGISTER 19-26: **CiTRmnCON: ECAN™ TX/RX BUFFER m CONTROL REGISTER**
(m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI<1:0>	
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm[1]	TXLARBm[1]	TXERRm[1]	TXREQm	RTRENm	TXmPRI<1:0>	
bit 7							bit 0

Legend:		C = Writeable bit, but only '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   See Definition for Bits 7-0, Controls Buffer n

bit 7   **TXENm:** TX/RX Buffer Selection bit

   1 = Buffer TRBn is a transmit buffer
   0 = Buffer TRBn is a receive buffer

bit 6   **TXABTm:** Message Aborted bit[1]

   1 = Message was aborted
   0 = Message completed transmission successfully

bit 5   **TXLARBm:** Message Lost Arbitration bit[1]

   1 = Message lost arbitration while being sent
   0 = Message did not lose arbitration while being sent

bit 4   **TXERRm:** Error Detected During Transmission bit[1]

   1 = A bus error occurred while the message was being sent
   0 = A bus error did not occur while the message was being sent

bit 3   **TXREQm:** Message Send Request bit

   1 = Requests that a message be sent. The bit automatically clears when the message is successfully sent
   0 = Clearing the bit to '0' while set requests a message abort

bit 2   **RTRENm:** Auto-Remote Transmit Enable bit

   1 = When a remote transmit is received, TXREQ will be set
   0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0   **TXmPRI<1:0>:** Message Transmission Priority bits

   11 = Highest message priority
   10 = High intermediate message priority
   01 = Low intermediate message priority
   00 = Lowest message priority

Note 1:   This bit is cleared when the TXREQ bit is set.

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers are located in DMA RAM.

21.1 Comparator Resources

Many useful resources related to Comparators are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555

21.1.1 KEY RESOURCES

- **Section 34. "Comparator"** (DS70212)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

24.2 PMP Control Registers

REGISTER 24-1: PMCON: PARALLEL PORT CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0[1]	U-0	R/W-0[1]	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	—	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	**PMPEN:** Parallel Master Port Enable bit
	`1` = PMP enabled
	`0` = PMP disabled, no off-chip access performed
bit 14	**Unimplemented:** Read as '`0`'
bit 13	**PSIDL:** Stop in Idle Mode bit
	`1` = Discontinue module operation when device enters Idle mode
	`0` = Continue module operation in Idle mode
bit 12-11	**ADRMUX1:ADRMUX0:** Address/Data Multiplexing Selection bits[1]
	`11` = Reserved
	`10` = All 16 bits of address are multiplexed on PMD<7:0> pins
	`01` = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 3 bits are multiplexed on PMA<10:8>
	`00` = Address and data appear on separate pins
bit 10	**PTBEEN:** Byte Enable Port Enable bit (16-bit Master mode)
	`1` = PMBE port enabled
	`0` = PMBE port disabled
bit 9	**PTWREN:** Write Enable Strobe Port Enable bit
	`1` = PMWR/PMENB port enabled
	`0` = PMWR/PMENB port disabled
bit 8	**PTRDEN:** Read/Write Strobe Port Enable bit
	`1` = PMRD/$\overline{PMWR}$ port enabled
	`0` = PMRD/$\overline{PMWR}$ port disabled
bit 7-6	**CSF1:CSF0:** Chip Select Function bits
	`11` = Reserved
	`10` = PMCS1 functions as chip select
	`0x` = PMCS1 functions as address bit 14
bit 5	**ALP:** Address Latch Polarity bit[1]
	`1` = Active-high (PMALL and PMALH)
	`0` = Active-low ($\overline{PMALL}$ and $\overline{PMALH}$)
bit 4	**Unimplemented:** Read as '`0`'
bit 3	**CS1P:** Chip Select 1 Polarity bit[1]
	`1` = Active-high (PMCS1/PMCS1)
	`0` = Active-low ($\overline{PMCS1}$/$\overline{PMCS1}$)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

TABLE 25-5:   CODE FLASH SECURITY SEGMENT SIZES FOR 128 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K		BSS<2:0> = x10 1K		BSS<2:0> = x01 4K		BSS<2:0> = x00 8K	
SSS<2:0> = x11 0K	VS = 256 IW GS = 43776 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 768 IW GS = 43008 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 3840 IW GS = 39936 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh
SSS<2:0> = x10 4K	VS = 256 IW SS = 3840 IW GS = 39936 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 768 IW SS = 3072 IW GS = 39936 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 3840 IW GS = 39936 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh
SSS<2:0> = x01 8K	VS = 256 IW SS = 7936 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 768 IW SS = 7168 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x010000h 0x0157FEh	VS = 256 IW BS = 3840 IW SS = 4096 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 35840 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh
SSS<2:0> = x00 16K	VS = 256 IW SS = 16128 IW GS = 27648 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 768 IW SS = 15360 IW GS = 27648 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 3840 IW SS = 12288 IW GS = 27648 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh	VS = 256 IW BS = 7936 IW SS = 8192 IW GS = 27648 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00FFFEh 0x010000h 0x0157FEh

NOTES:

FIGURE 28-3: CLKO AND I/O TIMING CHARACTERISTICS

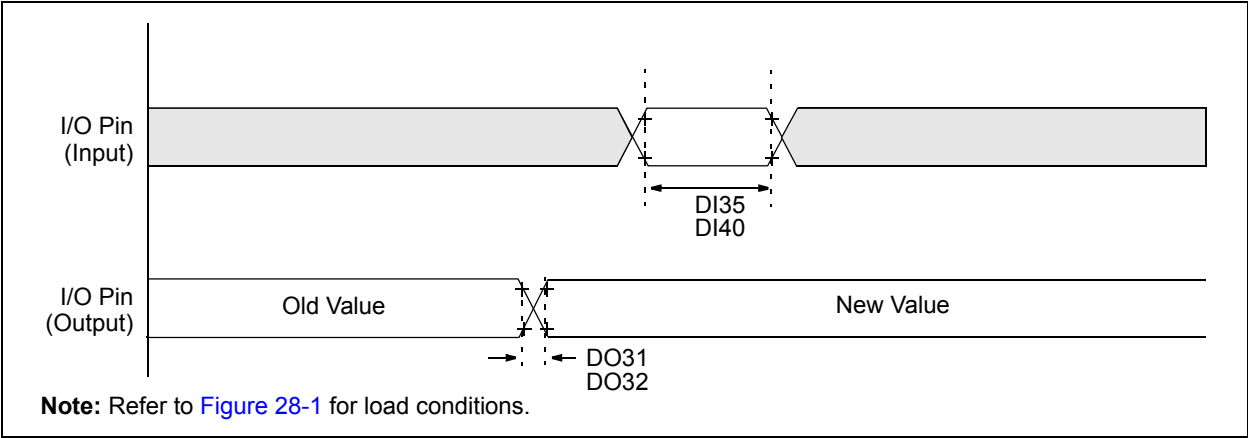**Note:** Refer to Figure 28-1 for load conditions.

TABLE 28-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ$^{(1)}$	Max	Units	Conditions	
DO31	T$_{IOR}$	Port Output Rise Time	—	10	25	ns	—	
DO32	T$_{IOF}$	Port Output Fall Time	—	10	25	ns	—	
DI35	T$_{INP}$	INTx Pin High or Low Time (input)	20	—	—	ns	—	
DI40	T$_{RBP}$	CNx High or Low Time (input)	2	—	—	T$_{CY}$	—	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

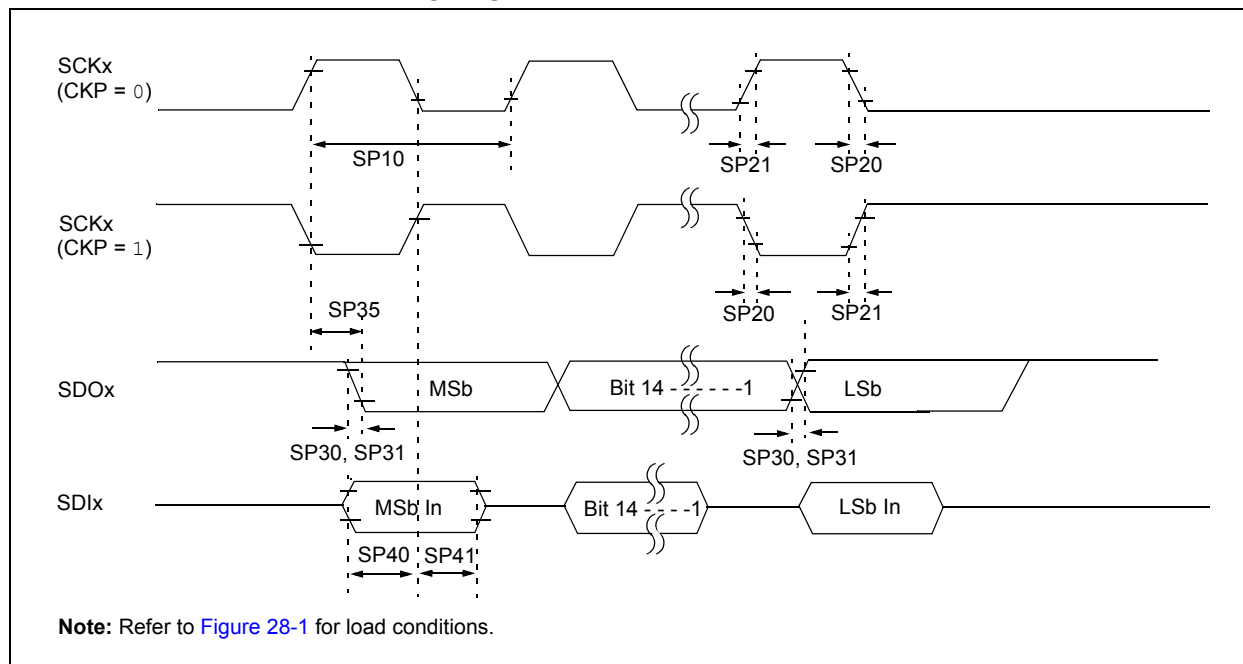**FIGURE 28-12:** SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS

Note: Refer to Figure 28-1 for load conditions.

TABLE 28-31: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

| AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ[2]	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	—	9	MHz	-40ºC to +125ºC and see **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

   2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

   3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

   4: Assumes 50 pF load on all SPIx pins.

FIGURE 28-15: **SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**

Note: Refer to Figure 28-1 for load conditions.
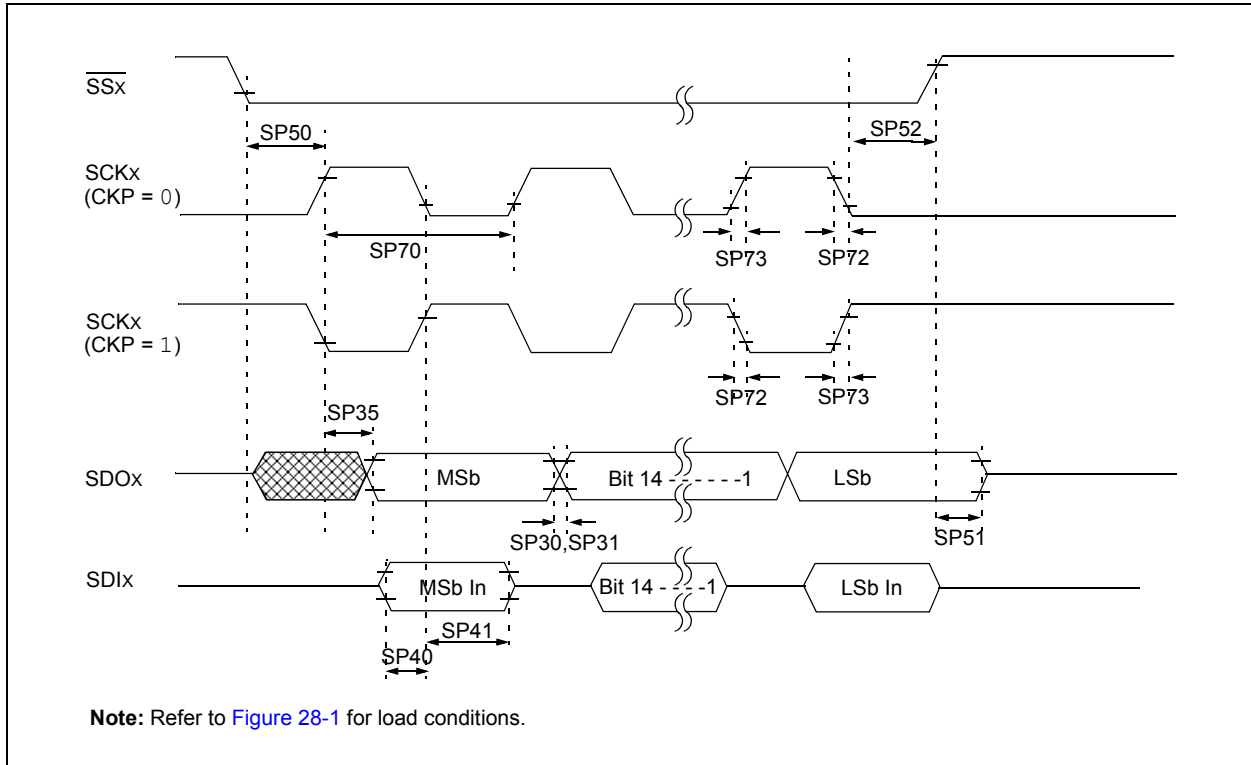
Revision C (May 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

• Changed all instances of OSCI to OSC1 and OSCO to OSC2
• Changed all instances of VDDCORE and VDDCORE/ VCAP to VCAP/VDDCORE

The other changes are referenced by their respective section in the following table.

TABLE A-2:   MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Microcontrollers"	Updated all pin diagrams to denote the pin voltage tolerance (see **"Pin Diagrams"**).
	Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to VSS.
Section 1.0 "Device Overview"	Updated AVDD in the PINOUT I/O Descriptions (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Microcontrollers"	Added new section to the data sheet that provides guidelines on getting started with 16-bit Digital Signal Controllers.
	Added Peripheral Pin Select (PPS) capability column to Pinout I/O Descriptions (see Table 1-1).
Section 3.0 "CPU"	Updated CPU Core Block Diagram with a connection from the DSP Engine to the Y Data Bus (see Figure 3-1).
Section 4.0 "Memory Organization"	Updated Reset value for CORCON in the CPU Core Register Map (see Table 4-1).
	Updated Reset value for IPC15 in the Interrupt Controller Register Map (see Table 4-4).
	Removed the FLTA1IE bit (IEC3) from the Interrupt Controller Register Map (see Table 4-4).
	Updated bit locations for RPINR25 in the Peripheral Pin Select Input Register Map (see Table 4-19).
	Updated the Reset value for CLKDIV in the System Control Register Map (see Table 4-31).
Section 5.0 "Flash Program Memory"	Updated **Section 5.3 "Programming Operations"** with programming time formula.
Section 9.0 "Oscillator Configuration"	Updated the Oscillator System Diagram and added Note 2 (see Figure 9-1).
	Updated default bit values for DOZE<2:0> and FRCDIV<2:0> in the Clock Divisor (CLKDIV) Register (see Register 9-2).
	Added a paragraph regarding FRC accuracy at the end of **Section 9.1.1 "System Clock Sources"**.
	Added Note 3 to **Section 9.2.2 "Oscillator Switching Sequence"**.
	Added Note 1 to the FRC Oscillator Tuning (OSCTUN) Register (see Register 9-4).