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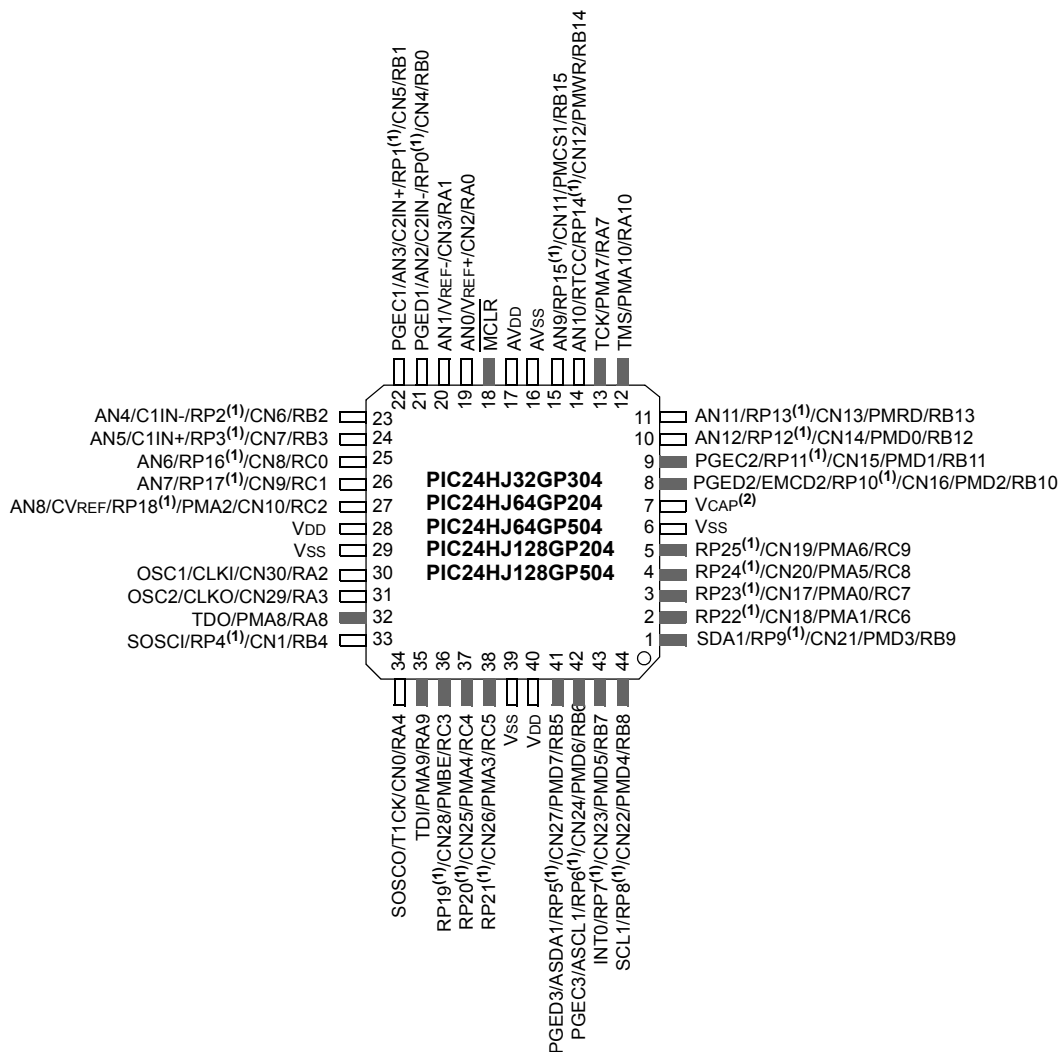
#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp204t-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp204t-i-ml</a>

# Pin Diagrams (Continued)

## 44-Pin TQFP

■ Pins are up to 5V tolerant



- Note** 1: The RPx pins can be used by any remappable peripheral. See [Table 1](#) in this section for the list of available peripherals.  
 2: Refer to [Section 2.3 "CPU Logic Filter Capacitor Connection \(Vcap\)"](#) for proper connection to this pin.

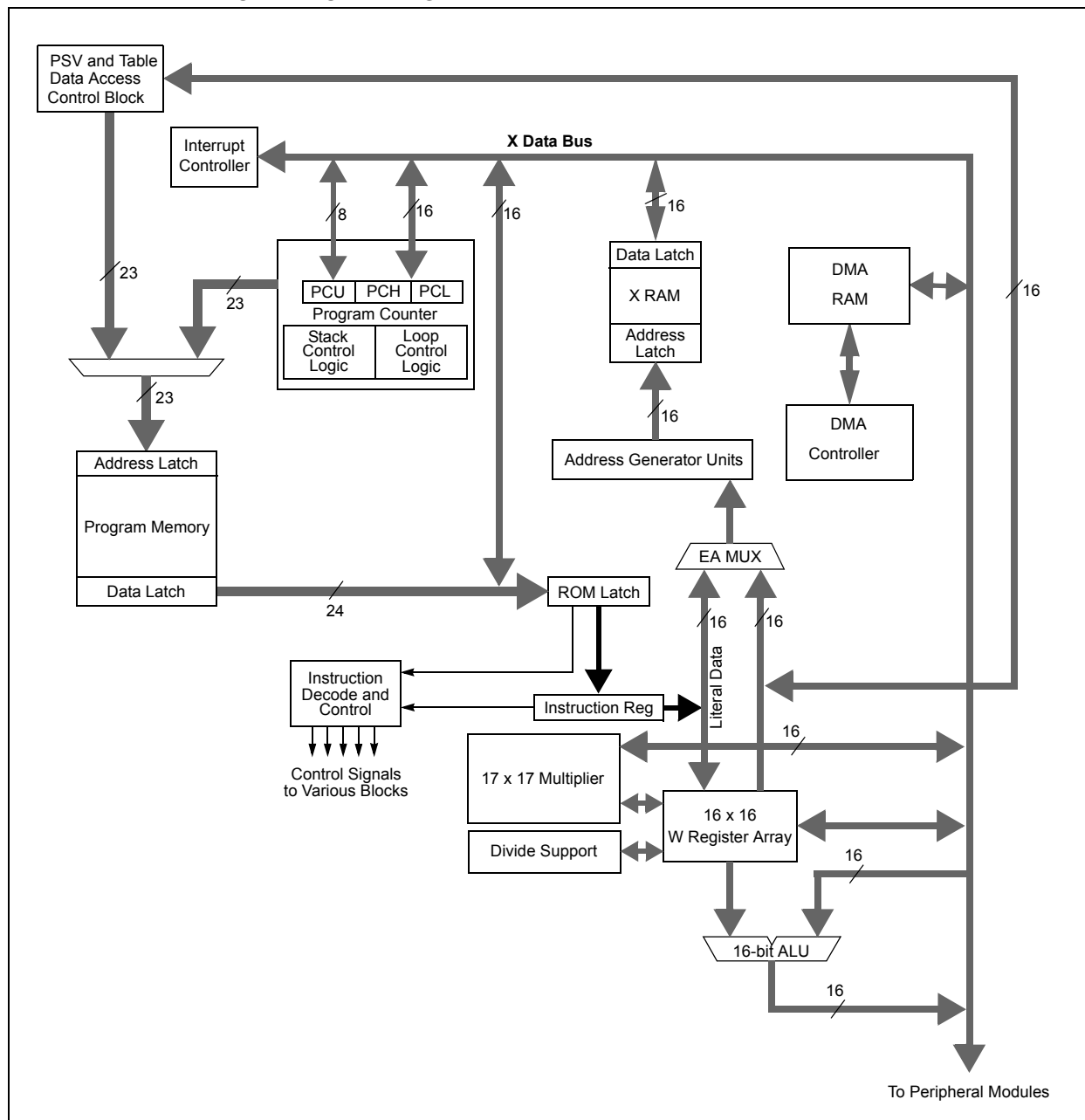
### 3.3 Special MCU Features

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 features a 17-bit by 17-bit, single-cycle multiplier. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication makes mixed-sign multiplication possible.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices support 16/16 and 32/16 integer divide operations. All divide instructions are iterative operations. They must be executed within a **REPEAT** loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A multi-bit data shifter is used to perform up to a 16-bit, left or right shift in a single cycle.

**FIGURE 3-1: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 CPU CORE BLOCK DIAGRAM**



## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. “Program Memory”** (DS70203) of the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

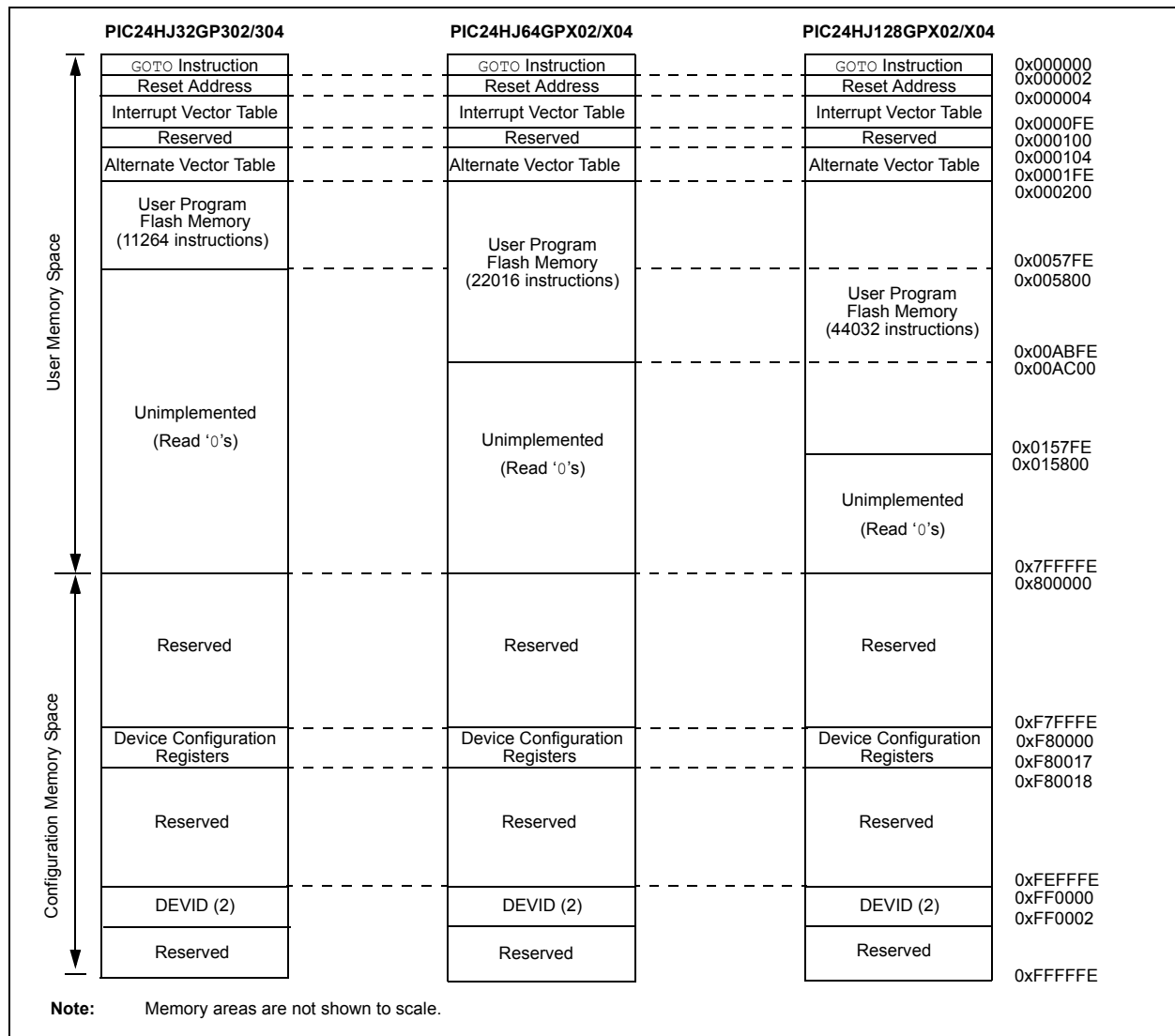
## 4.1 Program Address Space

The program address memory space of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory map for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices is shown in **Figure 4-1**.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 DEVICES**



## 5.0 FLASH PROGRAM MEMORY

**Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Programming”** (DS70191) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGEC1/PGED1,

PGEC2/PGED2 or PGEC3/PGED3), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data either in blocks or ‘rows’ of 64 instructions (192 bytes) at a time or a single program memory word, and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

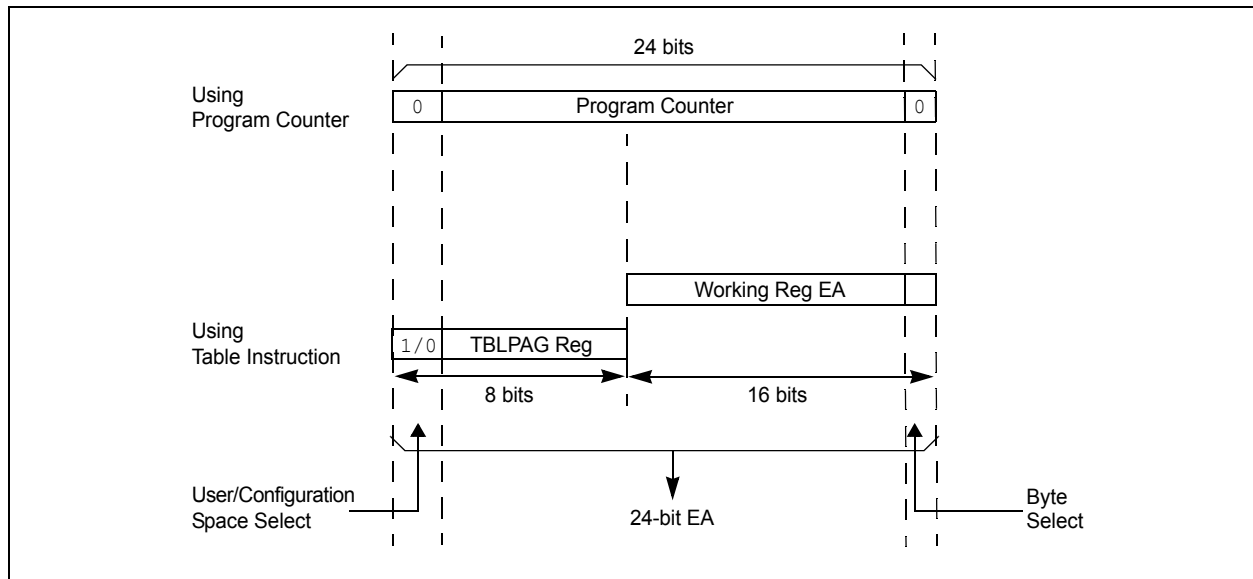
### 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits <7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in [Figure 5-1](#).

The TBLRDL and the TBLWTL instructions are used to read or write to bits <15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits <23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

**FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS**



**REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3**

U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	RTCIF	DMA5IF	—	—	—	—	—
bit 15			bit 8				

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7			bit 0				

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 13 **DMA5IF:** DMA Channel 5 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 12-0 **Unimplemented:** Read as '0'

**REGISTER 11-7: RPNR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	OCFAR<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **OCFAR<4:0>:** Assign Output Compare A (OCFA) to the corresponding RPN pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

**REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22**

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK2R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI2R<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK2R<4:0>:** Assign SPI2 Clock Input (SCK2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•  
•  
•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI2R<4:0>:** Assign SPI2 Data Input (SDI2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•  
•  
•

00001 = Input tied to RP1

00000 = Input tied to RP0



**REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER**

R-0 HSC	R-0 HSC	U-0	U-0	U-0	R/C-0 HS	R-0 HSC	R-0 HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0 HS	R/C-0 HS	R-0 HSC	R/C-0 HSC	R/C-0 HSC	R-0 HSC	R-0 HSC	R-0 HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

<b>Legend:</b>	U = Unimplemented bit, read as '0'	C = Clear only bit
R = Readable bit	W = Writable bit	HS = Set in hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15      **ACKSTAT:** Acknowledge Status bit  
(when operating as I<sup>2</sup>C™ master, applicable to master transmit operation)  
1 = NACK received from slave  
0 = ACK received from slave  
Hardware set or clear at end of slave Acknowledge.
- bit 14      **TRSTAT:** Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation)  
1 = Master transmit is in progress (8 bits + ACK)  
0 = Master transmit is not in progress  
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.
- bit 13-11      **Unimplemented:** Read as '0'
- bit 10      **BCL:** Master Bus Collision Detect bit  
1 = A bus collision has been detected during a master operation  
0 = No collision  
Hardware set at detection of bus collision.
- bit 9      **GCSTAT:** General Call Status bit  
1 = General call address was received  
0 = General call address was not received  
Hardware set when address matches general call address. Hardware clear at Stop detection.
- bit 8      **ADD10:** 10-bit Address Status bit  
1 = 10-bit address was matched  
0 = 10-bit address was not matched  
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.
- bit 7      **IWCOL:** Write Collision Detect bit  
1 = An attempt to write the I2CxTRN register failed because the I<sup>2</sup>C module is busy  
0 = No collision  
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).
- bit 6      **I2COV:** Receive Overflow Flag bit  
1 = A byte was received while the I2CxRCV register is still holding the previous byte  
0 = No overflow  
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5      **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)  
1 = Indicates that the last byte received was data  
0 = Indicates that the last byte received was device address  
Hardware clear at device address match. Hardware set by reception of slave byte.
- bit 4      **P:** Stop bit  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last  
Hardware set or clear when Start, Repeated Start or Stop detected.

## 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "UART"** (DS70188) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN 2.0, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA® encoder and decoder.

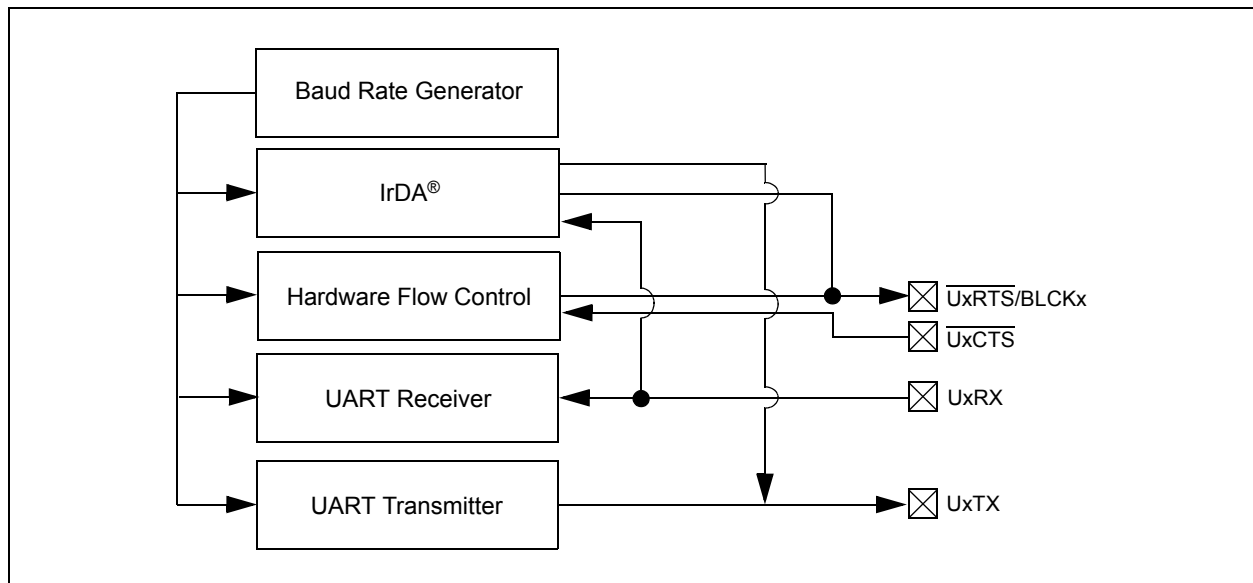
The primary features of the UART module are:

- Full-Duplex, 8- or 9-bit Data Transmission through the UxTX and UxRX pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or two stop bits
- Hardware flow control option with  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins
- Fully integrated Baud Rate Generator with 16-bit prescaler
- Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-deep First-In First-Out (FIFO) Transmit Data buffer
- 4-deep FIFO Receive Data buffer
- Parity, framing and buffer overrun error detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive interrupts
- A separate interrupt for all UART error conditions
- Loopback mode for diagnostic support
- Support for sync and break characters
- Support for automatic baud rate detection
- IrDA® encoder and decoder logic
- 16x baud clock output for IrDA® support

A simplified block diagram of the UART module is shown in **Figure 18-1**. The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 18-1: UART SIMPLIFIED BLOCK DIAGRAM**



**Note 1:** Both UART1 and UART2 can trigger a DMA data transfer.

**2:** If DMA transfers are required, the UART TX/RX FIFO buffer must be set to a size of 1 byte/word (i.e., UTXISEL<1:0> = 00 and URXISEL<1:0> = 00).

## 21.2 Comparator Control Register

REGISTER 21-1: CMCON: COMPARATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIDL	—	C2EVT	C1EVT	C2EN	C1EN	C2OUTEN <sup>(1)</sup>	C1OUTEN <sup>(2)</sup>
bit 15						bit 8	

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	C2NEG	C2POS	C1NEG	C1POS
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CMIDL:** Stop in Idle Mode  
 1 = When device enters Idle mode, module does not generate interrupts. Module is still enabled  
 0 = Continue normal module operation in Idle mode
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **C2EVT:** Comparator 2 Event  
 1 = Comparator output changed states  
 0 = Comparator output did not change states
- bit 12 **C1EVT:** Comparator 1 Event  
 1 = Comparator output changed states  
 0 = Comparator output did not change states
- bit 11 **C2EN:** Comparator 2 Enable  
 1 = Comparator is enabled  
 0 = Comparator is disabled
- bit 10 **C1EN:** Comparator 1 Enable  
 1 = Comparator is enabled  
 0 = Comparator is disabled
- bit 9 **C2OUTEN:** Comparator 2 Output Enable<sup>(1)</sup>  
 1 = Comparator output is driven on the output pad  
 0 = Comparator output is not driven on the output pad
- bit 8 **C1OUTEN:** Comparator 1 Output Enable<sup>(2)</sup>  
 1 = Comparator output is driven on the output pad  
 0 = Comparator output is not driven on the output pad
- bit 7 **C2OUT:** Comparator 2 Output bit  
 When C2INV = 0:  
 1 = C2 VIN+ > C2 VIN-  
 0 = C2 VIN+ < C2 VIN-  
 When C2INV = 1:  
 0 = C2 VIN+ > C2 VIN-  
 1 = C2 VIN+ < C2 VIN-

**Note 1:** If C2OUTEN = 1, the C2OUT peripheral output must be configured to an available RPx pin. See [Section 11.6 “Peripheral Pin Select”](#) for more information.

**2:** If C1OUTEN = 1, the C1OUT peripheral output must be configured to an available RPx pin. See [Section 11.6 “Peripheral Pin Select”](#) for more information.

**REGISTER 24-5: PMSTAT: PARALLEL PORT STATUS REGISTER**

R-0	R/W-0, HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15				bit 8			

R-1	R/W-0, HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7				bit 0			

<b>Legend:</b>	HS = Hardware Set bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **IBF:** Input Buffer Full Status bit  
             1 = All writable input buffer registers are full  
             0 = Some or all of the writable input buffer registers are empty
- bit 14      **IBOV:** Input Buffer Overflow Status bit  
             1 = A write attempt to a full input byte register occurred (must be cleared in software)  
             0 = No overflow occurred
- bit 13-12    **Unimplemented:** Read as '0'
- bit 11-8     **IB3F:IB0F** Input Buffer x Status Full bits  
             1 = Input buffer contains data that has not been read (reading buffer will clear this bit)  
             0 = Input buffer does not contain any unread data
- bit 7        **OBE:** Output Buffer Empty Status bit  
             1 = All readable output buffer registers are empty  
             0 = Some or all of the readable output buffer registers are full
- bit 6        **OBUF:** Output Buffer Underflow Status bits  
             1 = A read occurred from an empty output byte register (must be cleared in software)  
             0 = No underflow occurred
- bit 5-4     **Unimplemented:** Read as '0'
- bit 3-0     **OB3E:OB0E** Output Buffer x Status Empty bit  
             1 = Output buffer is empty (writing data to the buffer will clear this bit)  
             0 = Output buffer contains data that has not been transmitted

## 25.0 SPECIAL FEATURES

**Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33F/PIC24H Family Reference Manual”. Please see the Microchip web site ([www.microchip.com](http://www.microchip.com)) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices include the following features that are intended to maximize application flexibility and reliability, and minimize cost through elimination of external components:

- Flexible configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

## 25.1 Configuration Bits

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices provide nonvolatile memory implementation for device configuration bits. Refer to [Section 25. “Device Configuration”](#) (DS70194), in the “dsPIC33F/PIC24H Family Reference Manual” for more information on this implementation.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in [Table 25-1](#).

Note that address 0xF80000 is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFF), which can only be accessed using table reads and table writes.

The Device Configuration register map is shown in [Table 25-1](#).

**TABLE 25-1: DEVICE CONFIGURATION REGISTER MAP**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	RBS<1:0>		—	—	BSS<2:0>			BWRP
0xF80002	FSS <sup>(1)</sup>	RSS<1:0>		—	—	SSS<2:0>			SWRP
0xF80004	FGS	—	—	—	—	—	GSS<1:0>		GWRP
0xF80006	FOSCSEL	IESO	—	—	—		FNOSC<2:0>		
0xF80008	FOSC	FCKSM<1:0>		IOL1WAY	—	—	OSCIOFNC	POSCMD<1:0>	
0xF8000A	FWDT	FWDTEN	WINDIS	—	WDTPRE	WDTPOST<3:0>			
0xF8000C	FPOR	Reserved <sup>(2)</sup>			ALTI2C	—	FPWRT<2:0>		
0xF8000E	FICD	Reserved <sup>(3)</sup>		JTAGEN	—	—	—	ICS<1:0>	
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							
0xF80014	FUID2	User Unit ID Byte 2							
0xF80016	FUID3	User Unit ID Byte 3							

**Legend:** — = unimplemented bit, read as ‘0’.

**Note 1:** This Configuration register is not available and reads as 0xFF on PIC24HJ32GP302/304 devices.

**2:** These bits are reserved and always read as ‘1’.

**3:** These bits are reserved for use by development tools and must be programmed as ‘1’.

## 28.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 electrical characteristics. Additional information is provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

### Absolute Maximum Ratings<sup>(1)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +160°C
Voltage on VDD with respect to Vss .....	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss <sup>(4)</sup> .....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD ≥ 3.0V <sup>(4)</sup> .....	-0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V <sup>(4)</sup> .....	-0.3V to 3.6V
Maximum current out of Vss pin .....	300 mA
Maximum current into VDD pin <sup>(2)</sup> .....	250 mA
Maximum current sourced/sunk by any 2x I/O pin <sup>(3)</sup> .....	8 mA
Maximum current sourced/sunk by any 4x I/O pin <sup>(3)</sup> .....	15 mA
Maximum current sourced/sunk by any 8x I/O pin <sup>(3)</sup> .....	25 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports <sup>(2)</sup> .....	200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see [Table 28-2](#)).

**3:** Exceptions are CLKOUT, which is able to sink/source 25 mA, and the VREF+, VREF-, SCLx, SDAX, PGECx and PGEDx pins, which are able to sink/source 12 mA.

**4:** See the “[Pin Diagrams](#)” section for 5V tolerant pins.

FIGURE 28-3: CLKO AND I/O TIMING CHARACTERISTICS

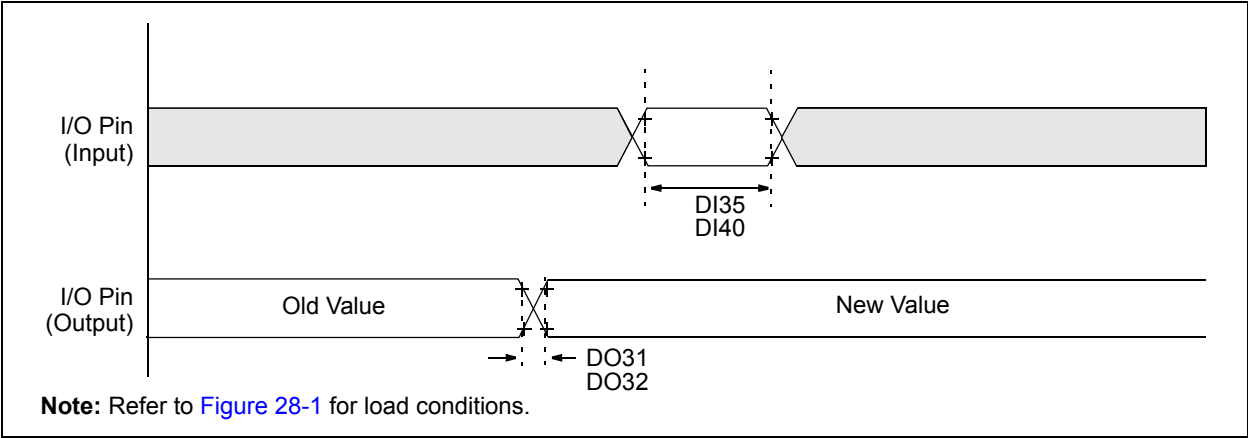
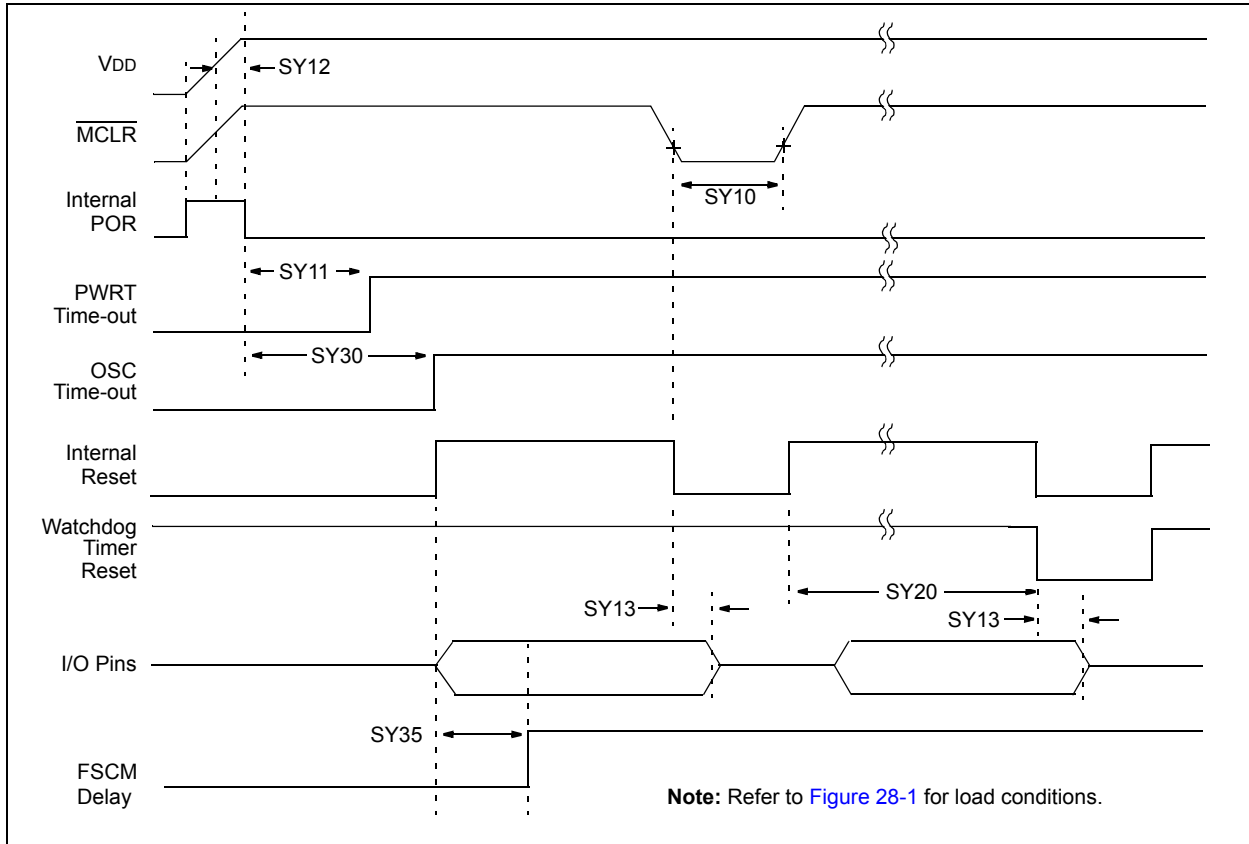


TABLE 28-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	—
DO32	TioF	Port Output Fall Time	—	10	25	ns	—
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TcY	—

**Note 1:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

**FIGURE 28-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS**





**TABLE 28-23: TIMER2 AND TIMER 4 EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min	Typ	Max	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 28-24: TIMER3 AND TIMER5 EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min	Typ	Max	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 28-35: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	—	—	11	MHz	See <b>Note 3</b>
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter <a href="#">DO32</a> and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter <a href="#">DO31</a> and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter <a href="#">DO32</a> and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter <a href="#">DO31</a> and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sch, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP50	TssL2sch, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance <sup>(4)</sup>	10	—	50	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See <b>Note 4</b>

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

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