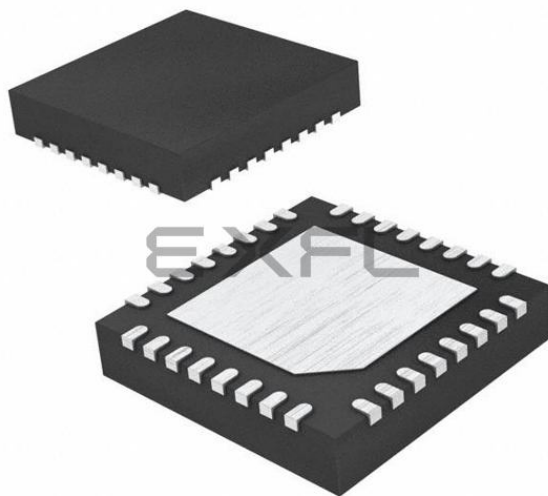




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp502-h-mm

FIGURE 4-6: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION

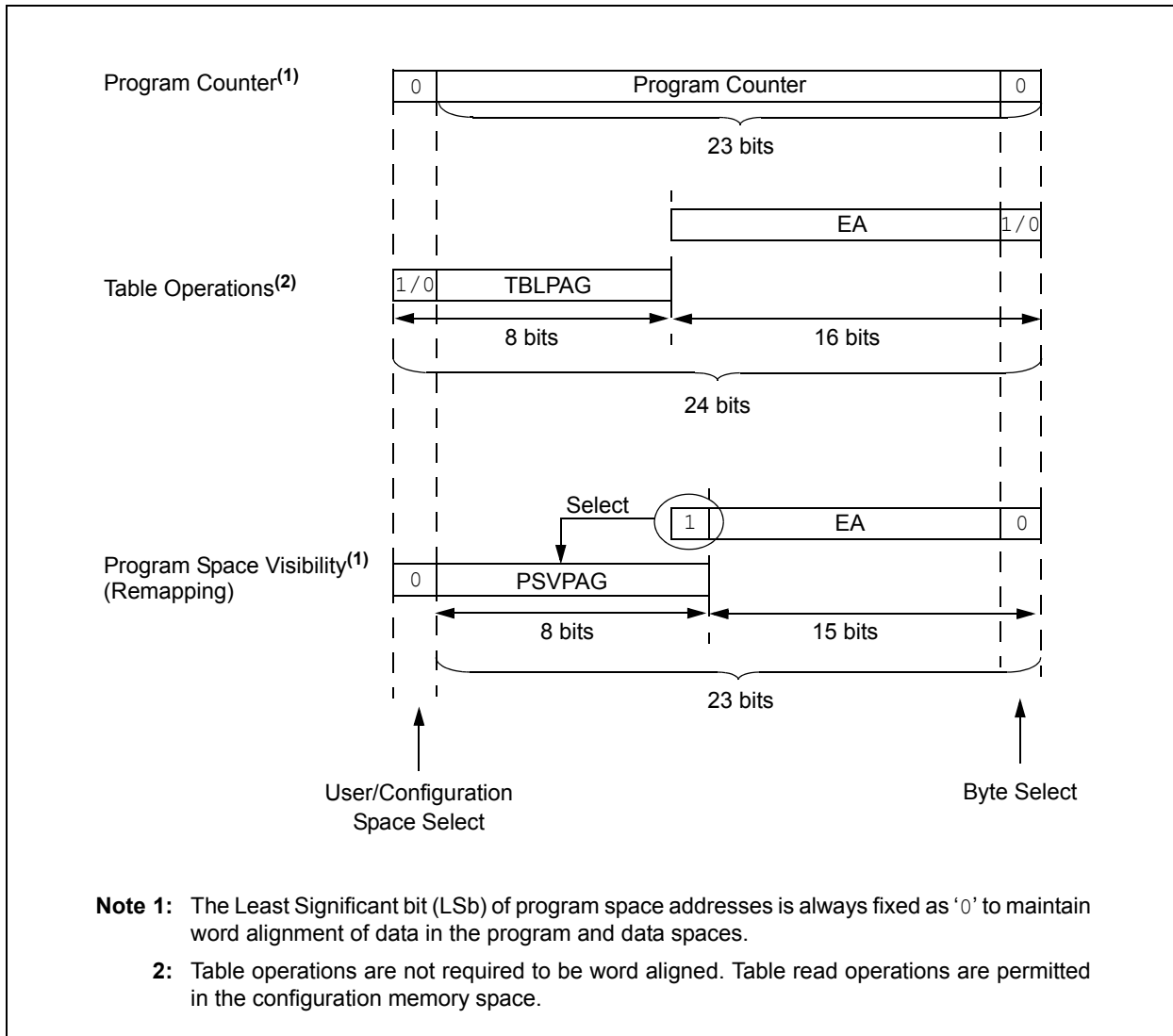


TABLE 7-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
0	0x000004	0x000104	Reserved
1	0x000006	0x000106	Oscillator Failure
2	0x000008	0x000108	Address Error
3	0x00000A	0x00010A	Stack Error
4	0x00000C	0x00010C	Math Error
5	0x00000E	0x00010E	DMA Error
6-7	0x000010-0x000012	0x000110-0x000112	Reserved
8	0x000014	0x000114	INT0 – External Interrupt 0
9	0x000016	0x000116	IC1 – Input Capture 1
10	0x000018	0x000118	OC1 – Output Compare 1
11	0x00001A	0x00011A	T1 – Timer1
12	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	0x00001E	0x00011E	IC2 – Input Capture 2
14	0x000020	0x000120	OC2 – Output Compare 2
15	0x000022	0x000122	T2 – Timer2
16	0x000024	0x000124	T3 – Timer3
17	0x000026	0x000126	SPI1E – SPI1 Error
18	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	0x00002A	0x00012A	U1RX – UART1 Receiver
20	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	0x00002E	0x00012E	ADC1 – ADC 1
22	0x000030	0x000130	DMA1 – DMA Channel 1
23	0x000032	0x000132	Reserved
24	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	0x000038	0x000138	CM – Comparator Interrupt
27	0x00003A	0x00013A	CN – Change Notification Interrupt
28	0x00003C	0x00013C	INT1 – External Interrupt 1
29	0x00003E	0x00013E	Reserved
30	0x000040	0x000140	IC7 – Input Capture 7
31	0x000042	0x000142	IC8 – Input Capture 8
32	0x000044	0x000144	DMA2 – DMA Channel 2
33	0x000046	0x000146	OC3 – Output Compare 3
34	0x000048	0x000148	OC4 – Output Compare 4
35	0x00004A	0x00014A	T4 – Timer4
36	0x00004C	0x00014C	T5 – Timer5
37	0x00004E	0x00014E	INT2 – External Interrupt 2
38	0x000050	0x000150	U2RX – UART2 Receiver
39	0x000052	0x000152	U2TX – UART2 Transmitter
40	0x000054	0x000154	SPI2E – SPI2 Error
41	0x000056	0x000156	SPI2 – SPI2 Transfer Done
42	0x000058	0x000158	C1RX – ECAN1 RX Data Ready
43	0x00005A	0x00015A	C1 – ECAN1 Event
44	0x00005C	0x00015C	DMA3 – DMA Channel 3
45-52	0x00005E-0x00006C	0x00015E-0x00016C	Reserved
53	0x00006E	0x00016E	PMP – Parallel Master Port
54	0x000070	0x000170	DMA – DMA Channel 4

TABLE 7-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	IVT Address	AIVT Address	Interrupt Source
55-68	0x000072-0x00008C	0x000172-0x00018C	Reserved
69	0x00008E	0x00018E	DMA5 – DMA Channel 5
70	0x000090	0x000190	RTCC – Real Time Clock
71-72	0x000092-0x000094	0x000192-0x000194	Reserved
73	0x000096	0x000196	U1E – UART1 Error
74	0x000098	0x000198	U2E – UART2 Error
75	0x00009A	0x00019A	CRC – CRC Generator Interrupt
76	0x00009C	0x00019C	DMA6 – DMA Channel 6
77	0x00009E	0x00019E	DMA7 – DMA Channel 7
78	0x0000A0	0x0001A0	C1TX – ECAN1 TX Data Request
79-126	0x0000A2-0x0000FE	0x0001A2-0x0001FE	Reserved

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

bit 2	CMIE: Comparator Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled
bit 1	MI2C1IE: I2C1 Master Events Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled
bit 0	SI2C1IE: I2C1 Slave Events Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled

REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP<2:0>			—	CMIP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP<2:0>			—	SI2C1IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

REGISTER 7-25: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	DMA4IP<2:0>		
bit 15					bit 8		

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PMPIP<2:0>			—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **PMPIP<2:0>:** Parallel Master Port Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

8.1 DMA Resources

Many useful resources related to DMA are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555>

8.1.1 KEY RESOURCES

- **Section 38. “Direct Memory Access (DMA) (Part III)” (DS70215)**
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

8.2 DMAC Registers

Each DMAC Channel x ($x = 0, 1, 2, 3, 4, 5, 6$ or 7) contains the following registers:

- A 16-bit DMA Channel Control register (DMAxCON)
- A 16-bit DMA Channel IRQ Select register (DMAxREQ)
- A 16-bit DMA RAM Primary Start Address register (DMAxSTA)
- A 16-bit DMA RAM Secondary Start Address register (DMAxSTB)
- A 16-bit DMA Peripheral Address register (DMAxPAD)
- A 10-bit DMA Transfer Count register (DMAxCNT)

An additional pair of status registers, DMACS0 and DMACS1, are common to all DMAC channels. DMACS0 contains the DMA RAM and SFR write collision flags, XWCOLx and PWCOLx, respectively. DMACS1 indicates DMA channel and Ping-Pong mode status.

The DMAxCON, DMAxREQ, DMAxPAD and DMAxCNT are all conventional read/write registers. Reads of DMAxSTA or DMAxSTB reads the contents of the DMA RAM Address register. Writes to DMAxSTA or DMAxSTB write to the registers. This allows the user to determine the DMA buffer pointer value (address) at any time.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

9.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides significant flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 9-2.

The output of the primary oscillator or FRC, denoted as 'FIN', is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL's Voltage Controlled Oscillator (VCO). The input to the VCO must be selected in the range of 0.8 MHz to 8 MHz. The prescale factor 'N1' is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFB<8:0>), provides a factor 'M', by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor 'N2'. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). 'N2' can be either 2, 4 or 8, and must be selected such that the PLL output frequency (Fosc) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output 'FIN', the PLL output 'Fosc' is given by:

EQUATION 9-2: Fosc CALCULATION

$$F_{OSC} = F_{IN} \cdot \left(\frac{M}{N1 \cdot N2} \right)$$

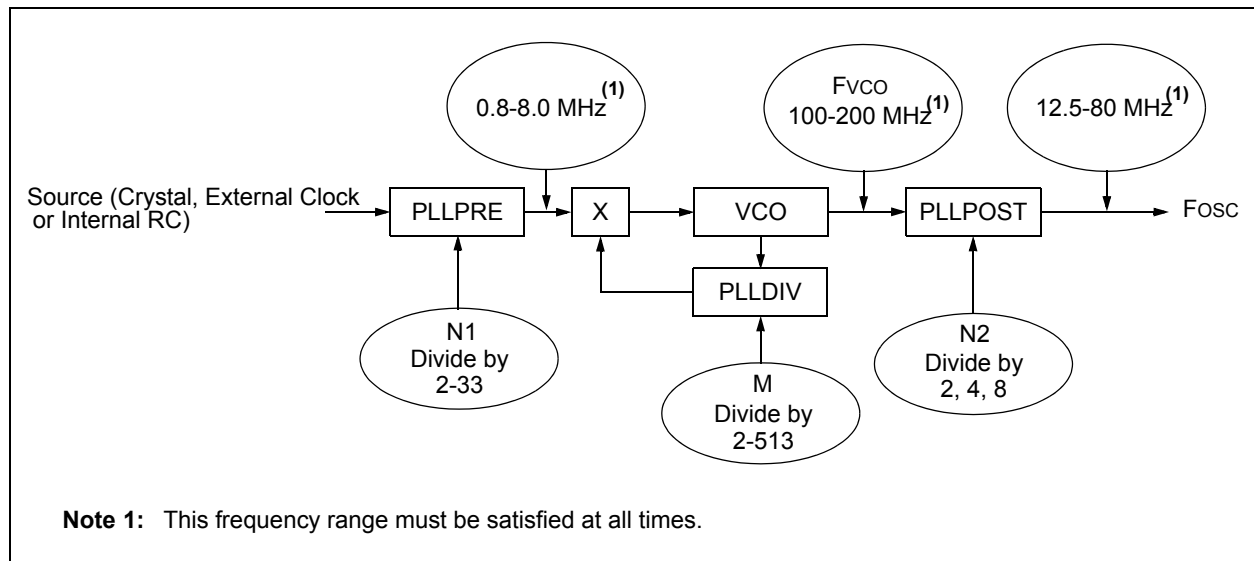
For example, suppose a 10 MHz crystal is being used with the selected oscillator mode of XT with PLL.

- If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 10/2 = 5 MHz, which is within the acceptable range of 0.8-8 MHz.
- If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 x 32 = 160 MHz, which is within the 100-200 MHz range needed.
- If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.

EQUATION 9-3: XT WITH PLL MODE EXAMPLE

$$F_{CY} = \frac{F_{OSC}}{2} = \frac{1}{2} \left(\frac{10000000 \cdot 32}{2 \cdot 2} \right) = 40 \text{ MIPS}$$

FIGURE 9-2: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 PLL BLOCK DIAGRAM



12.1 Timer Resources

Many useful resources related to Timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315
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12.1.1 KEY RESOURCES

- **Section 11. “Timers”** (DS70205)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

14.2 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER (x = 1, 2, 7 OR 8)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15			bit 8				

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
 1 = Input capture module halts in CPU Idle mode
 0 = Input capture module continues to operate in CPU Idle mode
- bit 12-8 **Unimplemented:** Read as '0'
- bit 7 **ICTMR:** Input Capture Timer Select bits
 1 = TMR2 contents are captured on capture event
 0 = TMR3 contents are captured on capture event
- bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event
- bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture overflow occurred
 0 = No input capture overflow occurred
- bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty
- bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode
 (Rising edge detect only, all other control bits are not applicable)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge
 100 = Capture mode, every 4th rising edge
 011 = Capture mode, every rising edge
 010 = Capture mode, every falling edge
 001 = Capture mode, every edge (rising and falling)
 (ICI<1:0> bits do not control interrupt generation for this mode)
 000 = Input capture module turned off

REGISTER 19-7: CIINTE: ECAN™ INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:	C = Writeable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled
- bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

21.3 Comparator Voltage Reference

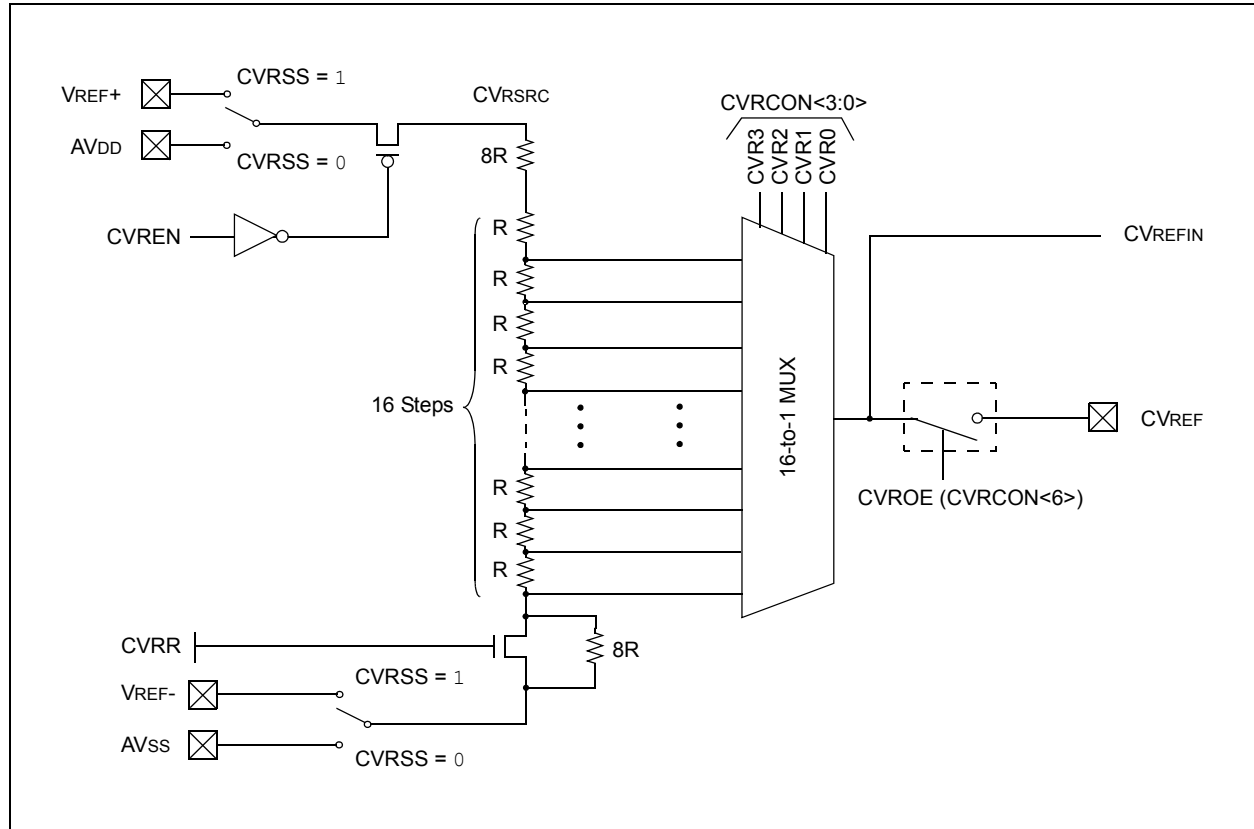
21.3.1 CONFIGURING THE COMPARATOR VOLTAGE REFERENCE

The Voltage Reference module is controlled through the CVRCON register ([Register 21-2](#)). The comparator voltage reference provides two ranges of output voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF Selection bits (CVR3:CVR0), with one range offering finer resolution.

The comparator reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<4>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 21-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



22.3 RTCC Registers

REGISTER 22-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR<1:0>	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL<7:0>							
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
 1 = RTCC module is enabled
 0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
 1 = RTCVALH and RTCVALL registers can be written to by the user
 0 = RTCVALH and RTCVALL registers are locked out from being written to by the user
- bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
 1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid
 0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple
- bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾
 1 = Second half period of a second
 0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
 1 = RTCC output enabled
 0 = RTCC output disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
 Points to the corresponding RTCC Value registers when reading RTCVALH and RTCVALL registers; the RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
RTCVAL<15:8>:
 11 = Reserved
 10 = MONTH
 01 = WEEKDAY
 00 = MINUTES
RTCVAL<7:0>:
 11 = YEAR
 10 = DAY
 01 = HOURS
 00 = SECONDS

Note 1: The RCFGAL register is only affected by a POR.

Note 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

Note 3: This bit is read-only. It is cleared to '0' on a write to the lower half of the MINSEC register.

23.4 Programmable CRC Resources

Many useful resources related to Programmable CRC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555
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23.4.1 KEY RESOURCES

- **Section 36. “Programmable Cyclic Redundancy Check CRC)”** (DS70298)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

TABLE 28-5: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units	Conditions	
Operating Current (I _{DD}) ⁽¹⁾					
DC20d	18	21	mA	-40°C	3.3V 10 MIPS
DC20a	18	22	mA	+25°C	
DC20b	18	22	mA	+85°C	
DC20c	18	25	mA	+125°C	
DC21d	30	35	mA	-40°C	3.3V 16 MIPS
DC21a	30	34	mA	+25°C	
DC21b	30	34	mA	+85°C	
DC21c	30	36	mA	+125°C	
DC22d	34	42	mA	-40°C	3.3V 20 MIPS
DC22a	34	41	mA	+25°C	
DC22b	34	42	mA	+85°C	
DC22c	35	44	mA	+125°C	
DC23d	49	58	mA	-40°C	3.3V 30 MIPS
DC23a	49	57	mA	+25°C	
DC23b	49	57	mA	+85°C	
DC23c	49	60	mA	+125°C	
DC24d	63	75	mA	-40°C	3.3V 40 MIPS
DC24a	63	74	mA	+25°C	
DC24b	63	74	mA	+85°C	
DC24c	63	76	mA	+125°C	

Note 1: I_{DD} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DD} measurements are as follows:

- Oscillator is configured in EC mode, no PLL until 10 MIPS, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = \text{V}_{\text{DD}}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero)
- CPU executing `while(1)` statement
- JTAG is disabled

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: These parameters are characterized but not tested in manufacturing.

28.2 AC Characteristics and Timing Parameters

This section defines PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 AC characteristics and timing parameters.

TABLE 28-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Operating voltage V_{DD} range as described in Table 28-1 .
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FIGURE 28-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

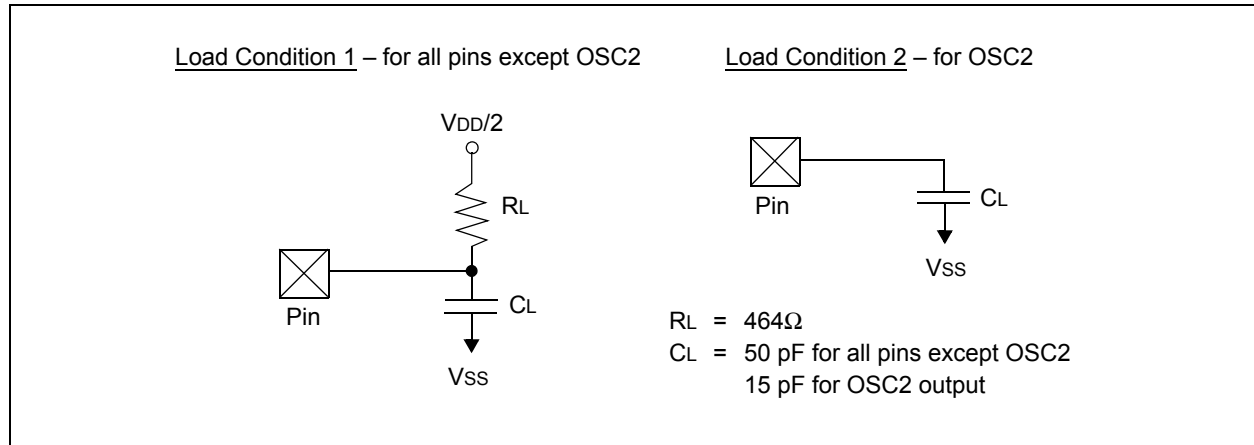


TABLE 28-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO50	Cosc2	OSC2/SOSC2 pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Cio	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	Cb	SCLx, SDAx	—	—	400	pF	In I ² C™ mode

FIGURE 28-3: CLKO AND I/O TIMING CHARACTERISTICS

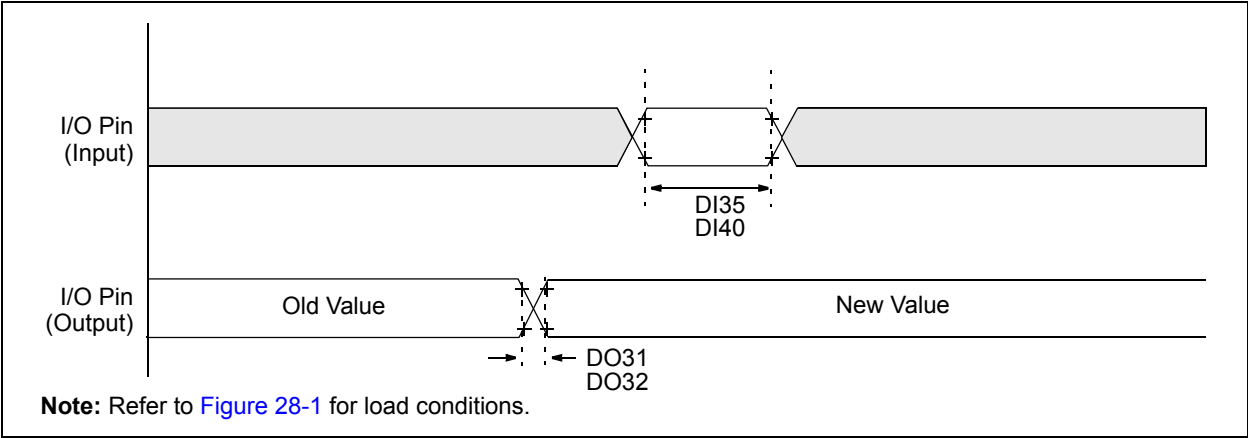


TABLE 28-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	—
DO32	TioF	Port Output Fall Time	—	10	25	ns	—
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TcY	—

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

TABLE 29-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-bit Mode) – Measurements with External VREF+/VREF-⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 data bits			bits	—
HAD21b	INL	Integral Nonlinearity	-3	—	3	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22b	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23b	GERR	Gain Error	-5	—	6	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24b	EOFF	Offset Error	-1	—	5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
ADC Accuracy (10-bit Mode) – Measurements with Internal VREF+/VREF-⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 data bits			bits	—
HAD21b	INL	Integral Nonlinearity	-2	—	2	LSb	V _{INL} = AV _{SS} = 0V, AV _{DD} = 3.6V
HAD22b	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	V _{INL} = AV _{SS} = 0V, AV _{DD} = 3.6V
HAD23b	GERR	Gain Error	-5	—	15	LSb	V _{INL} = AV _{SS} = 0V, AV _{DD} = 3.6V
HAD24b	EOFF	Offset Error	-1.5	—	7	LSb	V _{INL} = AV _{SS} = 0V, AV _{DD} = 3.6V
Dynamic Performance (10-bit Mode)⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	—

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

NOTES:

Peripheral Module Disable (PMD)	130
Pinout I/O Descriptions	11
PMD Module	
Register Map.....	46
PORTA	
Register Map.....	44, 45
PORTB	
Register Map.....	45
Power-on Reset (POR)	65
Power-Saving Features	129
Clock Frequency and Switching.....	129
Program Address Space	25
Construction.....	49
Data Access from Program Memory	
Using Program Space Visibility.....	52
Data Access from Program Memory	
Using Table Instructions	51
Data Access from, Address Generation.....	50
Memory Map	25
Table Read Instructions	
TBLRDH	51
TBLRDL	51
Visibility Operation	52
Program Memory	
Interrupt Vector	26
Organization	26
Reset Vector	26

R

Reader Response	388
Register Map	
CRC	44
Dual Comparator.....	44
Parallel Master/Slave Port	43
Real-Time Clock and Calendar.....	44
Registers	
AD1CHS0 (ADC1 Input Channel 0 Select)	238
AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select)	237
AD1CON1 (ADC1 Control 1)	232
AD1CON2 (ADC1 Control 2)	234
AD1CON3 (ADC1 Control 3)	235
AD1CON4 (ADC1 Control 4)	236
AD1CSSL (ADC1 Input Scan Select Low)	239
AD1PCFGL (ADC1 Port Configuration Low)	239
CiBUFNT1 (ECAN Filter 0-3 Buffer Pointer).....	213
CiBUFNT2 (ECAN Filter 4-7 Buffer Pointer).....	214
CiBUFNT3 (ECAN Filter 8-11 Buffer Pointer).....	214
CiBUFNT4 (ECAN Filter 12-15 Buffer Pointer).....	215
CiCFG1 (ECAN Baud Rate Configuration 1)	211
CiCFG2 (ECAN Baud Rate Configuration 2)	212
CiCTRL1 (ECAN Control 1)	204
CiCTRL2 (ECAN Control 2)	205
CiEC (ECAN Transmit/Receive Error Count).....	211
CiFCTRL (ECAN FIFO Control).....	207
CiFEN1 (ECAN Acceptance Filter Enable)	213
CiFIFO (ECAN FIFO Status).....	208
CiFMSKSEL1 (ECAN Filter 7-0 Mask Selection).....	217, 218
CiINTE (ECAN Interrupt Enable)	210
CiINTF (ECAN Interrupt Flag).....	209
CiRXFnEID (ECAN Acceptance Filter n	
Extended Identifier).....	217
CiRXFnSID (ECAN Acceptance Filter n	
Standard Identifier)	216
CiRXFUL1 (ECAN Receive Buffer Full 1)	220
CiRXFUL2 (ECAN Receive Buffer Full 2)	220
CiRXMnEID (ECAN Acceptance Filter Mask n	

Extended Identifier)	219
CiRXMnSID (ECAN Acceptance Filter Mask n	
Standard Identifier).....	219
CiRXOVF1 (ECAN Receive Buffer Overflow 1).....	221
CiRXOVF2 (ECAN Receive Buffer Overflow 2).....	221
CiTRBnSID (ECAN Buffer n Standard Identifier).....	223, 224, 226
CiTRmnCON (ECAN TX/RX Buffer m Control)	222
CiVEC (ECAN Interrupt Code)	206
CLKDIV (Clock Divisor)	125
CORCON (Core Control).....	22, 74
DMACS0 (DMA Controller Status 0)	114
DMACS1 (DMA Controller Status 1)	116
DMAxCNT (DMA Channel x Transfer Count).....	113
DMAxCON (DMA Channel x Control).....	110
DMAxPAD (DMA Channel x Peripheral Address)	113
DMAxREQ (DMA Channel x IRQ Select).....	111
DMAxSTA (DMA Channel x RAM Start Address A) .	112
DMAxSTB (DMA Channel x RAM Start Address B) .	112
DSADR (Most Recent DMA RAM Address)	117
I2CxCON (I2Cx Control).....	188
I2CxMSK (I2Cx Slave Mode Address Mask).....	192
I2CxSTAT (I2Cx Status)	190
IFS0 (Interrupt Flag Status 0)	77, 84
IFS1 (Interrupt Flag Status 1)	79, 86
IFS2 (Interrupt Flag Status 2)	81, 88
IFS3 (Interrupt Flag Status 3)	82, 89
IFS4 (Interrupt Flag Status 4)	83, 90
INTCON1 (Interrupt Control 1)	75
INTCON2 (Interrupt Control 2)	76
INTTREG Interrupt Control and Status Register	105
IPC0 (Interrupt Priority Control 0).....	91
IPC1 (Interrupt Priority Control 1).....	92
IPC11 (Interrupt Priority Control 11).....	101
IPC15 (Interrupt Priority Control 15).....	102
IPC16 (Interrupt Priority Control 16).....	103
IPC17 (Interrupt Priority Control 17).....	104
IPC2 (Interrupt Priority Control 2).....	93
IPC3 (Interrupt Priority Control 3).....	94
IPC4 (Interrupt Priority Control 4).....	95
IPC5 (Interrupt Priority Control 5).....	96
IPC6 (Interrupt Priority Control 6).....	97
IPC7 (Interrupt Priority Control 7).....	98
IPC8 (Interrupt Priority Control 8).....	99
IPC9 (Interrupt Priority Control 9).....	100
NVMCON (Flash Memory Control).....	55
NVMKEY (Nonvolatile Memory Key)	56
OCxCON (Output Compare x Control)	178
OSCCON (Oscillator Control).....	123
OSCTUN (FRC Oscillator Tuning).....	127
PLLFBD (PLL Feedback Divisor)	126
PMD1 (Peripheral Module Disable	
Control Register 1)	132
PMD2 (Peripheral Module Disable	
Control Register 2)	133
PMD3 (Peripheral Module Disable	
Control Register 3)	134
RCON (Reset Control).....	61
SPIxCON1 (SPIx Control 1)	182
SPIxCON2 (SPIx Control 2)	184
SPIxSTAT (SPIx Status and Control)	181
SR (CPU Status)	21, 74
T1CON (Timer1 Control)	163
TCxCON (Input Capture x Control)	173
TxCON (Type B Time Base Control)	168
TyCON (Type C Time Base Control).....	169
UxMODE (UARTx Mode)	195