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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp502t-i-so

TABLE 4-28: PORTA REGISTER MAP FOR PIC24HJ128GP204/504, PIC24HJ64GP204/504 AND PIC24HJ32GP304

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	02C2	—	—	—	—	—	RA10	RA9	RA8	RA7	—	—	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	02C4	—	—	—	—	—	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
ODCA	02C6	—	—	—	—	—	ODCA10	ODCA9	ODCA8	ODCA7	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: PORTB REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	02CE	—	—	—	—	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PORTC REGISTER MAP FOR PIC24HJ128GP204/504, PIC24HJ64GP204/504 AND PIC24HJ32GP304

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0	—	—	—	—	—	—	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	02D2	—	—	—	—	—	—	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	02D4	—	—	—	—	—	—	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	02D6	—	—	—	—	—	—	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: SYSTEM CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx[1]
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN	0300[2]
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values dependent on type of Reset.
2: OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

4.6.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The `TBLRDL` and `TBLWTL` instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The `TBLRDH` and `TBLWTH` instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. `TBLRDL` and `TBLWTL` access the space that contains the least significant data word. `TBLRDH` and `TBLWTH` access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- `TBLRDL` (Table Read Low):
  - In Word mode, this instruction maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- `TBLRDH` (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>), is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address, in the `TBLRDL` instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

Similarly, two table instructions, `TBLWTH` and `TBLWTL`, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

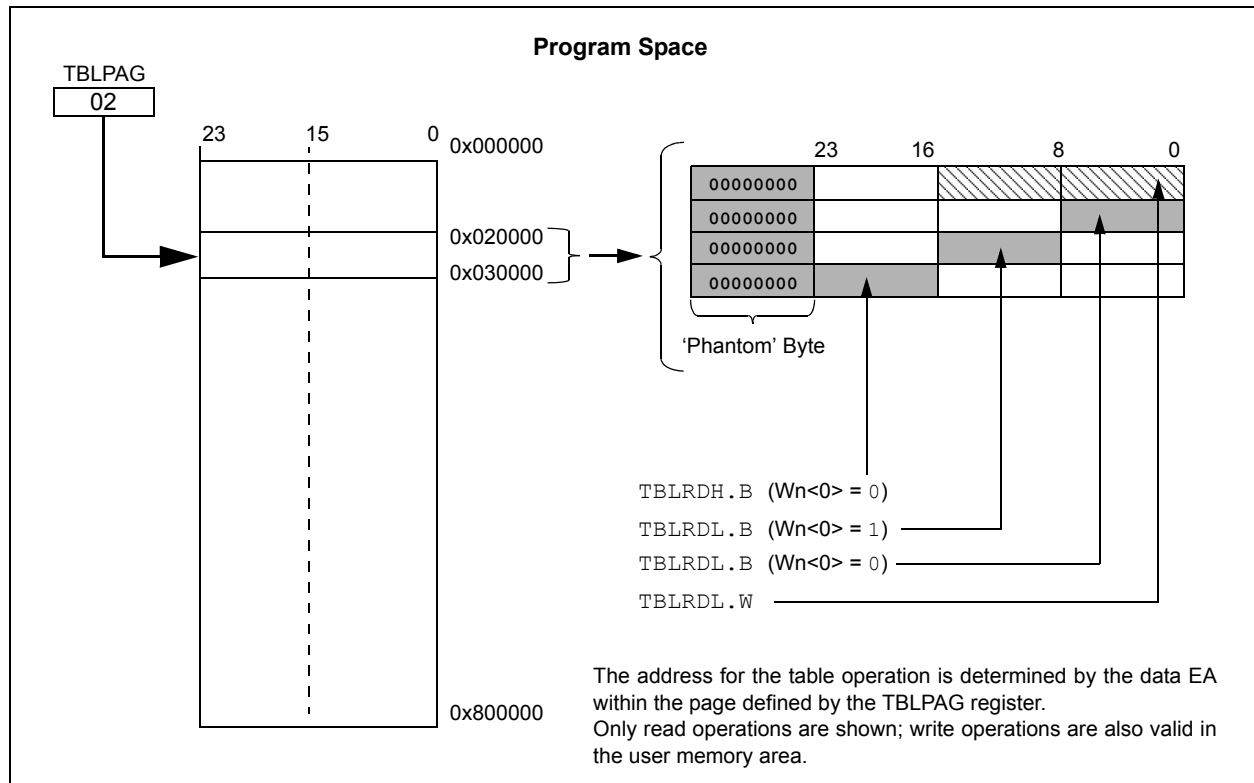**FIGURE 4-7:   ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**

The address for the table operation is determined by the data EA within the page defined by the TBLPAG register.
Only read operations are shown; write operations are also valid in the user memory area.

TABLE 7-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	IVT Address	AIVT Address	Interrupt Source
55-68	0x000072-0x00008C	0x000172-0x00018C	Reserved
69	0x00008E	0x00018E	DMA5 – DMA Channel 5
70	0x000090	0x000190	RTCC – Real Time Clock
71-72	0x000092-0x000094	0x000192-0x000194	Reserved
73	0x000096	0x000196	U1E – UART1 Error
74	0x000098	0x000198	U2E – UART2 Error
75	0x00009A	0x00019A	CRC – CRC Generator Interrupt
76	0x00009C	0x00019C	DMA6 – DMA Channel 6
77	0x00009E	0x00019E	DMA7 – DMA Channel 7
78	0x0000A0	0x0001A0	C1TX – ECAN1 TX Data Request
79-126	0x0000A2-0x0000FE	0x0001A2-0x0001FE	Reserved

REGISTER 7-21:   IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T4IP<2:0>			—	OC4IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	OC3IP<2:0>			—	DMA2IP<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **T4IP<2:0>:** Timer4 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **OC4IP<2:0>:** Output Compare Channel 4 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **OC3IP<2:0>:** Output Compare Channel 3 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **DMA2IP<2:0>:** DMA Channel 2 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

REGISTER 7-23:   IPC8: INTERRUPT PRIORITY CONTROL REGISTER 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	C1IP<2:0>[1]			—	C1RXIP<2:0>[1]		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI2IP<2:0>			—	SPI2EIP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **C1IP<2:0>:** ECAN1 Event Interrupt Priority bits[1]

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **C1RXIP<2:0>:** ECAN1 Receive Data Ready Interrupt Priority bits[1]

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **SPI2IP<2:0>:** SPI2 Event Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **SPI2EIP<2:0>:** SPI2 Error Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1:   Interrupts disabled on devices without ECAN™ modules.

REGISTER 7-27: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CRCIP<2:0>			—	U2EIP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1EIP<2:0>			—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CRCIP<2:0>:** CRC Generator Error Interrupt Flag Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U2EIP<2:0>:** UART2 Error Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U1EIP<2:0>:** UART1 Error Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

10.0 POWER-SAVING FEATURES

> **Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices can manage power consumption in four ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

> **Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake up.

10.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: **PWRSAV INSTRUCTION SYNTAX**

```
PWRSAV  #SLEEP_MODE     ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE      ; Put the device into IDLE mode
```

11.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24H devices include three features to prevent alterations to the peripheral map:

• Control register lock sequence
• Continuous state monitoring
• Configuration bit pin select lock

11.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) the IOLOCK bit as a single operation.

> **Note:** MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:
>
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
>
> See MPLAB Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

11.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset is triggered.

11.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY Configuration bit (FOSC<5>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T3CKR<4:0>				

bit 15   bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T2CKR<4:0>				

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **Unimplemented:** Read as '0'

bit 12-8   **T3CKR<4:0>:** Assign Timer3 External Clock (T3CK) to the corresponding RPn pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5   **Unimplemented:** Read as '0'

bit 4-0   **T2CKR<4:0>:** Assign Timer2 External Clock (T2CK) to the corresponding RPn pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

12.1   Timer Resources

Many useful resources related to Timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:**   In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en532315

12.1.1   KEY RESOURCES

- **Section 11. "Timers"** (DS70205)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 19-5:   CiFIFO: ECAN™ FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP<5:0>					
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB<5:0>					
bit 7							bit 0

Legend:		C = Writable bit, but only '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **FBP<5:0>:** FIFO Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

REGISTER 20-1:   AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 3   **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS<1:0> = `01` or `1x`)

When AD12B = `1`, SIMSAM is: U-0, Unimplemented, Read as '0'
`1` = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = `1x`); or
Samples CH0 and CH1 simultaneously (when CHPS<1:0> = `01`)
`0` = Samples multiple channels individually in sequence

bit 2   **ASAM:** ADC Sample Auto-Start bit

`1` = Sampling begins immediately after last conversion. SAMP bit is auto-set
`0` = Sampling begins when SAMP bit is set

bit 1   **SAMP:** ADC Sample Enable bit

`1` = ADC sample/hold amplifiers are sampling
`0` = ADC sample/hold amplifiers are holding
If ASAM = `0`, software can write '1' to begin sampling. Automatically set by hardware if ASAM = `1`.
If SSRC = `000`, software can write '0' to end sampling and start conversion. If SSRC ≠ `000`,
automatically cleared by hardware to end sampling and start conversion.

bit 0   **DONE:** ADC Conversion Status bit

`1` = ADC conversion cycle is completed
`0` = ADC conversion not started or in progress
Automatically set by hardware when ADC conversion is complete. Software can write '0' to clear
DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in
progress. Automatically cleared by hardware at start of a new conversion.

REGISTER 22-6: RTCVAL (WHEN RTCPTR<1:0> = 01): WKDYHR: WEEKDAY AND HOURS VALUE REGISTER[(1)]

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—		WDAY<2:0>	
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN<1:0>		HRONE<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'
bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; contains a value from 0 to 6
bit 7-6 **Unimplemented:** Read as '0'
bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit; contains a value from 0 to 2
bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit; contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 22-7: RTCVAL (WHEN RTCPTR<1:0> = 00): MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN<2:0>			MINONE<3:0>			
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN<2:0>			SECONE<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'
bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit; contains a value from 0 to 5
bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit; contains a value from 0 to 9
bit 7 **Unimplemented:** Read as '0'
bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit; contains a value from 0 to 5
bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit; contains a value from 0 to 9

TABLE 25-2: PIC24H CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection 1 = Boot segment can be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size X11 = No Boot program Flash segment Boot space is 1K Instruction Words (except interrupt vectors) 110 = Standard security; boot program Flash segment ends at 0x0007FE 010 = High security; boot program Flash segment ends at 0x0007FE Boot space is 4K Instruction Words (except interrupt vectors) 101 = Standard security; boot program Flash segment, ends at 0x001FFE 001 = High security; boot program Flash segment ends at 0x001FFE Boot space is 8K Instruction Words (except interrupt vectors) 100 = Standard security; boot program Flash segment ends at 0x003FFE 000 = High security; boot program Flash segment ends at 0x003FFE
RBS<1:0>[1]	FBS	Immediate	Boot Segment RAM Code Protection Size 11 = No Boot RAM defined 10 = Boot RAM is 128 bytes 01 = Boot RAM is 256 bytes 00 = Boot RAM is 1024 bytes
SWRP[1]	FSS[1]	Immediate	Secure Segment Program Flash Write-Protect bit 1 = Secure Segment can bet written 0 = Secure Segment is write-protected
SSS<2:0>[1]	FSS[1]	Immediate	Secure Segment Program Flash Code Protection Size **(Secure segment is not implemented on 32K devices)** X11 = No Secure program flash segment Secure space is 4K IW less BS 110 = Standard security; secure program flash segment starts at End of BS, ends at 0x001FFE 010 = High security; secure program flash segment starts at End of BS, ends at 0x001FFE Secure space is 8K IW less BS 101 = Standard security; secure program flash segment starts at End of BS, ends at 0x003FFE 001 = High security; secure program flash segment starts at End of BS, ends at 0x003FFE Secure space is 16K IW less BS 100 = Standard security; secure program flash segment starts at End of BS, ends at 007FFEh 000 = High security; secure program flash segment starts at End of BS, ends at 0x007FFE

Note 1: This Configuration register is not available on PIC24HJ32GP302/304 devices.

28.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 electrical characteristics. Additional information is provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings[1]

Ambient temperature under bias..-40°C to +125°C
Storage temperature .... -65°C to +160°C
Voltage on VDD with respect to VSS .... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS[4] .... -0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V[4] .... -0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V[4].. -0.3V to 3.6V
Maximum current out of VSS pin ....300 mA
Maximum current into VDD pin[2]...250 mA
Maximum current sourced/sunk by any 2x I/O pin[3] ....8 mA
Maximum current sourced/sunk by any 4x I/O pin[3] ....15 mA
Maximum current sourced/sunk by any 8x I/O pin[3] ....25 mA
Maximum current sunk by all ports ....200 mA
Maximum current sourced by all ports[2]..200 mA

> **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
>
> **2:** Maximum allowable current is a function of device maximum power dissipation (see Table 28-2).
>
> **3:** Exceptions are CLKOUT, which is able to sink/source 25 mA, and the VREF+, VREF-, SCLx, SDAx, PGECx and PGEDx pins, which are able to sink/source 12 mA.
>
> **4:** See the **"Pin Diagrams"** section for 5V tolerant pins.

FIGURE 28-17: **I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**

Note: Refer to Figure 28-1 for load conditions.
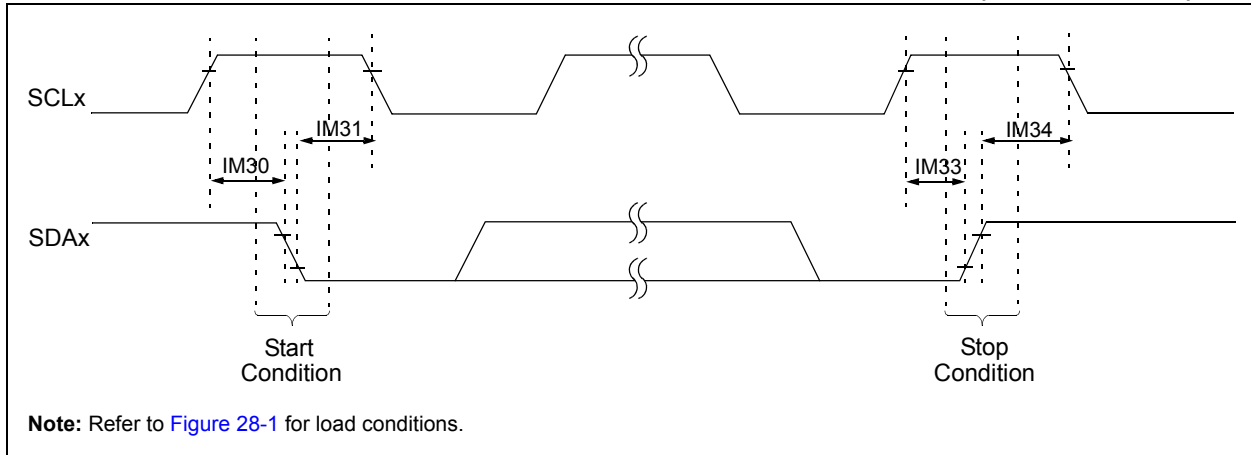
FIGURE 28-18: **I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

Note: Refer to Figure 28-1 for load conditions.
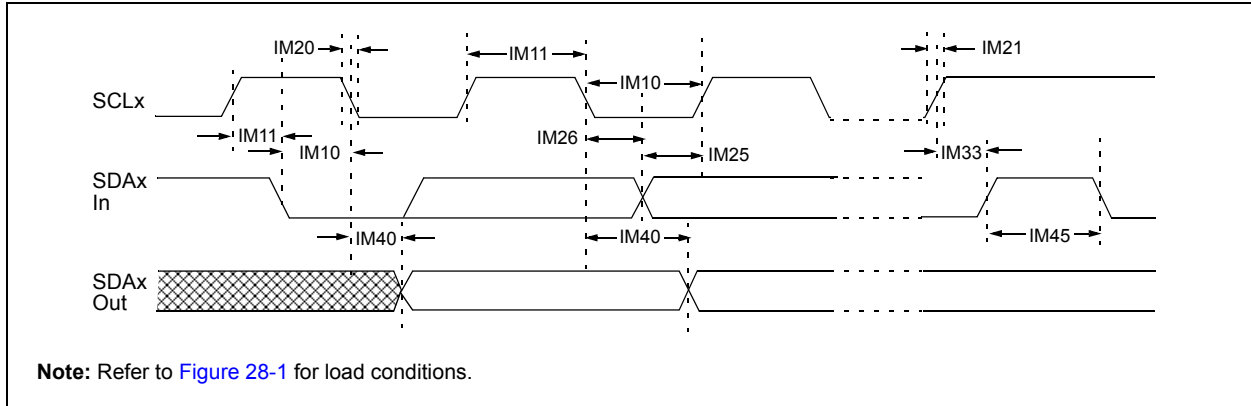
29.2   AC Characteristics and Timing Parameters

The information contained in this section defines PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 AC characteristics and timing parameters for high temperature devices. However, all AC timing specifications in this section are the same as those in **Section 28.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter OS53 in **Section 28.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 29-8:   TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤TA ≤+150°C for High Temperature Operating voltage VDD range as described in Table 29-1.

FIGURE 29-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

Load Condition 1 – for all pins except OSC2

Load Condition 2 – for OSC2

VDD/2

RL

Pin

CL

VSS

Pin

CL

VSS

RL = 464Ω
CL = 50 pF for all pins except OSC2
        15 pF for OSC2 output
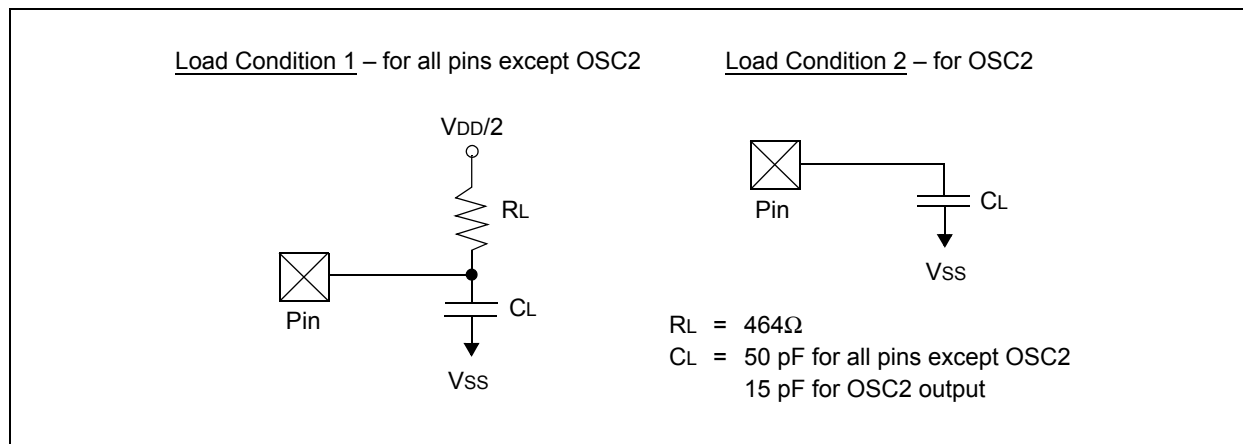
TABLE 29-9:   PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS		**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
HOS53	DCLK	CLKO Stability (Jitter)[1]	-5	0.5	5	%	Measured over 100 ms period

Note 1:   These parameters are characterized, but are not tested in manufacturing.

TABLE A-2:   MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 10.0 "Power-Saving Features"	Added the following registers: • PMD1: Peripheral Module Disable Control Register 1 (Register 10-1) • PMD2: Peripheral Module Disable Control Register 2 (Register 10-2) • PMD3: Peripheral Module Disable Control Register 3 (Register 10-3)
Section 11.0 "I/O Ports"	Removed Table 11-1 and added reference to pin diagrams for I/O pin availability and functionality. Added paragraph on ADPCFG register default values to **Section 11.3 "Configuring Analog Port Pins"**. Added Note box regarding PPS functionality with input mapping to **Section 11.6.2.1 "Input Mapping"**.
Section 16.0 "Serial Peripheral Interface (SPI)"	Added Note 2 and 3 to the SPIxCON1 register (see Register 16-2).
Section 18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the Notes in the UxMode register (see Register 18-1). Updated the UTXINV bit settings in the UxSTA register (see Register 18-2).
Section 19.0 "Enhanced CAN (ECAN™) Module"	Changed bit 11 in the ECAN Control Register 1 (CiCTRL1) to Reserved (see Register 19-1).
Section 20.0 "10-bit/12-bit Analog-to-Digital Converter (ADC1)"	Replaced the ADC1 Module Block Diagrams with new diagrams (see Figure 20-1 and Figure 20-2). Updated bit values for ADCS<7:0> and added Notes 1 and 2 to the ADC1 Control Register 3 (AD1CON3) (see Register 20-3). Added Note 2 to the ADC1 Input Scan Select Register Low (AD1CSSL) (see Register 20-7). Added Note 2 to the ADC1 Port Configuration Register Low (AD1PCFGL) (see Register 20-8).
Section 21.0 "Comparator Module"	Updated the Comparator Voltage Reference Block Diagram (see Figure 21-2).
Section 22.0 "Real-Time Clock and Calendar (RTCC)"	Updated the minimum positive adjust value for CAL<7:0> in the RTCC Calibration and Configuration (RCFGCAL) Register (see Register 22-1).
Section 25.0 "Special Features"	Added Note 1 to the Device Configuration Register Map (see Table 25-1). Updated Note 1 in the PIC24H Configuration Bits Description (see Table 25-2).

Revision D (November 2009)

The revision includes the following global update:

• Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-3:   MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Microcontrollers"	Added information on high temperature operation (see **"Operating Range:"**).
Section 11.0 "I/O Ports"	Changed the reference to digital-only pins to 5V tolerant pins in the second paragraph of **Section 11.2 "Open-Drain Configuration"**.
Section 18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the two baud rate range features to: 10 Mbps to 38 bps at 40 MIPS.
Section 20.0 "10-bit/12-bit Analog-to-Digital Converter (ADC1)"	Updated the ADC block diagrams (see Figure 20-1 and Figure 20-2).
Section 25.0 "Special Features"	Updated the second paragraph and removed the fourth paragraph in **Section 25.1 "Configuration Bits"**. Updated the Device Configuration Register Map (see Table 28-1).
Section 28.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4. Removed parameters DI26, DI28 and DI29 from the I/O Pin Input Specifications (see Table 28-9). Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Figure 28-12).
Section 29.0 "High Temperature Electrical Characteristics"	Added new chapter with high temperature specifications.
"Product Identification System"	Added the "H" definition for high temperature.