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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp504-h-ml

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “*dsPIC33F/PIC24H Family Reference Manual*”. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

This document contains device specific information for the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices.

[Figure 1-1](#) shows a general block diagram of the core and peripheral modules in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices.

[Table 1-1](#) lists the functions of the various pins shown in the pinout diagrams.

TABLE 4-18: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 (FOR PIC24HJ128GP502/504 AND PIC24HJ64GP502/504) (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF11EID	046E	EID<15:8>								EID<7:0>								xxxx	
C1RXF12SID	0470	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF12EID	0472	EID<15:8>								EID<7:0>								xxxx	
C1RXF13SID	0474	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF13EID	0476	EID<15:8>								EID<7:0>								xxxx	
C1RXF14SID	0478	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF14EID	047A	EID<15:8>								EID<7:0>								xxxx	
C1RXF15SID	047C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF15EID	047E	EID<15:8>								EID<7:0>								xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: PERIPHERAL PIN SELECT INPUT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	—	INT1R<4:0>					—	—	—	—	—	—	—	—	1F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	—	INT2R<4:0>					001F
RPINR3	0686	—	—	—	T3CKR<4:0>					—	—	—	T2CKR<4:0>					1F1F
RPINR4	0688	—	—	—	T5CKR<4:0>					—	—	—	T4CKR<4:0>					1F1F
RPINR7	068E	—	—	—	IC2R<4:0>					—	—	—	IC1R<4:0>					1F1F
RPINR10	0694	—	—	—	IC8R<4:0>					—	—	—	IC7R<4:0>					1F1F
RPINR11	0696	—	—	—	—	—	—	—	—	—	—	—	OCFAR<4:0>					001F
RPINR18	06A4	—	—	—	U1CTSR<4:0>					—	—	—	U1RXR<4:0>					1F1F
RPINR19	06A6	—	—	—	U2CTSR<4:0>					—	—	—	U2RXR<4:0>					1F1F
RPINR20	06A8	—	—	—	SCK1R<4:0>					—	—	—	SDI1R<4:0>					1F1F
RPINR21	06AA	—	—	—	—	—	—	—	—	—	—	—	SS1R<4:0>					001F
RPINR22	06AC	—	—	—	SCK2R<4:0>					—	—	—	SDI2R<4:0>					1F1F
RPINR23	06AE	—	—	—	—	—	—	—	—	—	—	—	SS2R<4:0>					001F
RPINR26 ⁽¹⁾	06B4	—	—	—	—	—	—	—	—	—	—	—	C1RXR<4:0>					001F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is present for PIC24HJ128GP502/504 and PIC24HJ64GP502/504 devices only.

TABLE 4-32: SECURITY REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
BSRAM	0750	—	—	—	—	—	—	—	—	—	—	—	—	—	IW_BSR	IR_BSR	RL_BSR	0000
SSRAM	0752	—	—	—	—	—	—	—	—	—	—	—	—	—	IW_SSR	IR_SSR	RL_SSR	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not present in devices with 32K Flash (PIC24HJ32GP302/304).

TABLE 4-33: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP<3:0>				0000
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	—	—	—	—	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDL** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The **TBLRDH** and **TBLWTH** instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. **TBLRDL** and **TBLWTL** access the space that contains the least significant data word. **TBLRDH** and **TBLWTH** access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- **TBLRDL** (Table Read Low):
 - In Word mode, this instruction maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$).

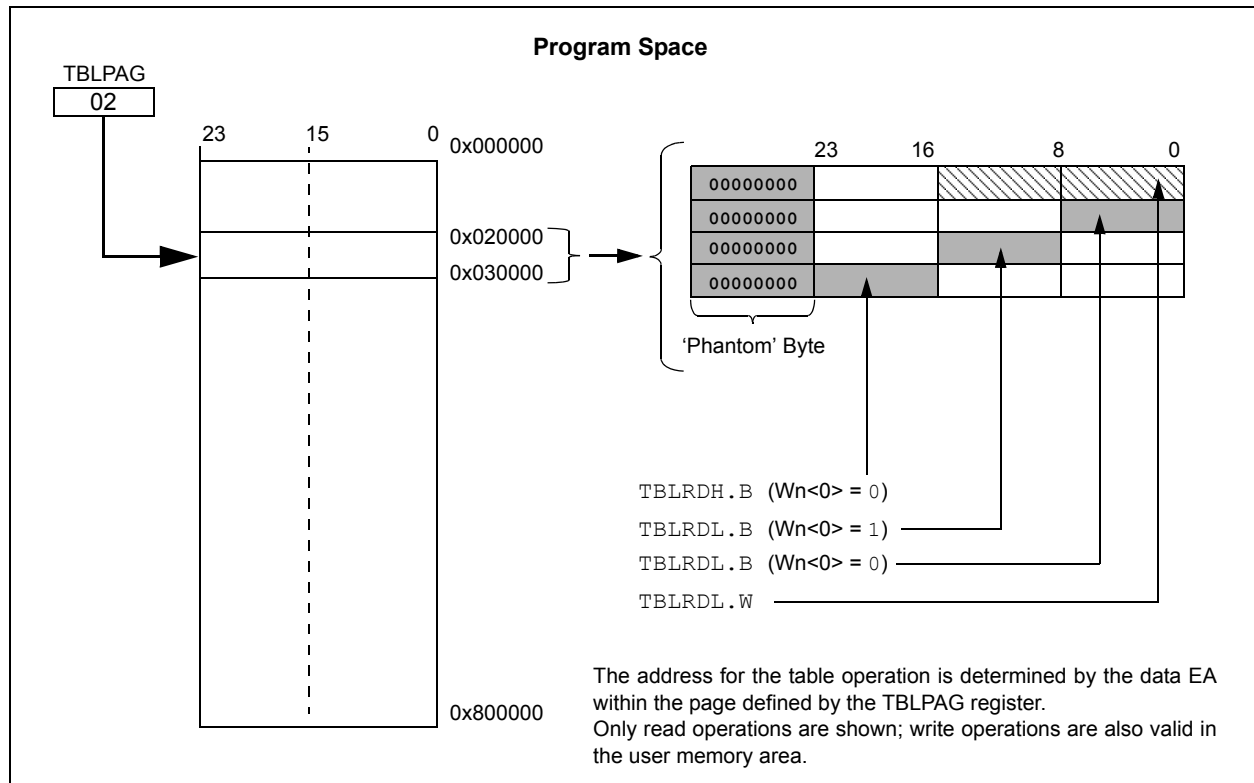
- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- **TBLRDH** (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. The 'phantom' byte ($D<15:8>$), is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address, in the **TBLRDL** instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

Similarly, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a program space address. The details of their operation are explained in [Section 5.0 "Flash Program Memory"](#).

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-7: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



7.3 Interrupt Control and Status Registers

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices implement a total of 30 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFSx
- IECx
- IPCx
- INTTREG

7.3.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

7.3.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.3.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.3.4 IPCx

The IPC registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.3.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number (VECNUM<6:0>) and Interrupt level (ILR<3:0>) bit fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in [Table 7-1](#). For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INTOIF bit is found in IFS0<0>, the INTOIE bit in IEC0<0>, and the INTOIP bits in the first position of IPC0 (IPC0<2:0>).

7.3.6 STATUS/CONTROL REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality.

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user software can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in [Register 7-1](#) through [Register 7-29](#).

7.4 Interrupt Resources

Many useful resources related Interrupts are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDoc-Name=en534555>

7.4.1 KEY RESOURCES

- **Section 32. “Interrupts (Part III)”** (DS70214)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

7.5 Interrupt Control Registers

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0> ⁽²⁾			RA	N	OV	Z	C
bit 7							bit 0

Legend:

C = Clear only bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Set only bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>**: CPU Interrupt Priority Level Status bits⁽²⁾

- 111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see [Register 3-1](#).

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽²⁾	PSV	—	—
bit 7							bit 0

Legend:

C = Clear only bit	R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
'0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'		

bit 3 **IPL3**: CPU Interrupt Priority Level Status bit 3⁽²⁾

- 1 = CPU interrupt priority level is greater than 7
- 0 = CPU interrupt priority level is 7 or less

Note 1: For complete register details, see [Register 3-2](#).

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit

1 = Use alternate vector table

0 = Use standard (default) vector table

bit 14 **DISI:** DISI Instruction Status bit

1 = DISI instruction is active

0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit

1 = Interrupt on negative edge

0 = Interrupt on positive edge

REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **DMA1IE:** DMA Channel 1 Data Transfer Complete Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 13 **AD1IE:** ADC1 Conversion Complete Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 10 **SPI1IE:** SPI1 Event Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 9 **SPI1EIE:** SPI1 Error Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 8 **T3IE:** Timer3 Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 7 **T2IE:** Timer2 Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 4 **DMA0IE:** DMA Channel 0 Data Transfer Complete Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled
- bit 3 **T1IE:** Timer1 Interrupt Enable bit
 1 = Interrupt request enabled
 0 = Interrupt request not enabled

REGISTER 7-22: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP<2:0>			—	U2RXIP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP<2:0>			—	T5IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **T5IP<2:0>:** Timer5 Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽²⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0> ⁽¹⁾					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽¹⁾

111111 = Center frequency -0.375% (7.345 MHz)

•

•

•

100001 = Center frequency -11.625% (6.52 MHz)

100000 = Center frequency -12% (6.49 MHz)

011111 = Center frequency +11.625% (8.23 MHz)

011110 = Center frequency +11.25% (8.20 MHz)

•

•

•

000001 = Center frequency +0.375% (7.40 MHz)

000000 = Center frequency (7.37 MHz nominal)

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.

2: This register is reset only on a Power-on Reset (POR).

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CMPMD	RTCCMD	PMPMD
bit 15					bit 8		

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
CRCMD	DAC1MD	—	—	—	—	—	—
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **CMPMD:** Comparator Module Disable bit
 1 = Comparator module is disabled
 0 = Comparator module is enabled
- bit 9 **RTCCMD:** RTCC Module Disable bit
 1 = RTCC module is disabled
 0 = RTCC module is enabled
- bit 8 **PMPMD:** PMP Module Disable bit
 1 = PMP module is disabled
 0 = PMP module is enabled
- bit 7 **CRCMD:** CRC Module Disable bit
 1 = CRC module is disabled
 0 = CRC module is enabled
- bit 6 **DAC1MD:** DAC1 Module Disable bit
 1 = DAC1 module is disabled
 0 = DAC1 module is enabled
- bit 5-0 **Unimplemented:** Read as '0'

REGISTER 11-9: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	U2CTSR<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	U2RXR<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **U2CTSR<4:0>:** Assign UART2 Clear to Send (U2CTS) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **U2RXR<4:0>:** Assign UART2 Receive (U2RX) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK2R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI2R<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK2R<4:0>:** Assign SPI2 Clock Input (SCK2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI2R<4:0>:** Assign SPI2 Data Input (SDI2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

REGISTER 19-5: CiFIFO: ECAN™ FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP<5:0>					
bit 15		bit 8					

REGISTER 21-1: CMCON: COMPARATOR CONTROL REGISTER (CONTINUED)

bit 6	C1OUT: Comparator 1 Output bit <u>When C1INV = 0:</u> 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN- <u>When C1INV = 1:</u> 0 = C1 VIN+ > C1 VIN- 1 = C1 VIN+ < C1 VIN-
bit 5	C2INV: Comparator 2 Output Inversion bit 1 = C2 output inverted 0 = C2 output not inverted
bit 4	C1INV: Comparator 1 Output Inversion bit 1 = C1 output inverted 0 = C1 output not inverted
bit 3	C2NEG: Comparator 2 Negative Input Configure bit 1 = Input is connected to VIN+ 0 = Input is connected to VIN- See Figure 21-1 for the comparator modes.
bit 2	C2POS: Comparator 2 Positive Input Configure bit 1 = Input is connected to VIN+ 0 = Input is connected to CVREF See Figure 21-1 for the comparator modes.
bit 1	C1NEG: Comparator 1 Negative Input Configure bit 1 = Input is connected to VIN+ 0 = Input is connected to VIN- See Figure 21-1 for the comparator modes.
bit 0	C1POS: Comparator 1 Positive Input Configure bit 1 = Input is connected to VIN+ 0 = Input is connected to CVREF See Figure 21-1 for the comparator modes.

- Note 1:** If C2OUTEN = 1, the C2OUT peripheral output must be configured to an available RPx pin. See [Section 11.6 “Peripheral Pin Select”](#) for more information.
- 2:** If C1OUTEN = 1, the C1OUT peripheral output must be configured to an available RPx pin. See [Section 11.6 “Peripheral Pin Select”](#) for more information.

22.1 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

22.1.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired timer register pair (see [Table 22-1](#)).

By writing the RTCVALH byte, the RTCC Pointer value, RTCPTR<1:0> bits, decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 22-1: RTCVAL REGISTER MAPPING

RTCPTR <1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR bits (ALCFGPRPT<9:8>) to select the desired Alarm register pair (see [Table 22-2](#)).

By writing the ALRMVALH byte, the Alarm Pointer value, ALRMPTR<1:0> bits, decrement by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

TABLE 22-2: ALRMVAL REGISTER MAPPING

ALRMPTR <1:0>	Alarm Value Register Window	
	ALRMVAL<15:8>	ALRMVAL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	—	—

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes will decrement the ALRMPTR<1:0> value. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations.

22.1.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (refer to [Example 22-1](#)).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only 1 instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that code follow the procedure in [Example 22-1](#).

EXAMPLE 22-1: SETTING THE RTCWREN BIT

```

MOV    #NVMKEY, W1      ;move the address of NVMKEY into W1
MOV    #0x55, W2
MOV    #0xAA, W3
MOV    W2, [W1]          ;start 55/AA sequence
MOV    W3, [W1]
BSET   RCFGCAL, #13      ;set the RTCWREN bit
    
```

REGISTER 23-2: CRCXOR: CRC XOR POLYNOMIAL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X<7:1>							—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **X<15:1>**: XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented**: Read as '0'

TABLE 28-5: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤TA ≤+125°C for Extended		
Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units	Conditions	
Operating Current (IDD) ⁽¹⁾					
DC20d	18	21	mA	-40°C	3.3V 10 MIPS
DC20a	18	22	mA	+25°C	
DC20b	18	22	mA	+85°C	
DC20c	18	25	mA	+125°C	
DC21d	30	35	mA	-40°C	3.3V 16 MIPS
DC21a	30	34	mA	+25°C	
DC21b	30	34	mA	+85°C	
DC21c	30	36	mA	+125°C	
DC22d	34	42	mA	-40°C	3.3V 20 MIPS
DC22a	34	41	mA	+25°C	
DC22b	34	42	mA	+85°C	
DC22c	35	44	mA	+125°C	
DC23d	49	58	mA	-40°C	3.3V 30 MIPS
DC23a	49	57	mA	+25°C	
DC23b	49	57	mA	+85°C	
DC23c	49	60	mA	+125°C	
DC24d	63	75	mA	-40°C	3.3V 40 MIPS
DC24a	63	74	mA	+25°C	
DC24b	63	74	mA	+85°C	
DC24c	63	76	mA	+125°C	

Note 1: I_{DD} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DD} measurements are as follows:

- Oscillator is configured in EC mode, no PLL until 10 MIPS, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = \text{V}_{\text{DD}}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero)
- CPU executing `while(1)` statement
- JTAG is disabled

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: These parameters are characterized but not tested in manufacturing.

TABLE 28-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No. ⁽³⁾	Typical ⁽²⁾	Max	Units	Conditions	
Power-Down Current (IPD) ⁽¹⁾					
DC60d	24	68	μA	-40°C	3.3V Base Power-Down Current ^(3,4)
DC60a	28	87	μA	+25°C	
DC60b	124	292	μA	+85°C	
DC60c	350	1000	μA	+125°C	
DC61d	8	13	μA	-40°C	3.3V Watchdog Timer Current: ΔI _{WDT} ^(3,5)
DC61a	10	15	μA	+25°C	
DC61b	12	20	μA	+85°C	
DC61c	13	25	μA	+125°C	

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off (i.e., Sleep mode), oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled, all peripheral modules are disabled (PMDx bits are all '1's)
- RTCC is disabled
- JTAG is disabled

2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The Watchdog Timer Current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

4: These currents are measured on the device containing the most memory in this family.

5: These parameters are characterized, but are not tested in manufacturing.

TABLE 28-28: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 28-29	—	—	0,1	0,1	0,1
9 MHz	—	Table 28-30	—	1	0,1	1
9 MHz	—	Table 28-31	—	0	0,1	1
15 MHz	—	—	Table 28-32	1	0	0
11 MHz	—	—	Table 28-33	1	1	0
15 MHz	—	—	Table 28-34	0	1	0
11 MHz	—	—	Table 28-35	0	0	0

FIGURE 28-9: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS

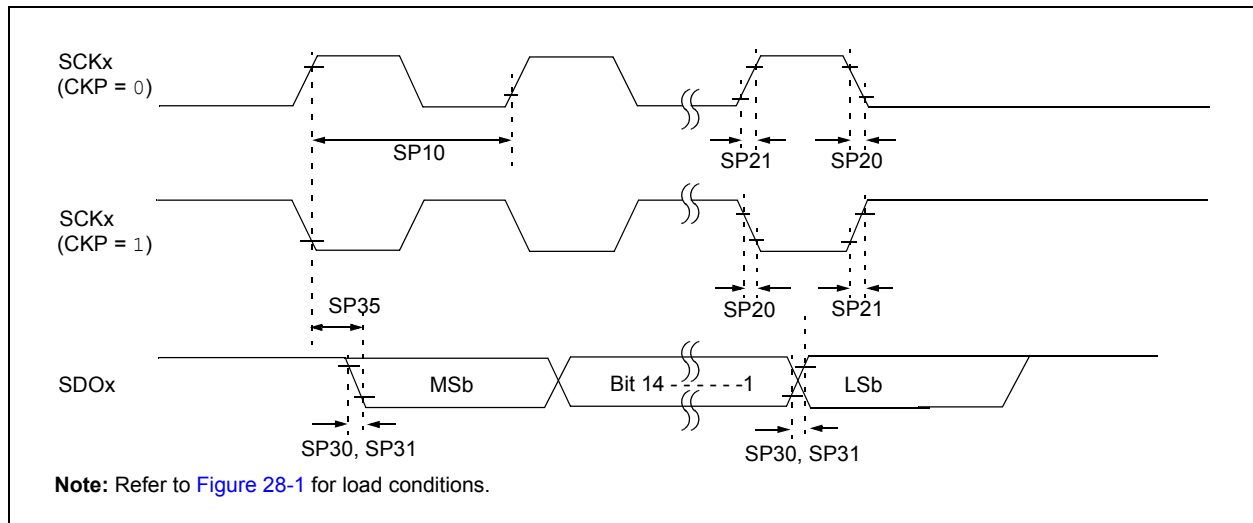


FIGURE 28-10: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS

