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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp504-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp504-i-pt</a>

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# PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

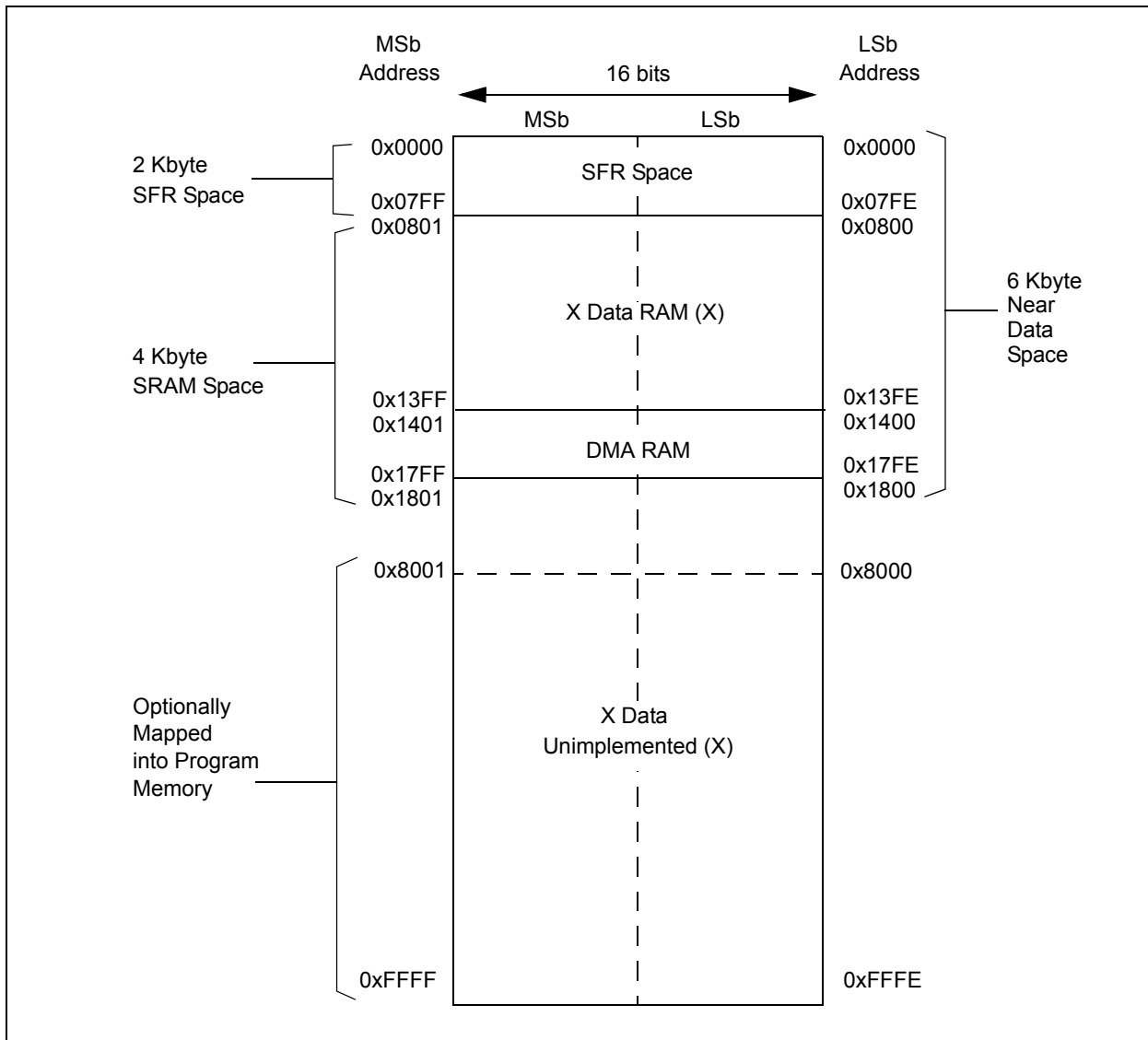
## 4.2.5 DMA RAM

The PIC24HJ32GP302/304 devices contain 1 Kbytes of dual ported DMA RAM located at the end of X data space. The PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices contain 2 Kbytes of dual ported DMA RAM located at the end of X data space, and is a part of X data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA controller module. DMA RAM is utilized by the DMA controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

**Note:** DMA RAM can be used for general purpose data storage if the DMA function is not required in an application.

**FIGURE 4-3: DATA MEMORY MAP FOR PIC24HJ32GP302/304 DEVICES WITH 4 KB RAM**



**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0088	—	DMA4IF	PMPIF	—	—	—	—	—	—	—	—	DMA3IF	C1IF <sup>(1)</sup>	C1RXIF <sup>(1)</sup>	SPI2IF	SPI2EIF	0000
IFS3	008A	—	RTCIF	DMA5IF	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	C1TXIF <sup>(1)</sup>	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	DMA4IE	PMPIE	—	—	—	—	—	—	—	—	DMA3IE	C1IE <sup>(1)</sup>	C1RXIE <sup>(1)</sup>	SPI2IE	SPI2EIE	0000
IEC3	009A	—	RTCIE	DMA5IE	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	C1TXIE <sup>(1)</sup>	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	00AC	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	IC8IP<2:0>			—	IC7IP<2:0>			—	—	—	—	—	INT1IP<2:0>			4404
IPC6	00B0	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	00B2	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	00B4	—	C1IP<2:0> <sup>(1)</sup>			—	C1RXIP<2:0> <sup>(1)</sup>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	00B6	—	—	—	—	—	—	—	—	—	—	—	—	—	DMA3IP<2:0>			0004
IPC11	00BA	—	—	—	—	—	DMA4IP<2:0>			—	PMPIP<2:0>			—	—	—	—	0440
IPC15	00C2	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	—	—	—	0440
IPC16	00C4	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	00C6	—	—	—	—	—	C1TXIP<2:0> <sup>(1)</sup>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			0444
INTTREG	00E0	—	—	—	—	—	ILR<3:0>			—	VECNUM<6:0>						4444	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Interrupts disabled on devices without ECAN™ modules.

TABLE 4-15: DMA REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA5PAD	03C4	PAD<15:0>																0000	
DMA5CNT	03C6	—	—	—	—	—	—	CNT<9:0>										0000	
DMA6CON	03C8	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA6REQ	03CA	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA6STA	03CC	STA<15:0>																0000	
DMA6STB	03CE	STB<15:0>																0000	
DMA6PAD	03D0	PAD<15:0>																0000	
DMA6CNT	03D2	—	—	—	—	—	—	CNT<9:0>										0000	
DMA7CON	03D4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA7REQ	03D6	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA7STA	03D8	STA<15:0>																0000	
DMA7STB	03DA	STB<15:0>																0000	
DMA7PAD	03DC	PAD<15:0>																0000	
DMA7CNT	03DE	—	—	—	—	—	—	CNT<9:0>										0000	
DMACS0	03E0	PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0	XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	0000	
DMACS1	03E2	—	—	—	—	LSTCH<3:0>				PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0	0000	
DSADR	03E4	DSADR<15:0>																0000	

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

## REGISTER 5-2: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8

**Unimplemented:** Read as '0'

bit 7-0

**NVMKEY<7:0>:** Key Register (write-only) bits

# PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04

## REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER<sup>(1)</sup>

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-9                      **Unimplemented:** Read as '0'  
 bit 8-0                      **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)  
                                     111111111 = 513  
                                     •  
                                     •  
                                     •  
                                     000110000 = 50 (default)  
                                     •  
                                     •  
                                     •  
                                     000000010 = 4  
                                     000000001 = 3  
                                     000000000 = 2

**Note 1:** This register is reset only on a Power-on Reset (POR).

**REGISTER 11-10: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20**

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK1R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI1R<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 15-13      **Unimplemented:** Read as '0'

bit 12-8      **SCK1R<4:0>:** Assign SPI1 Clock Input (SCK1) to the corresponding RPn pin

11111 = Input tied to Vss  
 11001 = Input tied to RP25

- 
- 
- 

00001 = Input tied to RP1  
 00000 = Input tied to RP0

bit 7-5      **Unimplemented:** Read as '0'

bit 4-0      **SDI1R<4:0>:** Assign SPI1 Data Input (SDI1) to the corresponding RPn pin

11111 = Input tied to Vss  
 11001 = Input tied to RP25

- 
- 
- 

00001 = Input tied to RP1  
 00000 = Input tied to RP0



**REGISTER 11-21: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTERS 6**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP13R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP12R<4:0>				
bit 7							bit 0

<b>Legend:</b>							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

- bit 15-13      **Unimplemented:** Read as '0'
- bit 12-8      **RP13R<4:0>:** Peripheral Output Function is Assigned to RP13 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)
- bit 7-5        **Unimplemented:** Read as '0'
- bit 4-0        **RP12R<4:0>:** Peripheral Output Function is Assigned to RP12 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

**REGISTER 11-22: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTERS 7**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP15R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP14R<4:0>				
bit 7							bit 0

<b>Legend:</b>							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

- bit 15-13      **Unimplemented:** Read as '0'
- bit 12-8      **RP15R<4:0>:** Peripheral Output Function is Assigned to RP15 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)
- bit 7-5        **Unimplemented:** Read as '0'
- bit 4-0        **RP14R<4:0>:** Peripheral Output Function is Assigned to RP14 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

### 13.0 TIMER2/3 AND TIMER4/5 FEATURE

**Note 1:** This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. “Timers”** (DS70205) of the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

- A Type B timer can be concatenated with a Type C timer to form a 32-bit timer
- The external clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of the Type B timer is shown in [Figure 13-1](#).

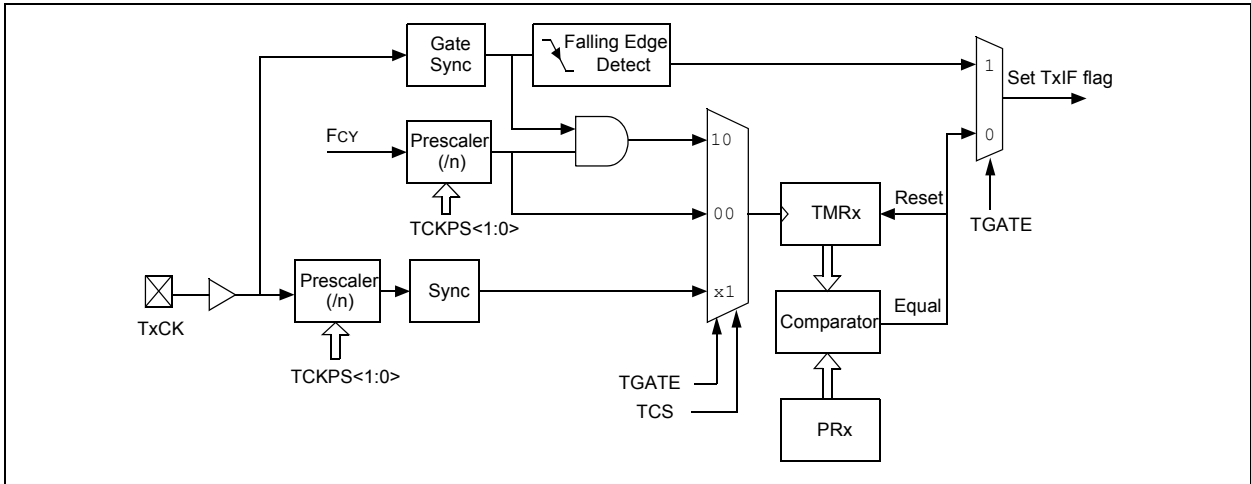
Timer3 and Timer5 are Type C timers with the following specific features:

- A Type C timer can be concatenated with a Type B timer to form a 32-bit timer
- At least one Type C timer has the ability to trigger an A/D conversion
- The external clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed before the prescaler

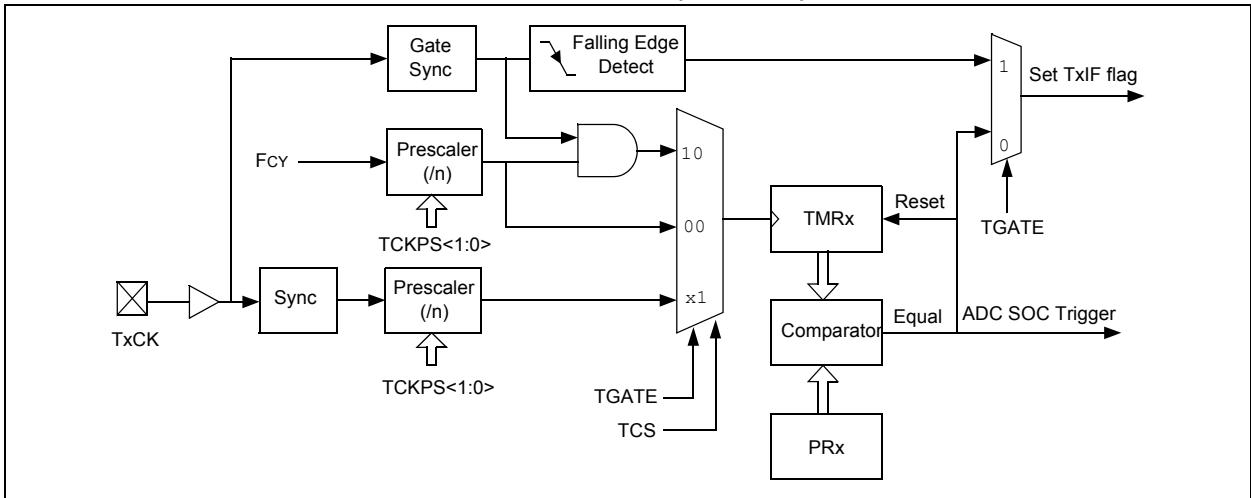
A block diagram of the Type C timer is shown in [Figure 13-2](#).

Timer2 and Timer4 are Type B timers with the following specific features:

**FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 or 4)**



**FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 or 5)**



**NOTES:**

**REGISTER 19-10: C1CFG2: ECAN™ BAUD RATE CONFIGURATION REGISTER 2**

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH<2:0>		
bit 15							bit 8

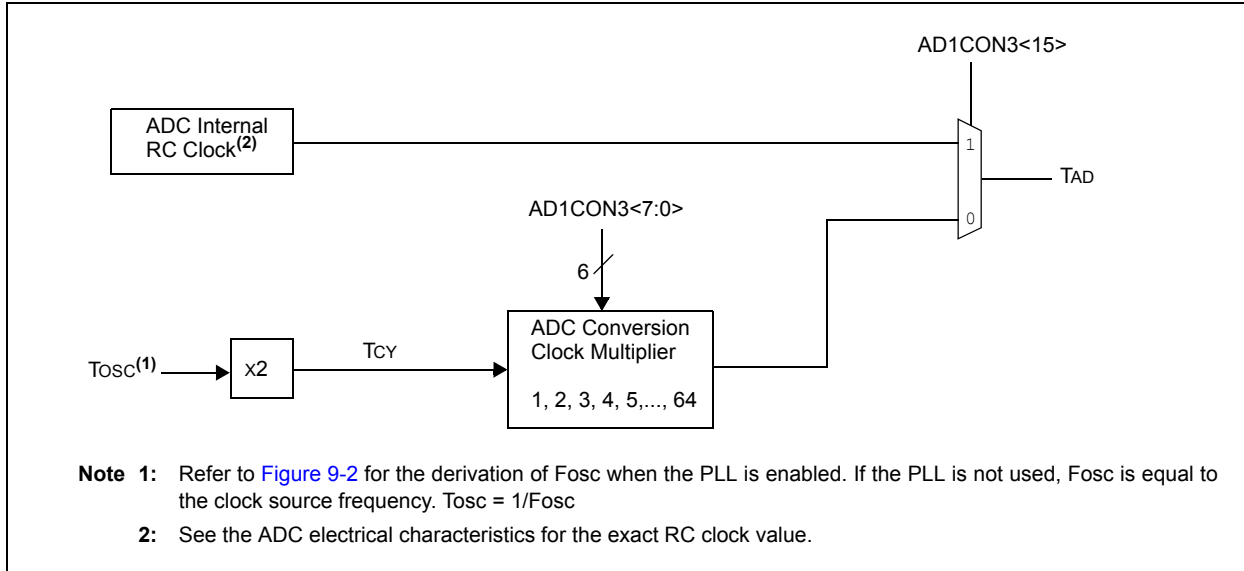
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>		
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15      **Unimplemented:** Read as '0'
- bit 14      **WAKFIL:** Select CAN bus Line Filter for Wake-up bit
  - 1 = Use CAN bus line filter for wake-up
  - 0 = CAN bus line filter is not used for wake-up
- bit 13-11   **Unimplemented:** Read as '0'
- bit 10-8    **SEG2PH<2:0>:** Phase Segment 2 bits
  - 111 = Length is 8 x T<sub>Q</sub>
  - 
  - 
  - 
  - 000 = Length is 1 x T<sub>Q</sub>
- bit 7        **SEG2PHTS:** Phase Segment 2 Time Select bit
  - 1 = Freely programmable
  - 0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater
- bit 6        **SAM:** Sample of the CAN bus Line bit
  - 1 = Bus line is sampled three times at the sample point
  - 0 = Bus line is sampled once at the sample point
- bit 5-3     **SEG1PH<2:0>:** Phase Segment 1 bits
  - 111 = Length is 8 x T<sub>Q</sub>
  - 
  - 
  - 
  - 000 = Length is 1 x T<sub>Q</sub>
- bit 2-0     **PRSEG<2:0>:** Propagation Time Segment bits
  - 111 = Length is 8 x T<sub>Q</sub>
  - 
  - 
  - 
  - 000 = Length is 1 x T<sub>Q</sub>

FIGURE 20-3: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



## 21.1 Comparator Resources

Many useful resources related to Comparators are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555>

### 21.1.1 KEY RESOURCES

- **Section 34. “Comparator”** (DS70212)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

TABLE 28-6: DC CHARACTERISTICS: IDLE CURRENT (IDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No. <sup>(3)</sup>	Typical <sup>(2)</sup>	Max	Units	Conditions	
<b>Idle Current (IDLE): Core OFF Clock ON Base Current<sup>(1)</sup></b>					
DC40d	8	10	mA	-40°C	3.3V 10 MIPS
DC40a	8	10	mA	+25°C	
DC40b	9	10	mA	+85°C	
DC40c	10	13	mA	+125°C	
DC41d	13	15	mA	-40°C	3.3V 16 MIPS
DC41a	13	15	mA	+25°C	
DC41b	13	16	mA	+85°C	
DC41c	13	19	mA	+125°C	
DC42d	15	18	mA	-40°C	3.3V 20 MIPS
DC42a	16	18	mA	+25°C	
DC42b	16	19	mA	+85°C	
DC42c	17	22	mA	+125°C	
DC43a	23	27	mA	+25°C	3.3V 30 MIPS
DC43d	23	26	mA	-40°C	
DC43b	24	28	mA	+85°C	
DC43c	25	31	mA	+125°C	
DC44d	31	42	mA	-40°C	3.3V 40 MIPS
DC44a	31	36	mA	+25°C	
DC44b	32	39	mA	+85°C	
DC44c	34	43	mA	+125°C	

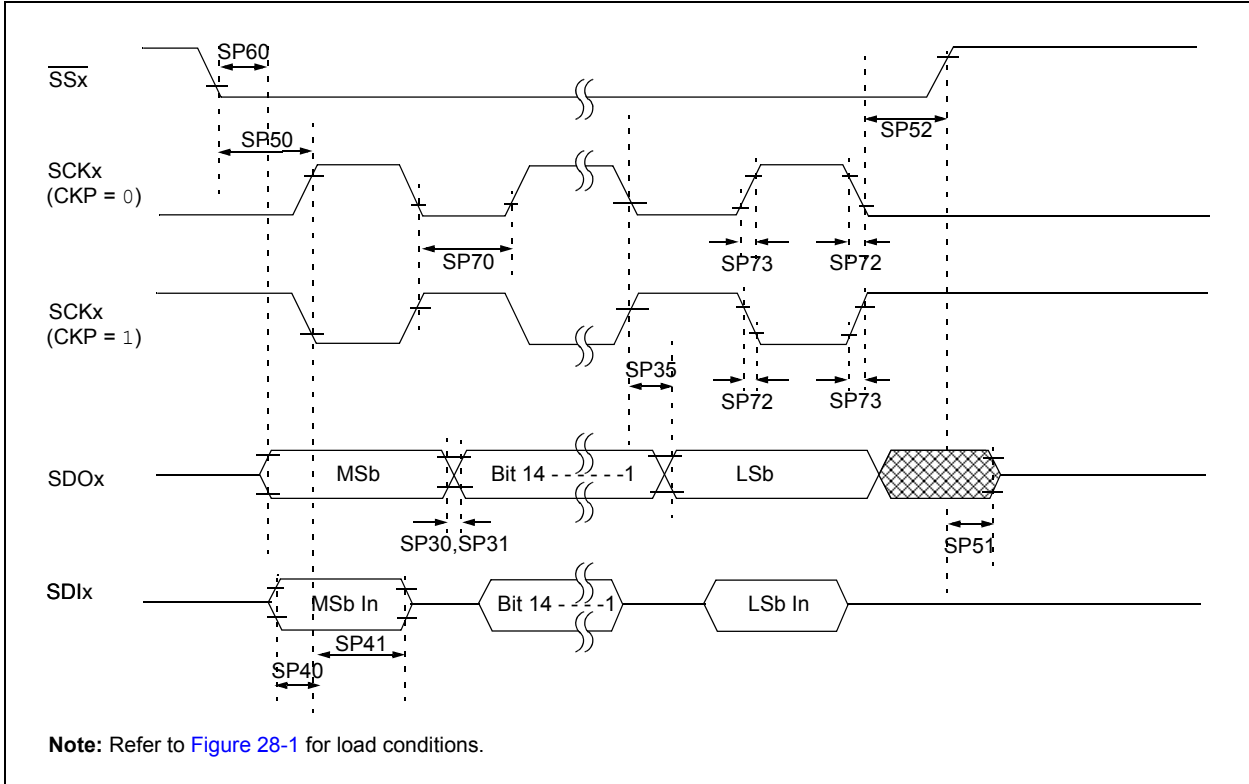
**Note 1:** Base IDLE current is measured as follows:

- CPU core is off (i.e., Idle mode), oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- External Secondary Oscillator disabled (i.e., SOSCO and SOSCI pins configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero)
- JTAG is disabled

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** These parameters are characterized but not tested in manufacturing.

FIGURE 28-13: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS





**TABLE 28-34: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	—	—	15	MHz	See <b>Note 3</b>
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter <a href="#">DO32</a> and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter <a href="#">DO31</a> and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter <a href="#">DO32</a> and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter <a href="#">DO31</a> and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sch, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP50	TssL2sch, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance <sup>(4)</sup>	10	—	50	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 Tcy + 40	—	—	ns	See <b>Note 4</b>

- Note 1:** These parameters are characterized, but are not tested in manufacturing.  
**Note 2:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.  
**Note 3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.  
**Note 4:** Assumes 50 pF load on all SPIx pins.

FIGURE 28-27: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

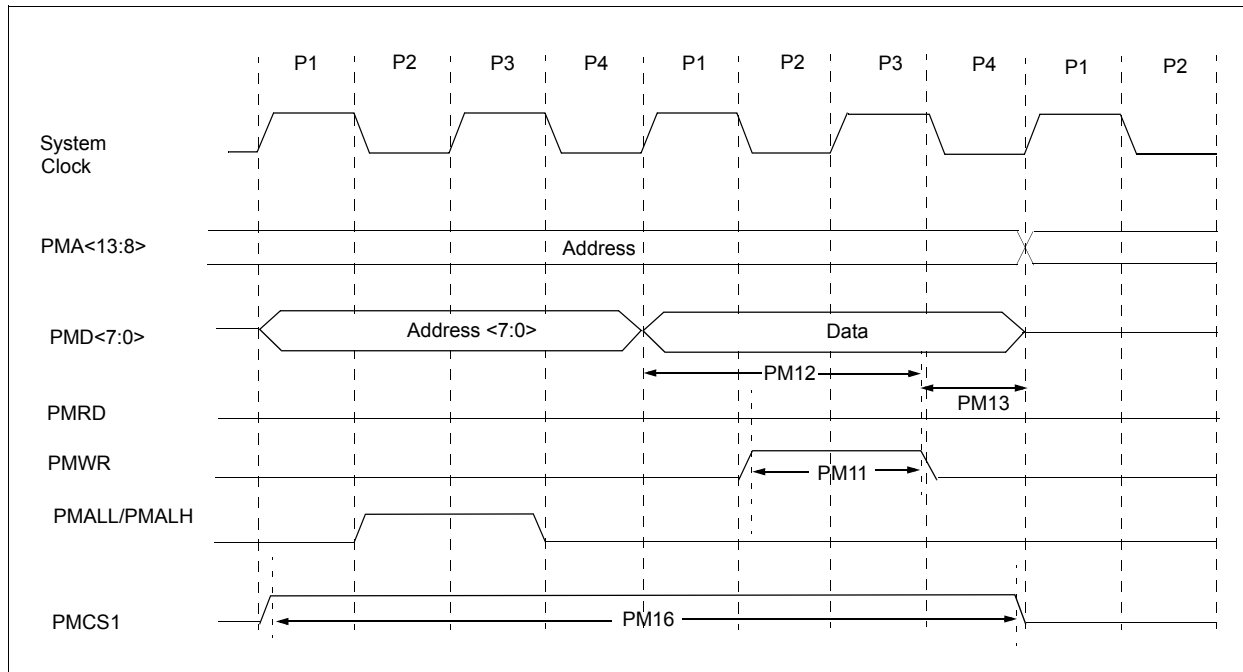


TABLE 28-50: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ	Max.	Units	Conditions
PM11	PMWR Pulse Width	—	0.5 T <sub>CY</sub>	—	ns	—
PM12	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	—	—	ns	—
PM13	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	—	—	ns	—
PM16	PMCSx Pulse Width	T <sub>CY</sub> - 5	—	—	ns	—

TABLE 28-51: DMA READ/WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ	Max.	Units	Conditions
DM1	DMA Read/Write Cycle Time	—	—	1 T <sub>CY</sub>	ns	—

**PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04**

**TABLE 29-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	<b>Output Low Voltage</b> I/O Pins: 2x Sink Driver Pins - RA2, RA7-RA10, RB10, RB11, RB7, RB4, RC3-RC9	—	—	0.4	V	$I_{OL} \leq 1.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output Low Voltage</b> I/O Pins: 4x Sink Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	—	—	0.4	V	$I_{OL} \leq 3.6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output Low Voltage</b> I/O Pins: 8x Sink Driver Pins - RA3, RA4	—	—	0.4	V	$I_{OL} \leq 6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
DO20	VOH	<b>Output High Voltage</b> I/O Pins: 2x Source Driver Pins - RA2, RA7-RA10, RB4, RB7, RB10, RB11, RC3-RC9	2.4	—	—	V	$I_{OL} \geq -1.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> I/O Pins: 4x Source Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	2.4	—	—	V	$I_{OL} \geq -3 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> I/O Pins: 8x Source Driver Pins - RA4, RA3	2.4	—	—	V	$I_{OL} \geq -6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
DO20A	VOH1	<b>Output High Voltage</b> I/O Pins: 2x Source Driver Pins - RA2, RA7-RA10, RB4, RB7, RB10, RB11, RC3-RC9	1.5	—	—	V	$I_{OH} \geq -1.9 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -1.85 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -1.4 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> 4x Source Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> I/O Pins: 8x Source Driver Pins - RA3, RA4	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>

**Note 1:** Parameters are characterized, but not tested.

TABLE A-4: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
<b>Section 29.0 “High Temperature Electrical Characteristics”</b>	Updated all ambient temperature end range values to +150°C throughout the chapter. Updated the storage temperature end range to +160°C. Updated the maximum junction temperature from +145°C to +155°C. Updated the maximum values for High Temperature Devices in the Thermal Operating Conditions (see Table 29-2). Updated the ADC Module Specifications (12-bit Mode), removing all parameters with the exception of HAD33a (see Table 29-14). Updated the ADC Module Specifications (10-bit Mode), removing all parameters with the exception of HAD33b (see Table 29-16).
<b>“Product Identification System”</b>	Updated the end range temperature value for H (High) devices.

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