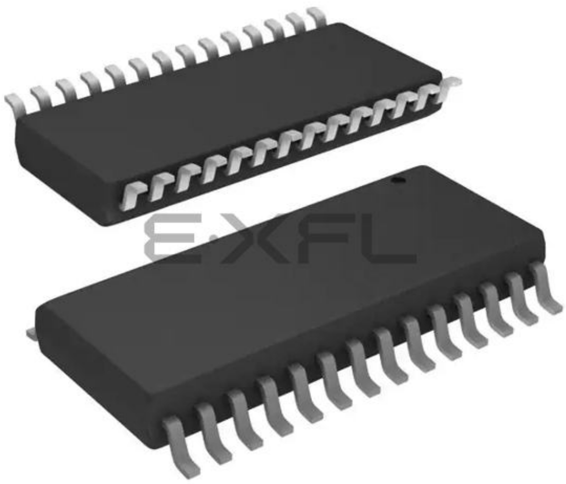

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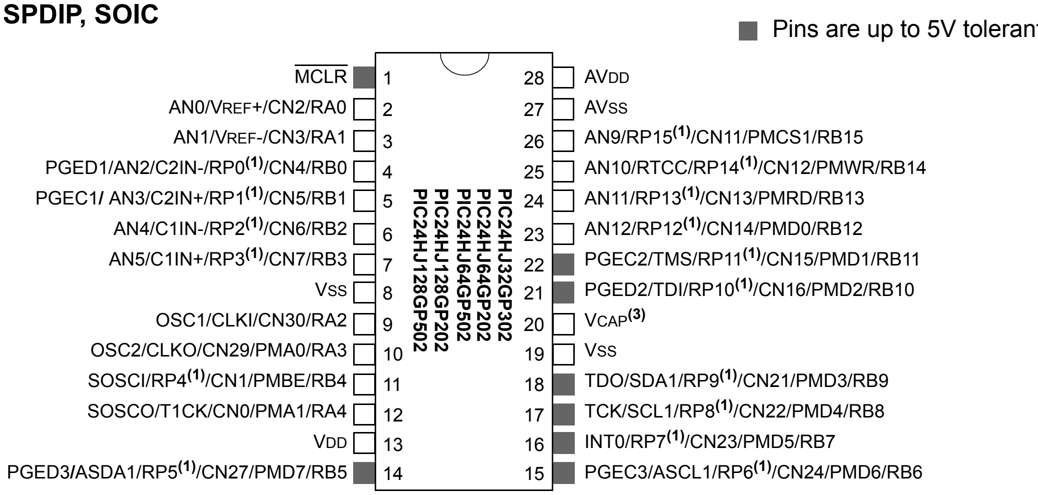
Applications of "Embedded - Microcontrollers"

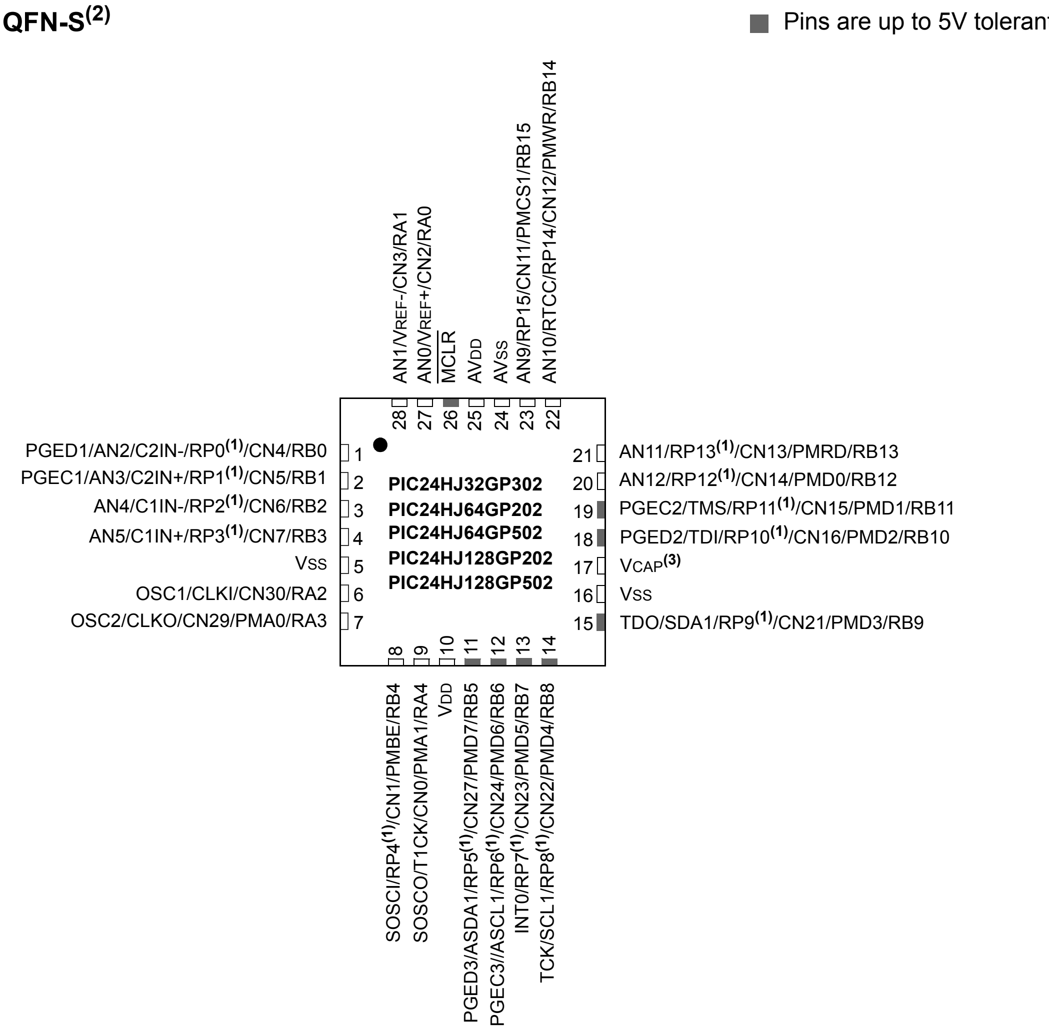
Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj32gp302t-i-so

Pin Diagrams

28-Pin SPDIP, SOIC



28-Pin QFN-S(2)



Note 1: The RPx pins can be used by any remappable peripheral. See Table 1 in this section for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

3: Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** for proper connection to this pin.

4.4.1 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-5. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

> **Note:** A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

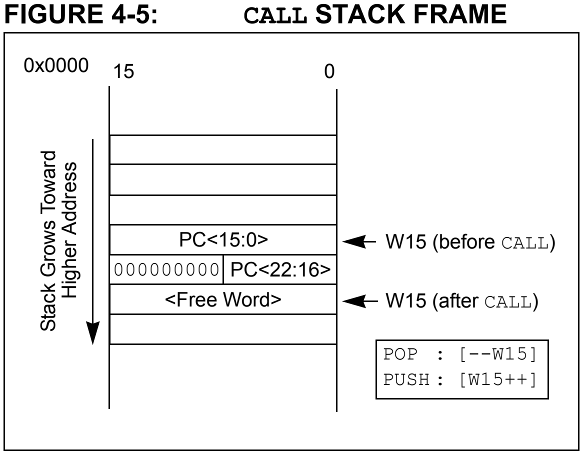
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap does not occur. The stack error trap occurs on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-5: CALL STACK FRAME



4.4.2 DATA RAM PROTECTION FEATURE

The PIC24H product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for BS) is accessible only from the Boot Segment Flash code when enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-35 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (near data space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where:

Operand 1 is always a working register (that is, the addressing mode can only be register direct), which is referred to as Wb.

Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

4.6.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access to stored constant data from the data space without the need to use special instructions, such as `TBLRDL/TBLRDH`.

Program space access through the data space occurs if the MSb of the data space EA is '`1`' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add a cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address 0x8000 and higher maps directly into a corresponding program memory address (see Figure 4-8), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '`1111 1111`' or '`0000 0000`' to force a `NOP`. This prevents possible issues should the area of code ever be accidentally executed.

Note:	PSV access is temporarily disabled during table reads/writes.

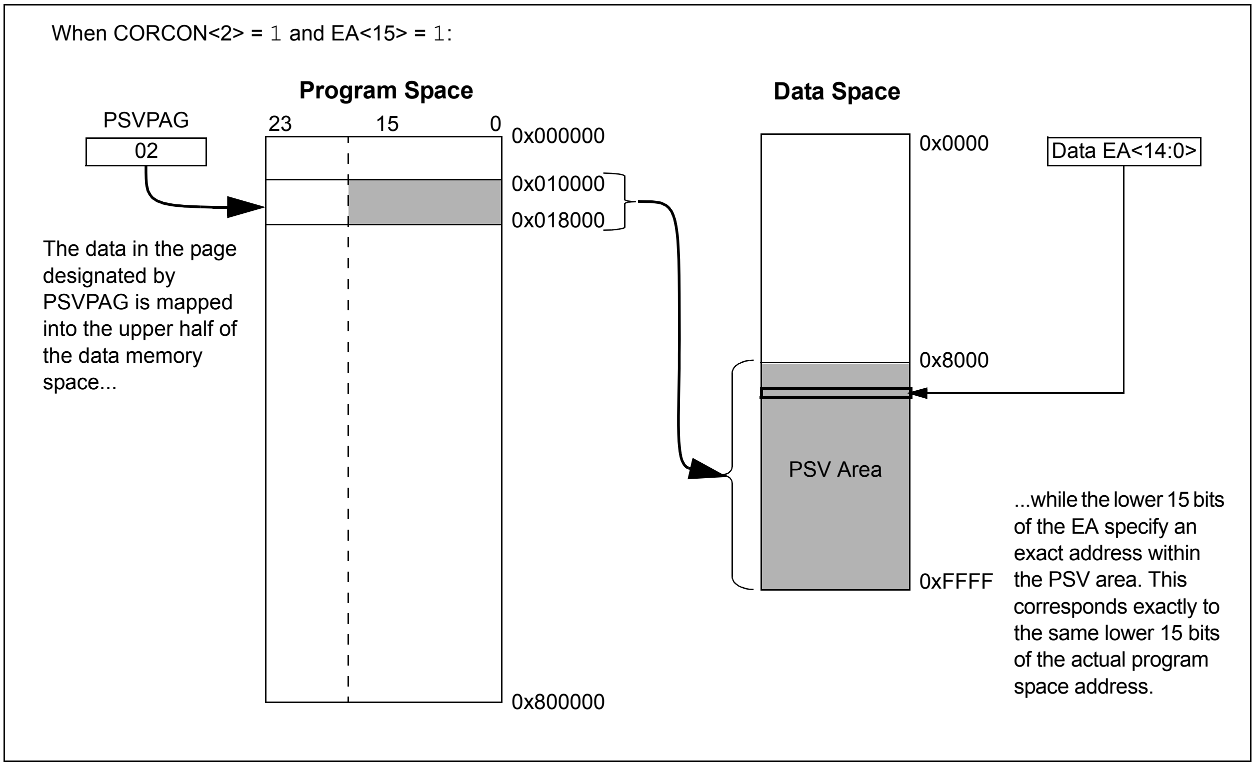
For operations that use PSV and are executed outside a `REPEAT` loop, the `MOV` and `MOV.D` instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, and are executed inside a `REPEAT` loop, these instances require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the `REPEAT` loop allows the instruction using PSV to access data, to execute in a single cycle.

FIGURE 4-8: PROGRAM SPACE VISIBILITY OPERATION



9.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides significant flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 9-2.

The output of the primary oscillator or FRC, denoted as ‘FIN’, is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL’s Voltage Controlled Oscillator (VCO). The input to the VCO must be selected in the range of 0.8 MHz to 8 MHz. The prescale factor ‘N1’ is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor ‘M’, by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor ‘N2’. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). ‘N2’ can be either 2, 4 or 8, and must be selected such that the PLL output frequency (FOSC) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output ‘FIN’, the PLL output ‘FOSC’ is given by:

EQUATION 9-2: FOSC CALCULATION

$$FOSC = FIN \bullet \left(\frac{M}{N1 \bullet N2}\right)$$

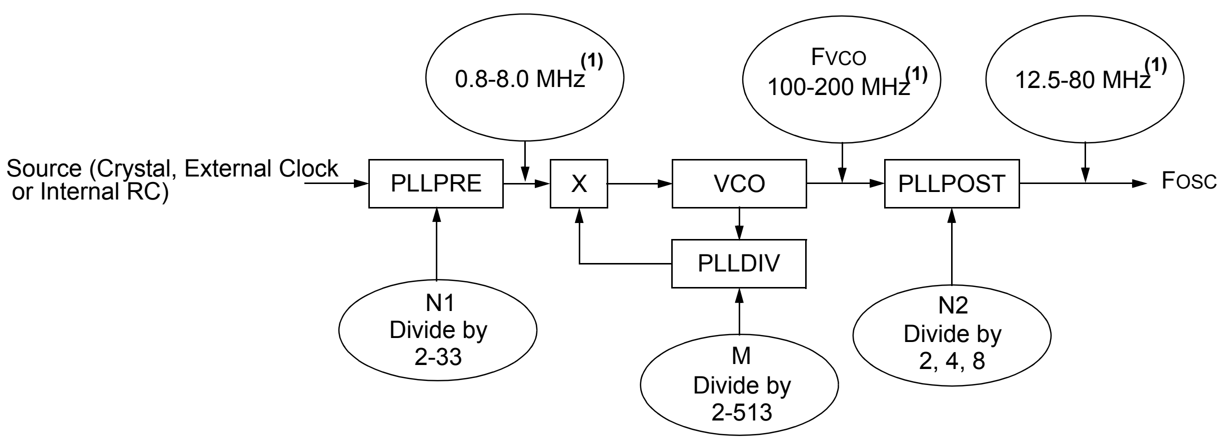
For example, suppose a 10 MHz crystal is being used with the selected oscillator mode of XT with PLL.

- If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 10/2 = 5 MHz, which is within the acceptable range of 0.8-8 MHz.
- If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 x 32 = 160 MHz, which is within the 100-200 MHz ranged needed.
- If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.

EQUATION 9-3: XT WITH PLL MODE EXAMPLE

$$FCY = \frac{FOSC}{2} = \frac{1}{2}\left(\frac{10000000 \bullet 32}{2 \bullet 2}\right) = 40MIPS$$

FIGURE 9-2: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 AND PIC24HJ128GPX02/X04 PLL BLOCK DIAGRAM



Note 1: This frequency range must be satisfied at all times.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3) (CONTINUED)

bit 3 **CF:** Clock Fail Detect bit (read/clear by application)
1 = FSCM has detected clock failure
0 = FSCM has not detected clock failure

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** Secondary (LP) Oscillator Enable bit
1 = Enable secondary oscillator
0 = Disable secondary oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 39. "Oscillator (Part III)"** (DS70308) in the *"dsPIC33F/PIC24H Family Reference Manual"* (available from the Microchip web site) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register is reset only on a Power-on Reset (POR).

11.0 I/O PORTS

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "I/O Ports"** (DS70193) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

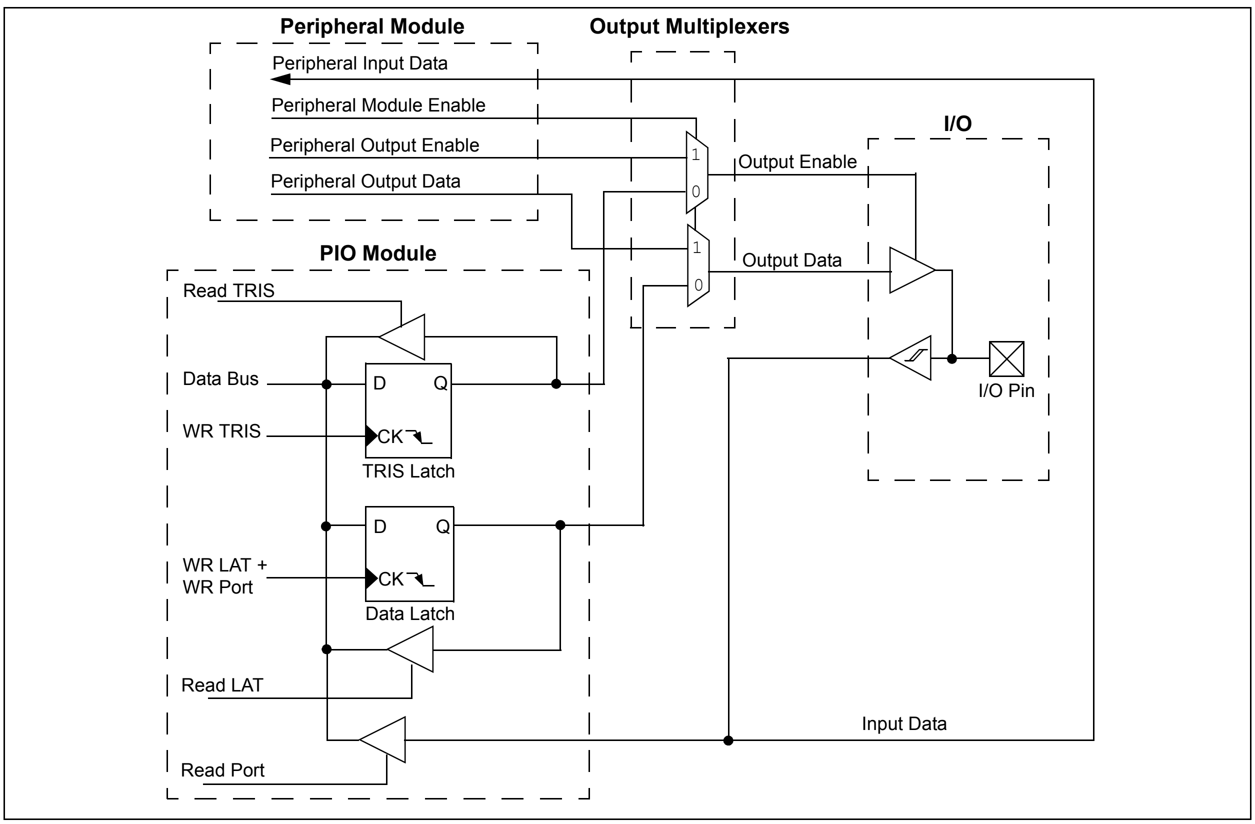
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 11-21: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTERS 6

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP13R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP12R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP13R<4:0>:** Peripheral Output Function is Assigned to RP13 Output Pin bits (see Table 11-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP12R<4:0>:** Peripheral Output Function is Assigned to RP12 Output Pin bits (see Table 11-2 for peripheral function numbers)

REGISTER 11-22: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTERS 7

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP15R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP14R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP15R<4:0>:** Peripheral Output Function is Assigned to RP15 Output Pin bits (see Table 11-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP14R<4:0>:** Peripheral Output Function is Assigned to RP14 Output Pin bits (see Table 11-2 for peripheral function numbers)

NOTES:

16.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In non-framed 3-wire mode, (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

Note:	This will insure that during power-up and initialization the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame sync pulse is active on the SSx pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. Refer to the SPI electrical characteristics for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.
5. To avoid invalid slave read data to the master, the user's master software must guarantee enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPI shift register and is empty once the data transmission begins.

16.2 SPI Resources

Many useful resources related to SPI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315

16.2.1 KEY RESOURCES

- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70206)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

21.3 Comparator Voltage Reference

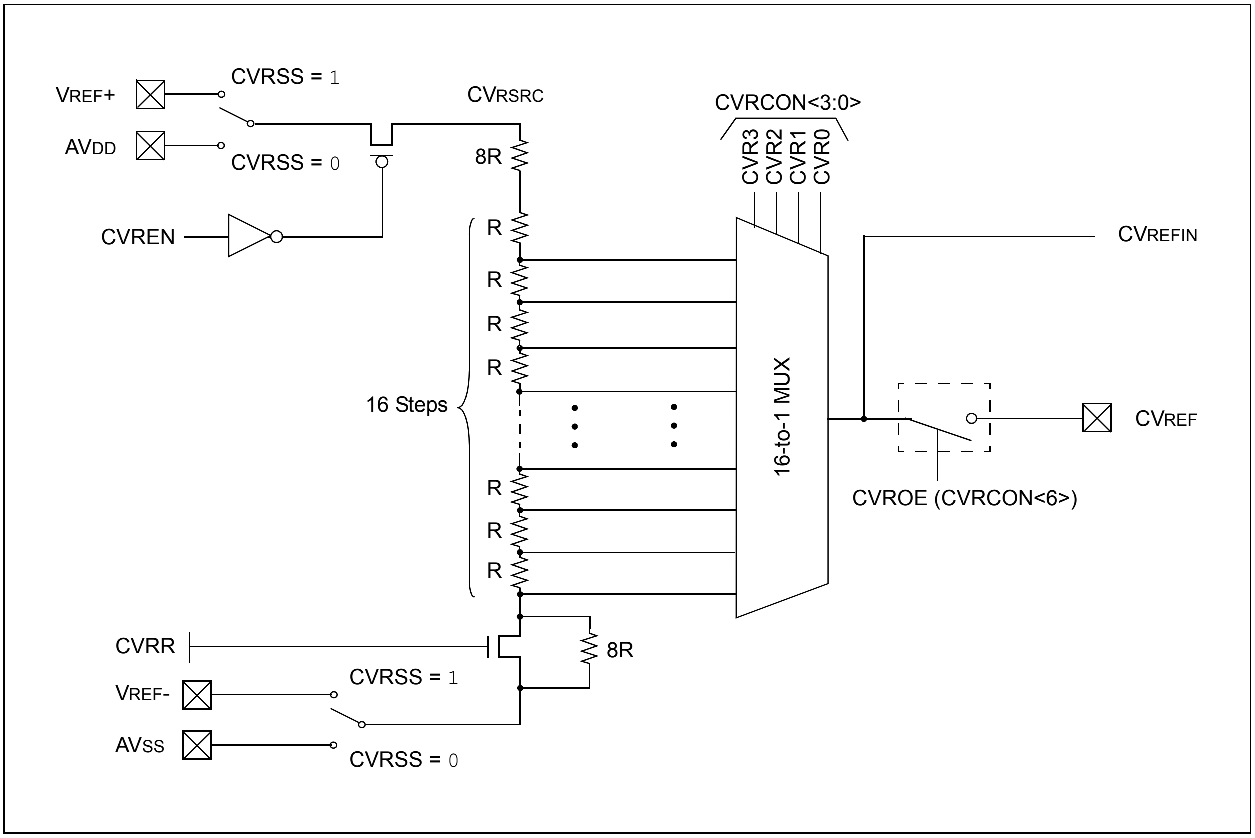
21.3.1 CONFIGURING THE COMPARATOR VOLTAGE REFERENCE

The Voltage Reference module is controlled through the CVRCON register (Register 21-2). The comparator voltage reference provides two ranges of output voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF Selection bits (CVR3:CVR0), with one range offering finer resolution.

The comparator reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<4>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 21-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



REGISTER 22-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL(1)	PMPTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit(1)
- 1 = RTCC seconds clock is selected for the RTCC pin
- 0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffers

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) needs to be set.

23.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. "Programmable Cyclic Redundancy Check (CRC)"** (DS70298) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable polynomial CRC equation
- Interrupt output
- Data FIFO

23.1 Overview

The module implements a software configurable CRC generator. The terms of the polynomial and its length can be programmed using the CRCXOR bits (X<15:1>) and the CRCCON bits (PLEN<3:0>), respectively.

EQUATION 23-1: CRC EQUATION

$$x^{16} + x^{12} + x^{5} + 1$$

To program this polynomial into the CRC generator, the CRC register bits should be set as shown in Table 23-1.

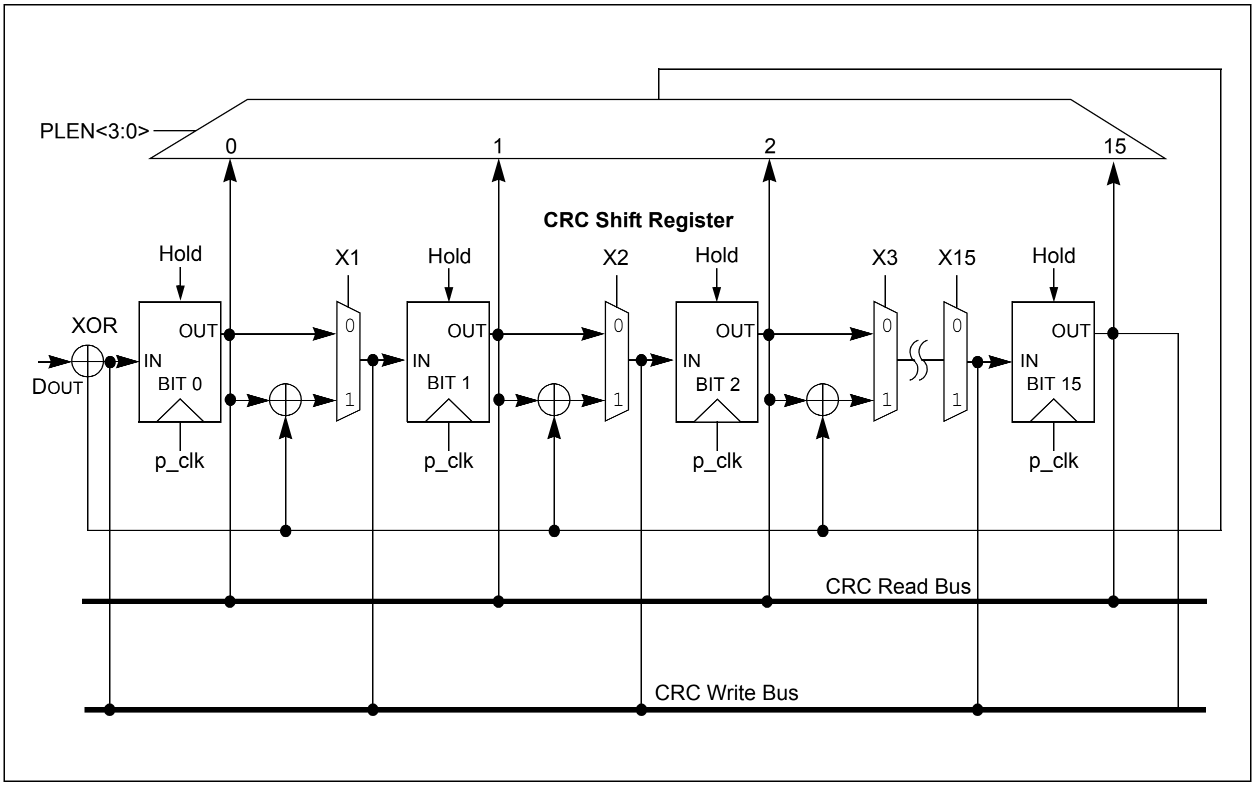
TABLE 23-1: EXAMPLE CRC SETUP

Bit Name	Bit Value
PLEN<3:0>	1111
X<15:1>	000100000010000

For the value of X<15:1>, the 12th bit and the 5th bit are set to '1', as required by the CRC equation. The 0th bit required by the CRC equation is always XORed. For a 16-bit polynomial, the 16th bit is also always assumed to be XORed; therefore, the X<15:1> bits do not have the 0th bit or the 16th bit.

The topology of a standard CRC generator is shown in Figure 23-2.

FIGURE 23-1: CRC SHIFTER DETAILS



23.4 Programmable CRC Resources

Many useful resources related to Programmable CRC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en534555

23.4.1 KEY RESOURCES

- **Section 36. "Programmable Cyclic Redundancy Check CRC)"** (DS70298)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 24-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 2 **BEP:** Byte Enable Polarity bit

1 = Byte enable active-high (PMBE)
0 = Byte enable active-low ($\overline{\text{PMBE}}$)

bit 1 **WRSP:** Write Strobe Polarity bit

For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):

1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)

For Master mode 1 (PMMODE<9:8> = 11):

1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit

For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):

1 = Read strobe active-high (PMRD)
0 = Read strobe active-low ($\overline{\text{PMRD}}$)

For Master mode 1 (PMMODE<9:8> = 11):

1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 24-2: PMMODE: PARALLEL PORT MODE REGISTER

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB<1:0>[(1)]		WAITM<3:0>				WAITE<1:0>[(1)]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy (not useful when the processor stall is active)
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = No interrupt generated, processor stall activated
01 = Interrupt generated at the end of the read/write cycle
00 = No interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
10 = Decrement ADDR<10:0> by 1 every read/write cycle
01 = Increment ADDR<10:0> by 1 every read/write cycle
00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
1 = 16-bit mode: data register is 16 bits, a read or write to the data register invokes two 8-bit transfers
0 = 8-bit mode: data register is 8 bits, a read or write to the data register invokes one 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 =Master mode 1 (PMCS1, PMRD/$\overline{\text{PMWR}}$, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
10 =Master mode 2 (PMCS1, PMRD, PMWR, PMBE, PMA<x:0> and PMD<7:0>)
01 =Enhanced PSP, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCS1}}$, PMD<7:0> and PMA<1:0>)
00 =Legacy Parallel Slave Port, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCS1}}$ and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Wait State Configuration bits[(1)]
11 = Data wait of 4 T_{CY}; multiplexed address phase of 4 T_{CY}
10 = Data wait of 3 T_{CY}; multiplexed address phase of 3 T_{CY}
01 = Data wait of 2 T_{CY}; multiplexed address phase of 2 T_{CY}
00 = Data wait of 1 T_{CY}; multiplexed address phase of 1 T_{CY}

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits
1111 = Wait of additional 15 T_{CY}
•
•
•
0001 = Wait of additional 1 T_{CY}
0000 = No additional wait cycles (operation forced into one T_{CY})

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits[(1)]
11 = Wait of 4 T_{CY}
10 = Wait of 3 T_{CY}
01 = Wait of 2 T_{CY}
00 = Wait of 1 T_{CY}

Note 1: WAITB and WAITE bits are ignored whenever WAITM3:WAITM0 = 0000.

25.4 Watchdog Timer (WDT)

For PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

25.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (T_{WDT}) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a `PWRSAV` instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a `CLRWDT` instruction during normal execution

Note:	The `CLRWDT` and `PWRSAV` instructions clear the prescaler and postscaler counts when executed.

25.4.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the `PWRSAV` instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3,2>) needs to be cleared in software after the device wakes up.

25.4.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

Note:	If the WINDIS bit (FWDT<6>) is cleared, the `CLRWDT` instruction should be executed by the application software only during the last 1/4 of the WDT period. This `CLRWDT` window can be determined by using a timer. If a `CLRWDT` instruction is executed before this window, a WDT Reset occurs.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

FIGURE 25-2: WDT BLOCK DIAGRAM

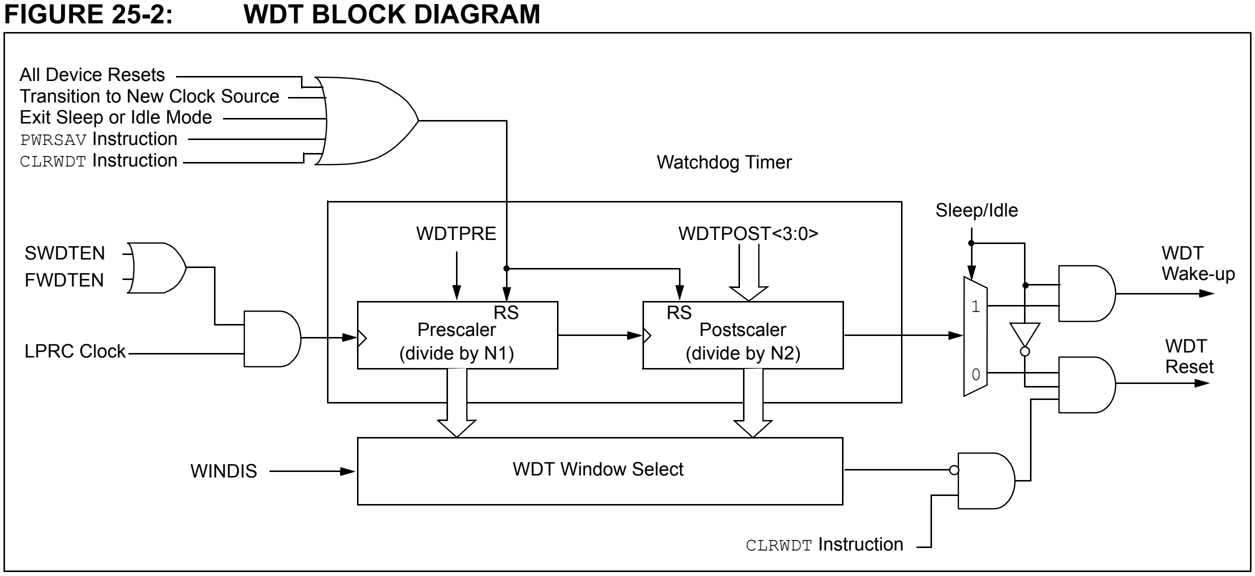


TABLE 25-3: CODE FLASH SECURITY SEGMENT SIZES FOR 32 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K		BSS<2:0> = x10 1K		BSS<2:0> = x01 4K		BSS<2:0> = x00 8K	
SSS<2:0> = x11 **0K**	VS = 256 IW GS = 11008 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x0057FEh 0x0157FEh	VS = 256 IW BS = 768 IW GS = 10240 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x0057FEh 0x0157FEh	VS = 256 IW BS = 3840 IW GS = 7168 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x0057FEh 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 3072 IW	0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x0057FEh 0x0157FEh

TABLE 25-4: CODE FLASH SECURITY SEGMENT SIZES FOR 64 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K	BSS<2:0> = x10 1K	BSS<2:0> = x01 4K	BSS<2:0> = x00 8K
SSS<2:0> = x11 **0K**	VS = 256 IW GS = 21760 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 768 IW GS = 20992 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 3840 IW GS = 17920 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh
SSS<2:0> = x10 **4K**	VS = 256 IW SS = 3840 IW GS = 17920 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 768 IW SS = 3072 IW GS = 17920 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 3840 IW GS = 17920 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh
SSS<2:0> = x01 **8K**	VS = 256 IW SS = 7936 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 768 IW SS = 7168 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 3840 IW SS = 4096 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 7936 IW GS = 13824 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh
SSS<2:0> = x00 **16K**	VS = 256 IW SS = 16128 IW GS = 5632 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 768 IW SS = 15360 IW GS = 5632 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 3840 IW SS = 12288 IW GS = 5632 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh	VS = 256 IW BS = 7936 IW SS = 8192 IW GS = 5632 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x00ABFEh 0x0157FEh

NOTES:

TABLE A-4: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 28.0 “Electrical Characteristics”	Updated the maximum value for Extended Temperature Devices in the Thermal Operating Conditions (see Table 28-2). Removed Note 4 from the DC Temperature and Voltage Specifications (see Table 28-4). Updated all typical and maximum Operating Current (I_{DD}) values (see Table 28-5). Updated all typical and maximum Idle Current (I_{IDLE}) values (see Table 28-6). Updated the maximum Power-Down Current (I_{PD}) values for parameters DC60d, DC60a, and DC60b (see Table 28-7). Updated all typical Doze Current (Idoze) values (see Table 28-8). Updated the maximum value for parameter DI19 and added parameters DI28, DI29, DI60a, DI60b, and DI60c to the I/O Pin Input Specifications (see Table 28-9). Added Note 2 to the PLL Clock Timing Specifications (see Table 28-17) Removed Note 2 from the AC Characteristics: Internal RC Accuracy (see Table 28-18). Updated the Internal RC Accuracy minimum and maximum values for parameter F21b (see Table 28-19). Updated the characteristic description for parameter DI35 in the I/O Timing Requirements (see Table 28-20). Updated *all* SPI specifications (see Table 28-28 through Table 28-35 and Figure 28-10 through Figure 28-16) Updated the ADC Module Specification minimum values for parameters AD05 and AD07, and updated the maximum value for parameter AD06 (see Table 28-41). Updated the ADC Module Specifications (12-bit Mode) minimum and maximum values for parameter AD21a (see Table 28-42). Updated all ADC Module Specifications (10-bit Mode) values, with the exception of Dynamic Performance (see Table 28-43). Updated the minimum value for parameter PM6 and the maximum value for parameter PM7 in the Parallel Master Port Read Timing Requirements (see Table 28-49). Added DMA Read/Write Timing Requirements (see Table 28-51).