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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp502-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

- Note 1: To access the documents listed below, browse to the documentation section of the PIC24HJ64GP204 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.
 In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.
- Section 1. "Introduction" (DS70197)
- Section 2. "CPU" (DS70204)
- Section 3. "Data Memory" (DS70202)
- Section 4. "Program Memory" (DS70202)
- Section 5. "Flash Programming" (DS70191)
- Section 8. "Reset" (DS70192)
- Section 9. "Watchdog Timer and Power-saving Modes" (DS70196)
- Section 11. "Timers" (DS70205)
- Section 12. "Input Capture" (DS70198)
- Section 13. "Output Compare" (DS70209)
- Section 16. "Analog-to-Digital Converter (ADC)" (DS70183)
- Section 17. "UART" (DS70188)
- Section 18. "Serial Peripheral Interface (SPI)" (DS70206)
- Section 19. "Inter-Integrated Circuit™ (I²C™)" (DS70195)
- Section 23. "CodeGuard™ Security" (DS70199)
- Section 24. "Programming and Diagnostics" (DS70209)
- Section 25. "Device Configuration" (DS70194)
- Section 30. "I/O Ports with Peripheral Pin Select (PPS)" (DS70190)
- Section 32. "Interrupts (Part III)" (DS70214)
- Section 33. "Audio Digital-to-Analog Converter (DAC)" (DS70211)
- Section 34. "Comparator" (DS70212)
- Section 35. "Parallel Master Port (PMP)" (DS70299)
- Section 36. "Programmable Cyclic Redundancy Check (CRC)" (DS70298)
- Section 37. "Real-Time Clock and Calendar (RTCC)" (DS70301)
- Section 38. "Direct Memory Access" (DS70215)
- Section 39. "Oscillator (Part III)" (DS70216)

6.0 RESETS

- **Note 1:** This data sheet summarizes the features PIC24HJ32GP302/304. of the PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 8. "Reset" (DS70192) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- · IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Uninitialized W Register Reset
 - Security Reset

FIGURE 6-1:

RESET SYSTEM BLOCK DIAGRAM

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 3.0 "CPU" of this manual for register Reset states.

All types of device Reset sets a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR bit (RCON<0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.



6.9 Configuration Mismatch Reset

To maintain the integrity of the peripheral pin select control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset occurs.

The Configuration Mismatch Flag bit (CM) in the Reset Control register (RCON<9>) is set to indicate the configuration mismatch Reset. Refer to **Section 11.0 "I/O Ports"** for more information on the configuration mismatch Reset.

Note: The configuration mismatch feature and associated reset flag is not available on all devices.

6.10 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- · Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag bit (IOPUWR) in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

6.10.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The illegal opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the illegal opcode Reset, use only the lower 16 bits of

each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

6.10.2 UNINITIALIZED W REGISTER RESET

Any attempts to use the uninitialized W register as an address pointer will Reset the device. The W register array (with the exception of W15) is cleared during all resets and is considered uninitialized until written to.

6.10.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a Call, Jump, Computed Jump, Return, Return from Subroutine, or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an Interrupt or Trap vector.

Refer to Section 25.8 "Code Protection and CodeGuard™ Security" for more information on Security Reset.

6.11 Using the RCON Status Bits

The user application can read the Reset Control register (RCON) after any device Reset to determine the cause of the reset.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the reset flag bit operation.

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR, BOR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access or Security Reset	POR, BOR
CM (RCON<9>)	Configuration Mismatch	POR, BOR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET instruction	POR, BOR
WDTO (RCON<4>)	WDT time-out	PWRSAV instruction, CLRWDT instruction, POR, BOR
SLEEP (RCON<3>)	PWRSAV #SLEEP instruction	POR, BOR
IDLE (RCON<2>)	PWRSAV #IDLE instruction	POR, BOR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

TABLE 6-3: RESET FLAG BIT OPERATION

Note: All Reset flag bits can be set or cleared by user software.

11.0	11.0	11.0	11.0	11.0	11.0	11.0	11.0
0-0	0-0	0-0	0-0	0-0	0-0	0-0	0-0
	_		_	_		—	—
Dit 15							Bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
_	C1TXIF ⁽¹⁾	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	_
bit 7	·						bit 0
Legena:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15 7	Unimplomon	tod: Dood os '	0'				
		NIA Transmit C			Nature 1: 1: (1)		
DIT 6				nterrupt Flag S	status bit		
	\perp = Interrupt i	request has oc	t occurred				
bit 5		A Channel 7 D	ata Transfor (Complete Interr	unt Elag Status	hit	
DIL 5	1 = Interrupt				upi Flag Status	DIL	
	0 = Interrupt I	request has no	t occurred				
bit 4	DMA6IF: DM	DMA6IE: DMA Channel 6 Data Transfer Complete Interrunt Flag Status hit					
	1 = Interrupt i	1 = Interrupt request has occurred					
	0 = Interrupt i	request has no	t occurred				
bit 3	CRCIF: CRC	CRCIF: CRC Generator Interrupt Flag Status bit					
	1 = Interrupt request has occurred						
	0 = Interrupt i	0 = Interrupt request has not occurred					
bit 2	U2EIF: UART	2 Error Interru	pt Flag Status	bit			
	1 = Interrupt i	request has oc	curred				
	0 = Interrupt i	request has no	t occurred				
bit 1	U1EIF: UART	1 Error Interru	pt Flag Status	bit			
	1 = Interrupt i	request has oc	curred				
	0 = Interrupt I	request has no	t occurred				

Note 1: Interrupts disabled on devices without ECAN[™] modules.

Unimplemented: Read as '0'

bit 0

9.1 CPU Clocking System

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices provide seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- · Low-Power RC (LPRC) Oscillator
- · FRC Oscillator with postscaler

9.1.1 SYSTEM CLOCK SOURCES

The Fast RC (FRC) internal oscillator runs at a nominal frequency of 7.37 MHz. User software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

The primary oscillator can use one of the following as its clock source:

- Crystal (XT): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- High-Speed Crystal (HS): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- External Clock (EC): External clock signal is directly applied to the OSC1 pin.

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The Low-Power RC (LPRC) internal oscillator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip PLL to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 9.1.3 "PLL Configuration**".

The FRC frequency depends on the FRC accuracy (see Table 28-19) and the value of the FRC Oscillator Tuning register (see Register 9-4).

9.1.2 SYSTEM CLOCK SELECTION

The oscillator source used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to Section 25.1 "Configuration Bits" for further details.) The Initial Oscillator FNOSC<2:0> Selection Configuration bits, (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose among 12 different clock modes, shown in Table 9-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected) FOSC is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device, and speeds up to 40 MHz are supported by the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 architecture.

Instruction execution speed or device operating frequency, FCY, is given by:

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$FCY = \frac{FOSC}{2}$$

REGISTER	9-2: CLKD	IV: CLOCK D	IVISOR RE	GISTER ⁽²⁾			
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI		DOZE<2:0>		DOZEN ⁽¹⁾		FRCDIV<2:0>	
bit 15							bit 8
R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPO	OST<1:0>				PLLPRE<4:0	>	
bit 7							bit 0
Legend:		v = Value set	from Configu	ration bits on P0)R		
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
in value at							
bit 15	ROI: Recove	r on Interrupt bi	t				
	1 = Interrupt 0 = Interrupt	s clears the DO s have no effec	ZEN bit and to the DOZ	the processor cl EN bit	ock/periphera	l clock ratio is se	t to 1:1
bit 14-12	DOZE<2:0>:	Processor Cloc	k Reduction	Select bits			
	111 = Fcy/12	28					
	110 = FCY/64	4					
	101 = FCY/32	2					
	100 = FCY/10) (default)					
	010 = Fcy/4						
	001 = Fcy/2						
	000 = Fcy/1						
bit 11	DOZEN: DO	ZE Mode Enabl	e bit ⁽¹⁾				
	1 = The DO2 0 = Processe	ZE<2:0> bits sp or clock/periphe	ecify the ration ration ration ration ration rational clock ration rational clock ration ration ration ration rational rationa	b between the pe b forced to 1:1	eripheral clock	s and the proces	ssor clocks
bit 10-8	FRCDIV<2:0	>: Internal Fast	RC Oscillato	or Postscaler bits	6		
	111 = FRC d	livide by 256					
	110 = FRC d	livide by 64					
	101 = FRC d	livide by 32					
	011 = FRC d	livide by 10					
	010 = FRC d	livide by 4					
	001 = FRC d	livide by 2					
	000 = FRC d	livide by 1 (defa	ult)				
bit 7-6	PLLPOST<1	:0>: PLL VCO (Output Divide	er Select bits (als	so denoted as	'N2', PLL postso	aler)
	11 = Output/	8					
	10 = Reserve	eu 4 (default)					
	00 = Output/2	2					
bit 5	Unimplemer	nted: Read as ')'				
bit 4-0	PLLPRE<4:0)>: PII Phase I	- Detector Inpu	ıt Divider bits (al	so denoted as	s 'N1', PLL presc	aler)
	11111 = Inp	ut/33				, , p.ccc	,
	•						
	•						
	•						
	00001 = Inp	ut/3					
	00000 = Inp i	ut/2 (default)					

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register is reset only on a Power-on Reset (POR).

11.7 I/O Helpful Tips

- 1. In some cases, certain pins as defined in Table 28-9 under "Injection Current", have internal protection diodes to VDD and VSS. The term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with nominal VDD with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
- I/O pins that are shared with any analog input pin, 2 (i.e., ANx), are always analog pins by default after any reset. Consequently, any pin(s) configured as an analog input pin, automatically disables the digital input pin buffer. As such, any attempt to read a digital input pin will always return a '0' regardless of the digital logic level on the pin if the analog pin is configured. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the analog pin configuration registers in the ADC module, (i.e., ADxPCFGL, AD1PCFGH), by setting the appropriate bit that corresponds to that I/O port pin to a '1'. On devices with more than one ADC, both analog pin configurations for both ADC modules must be configured as a digital I/O pin for that pin to function as a digital I/O pin.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.

11.8 I/O Ports Resources

Many useful resources related to I/O Ports are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en532315

11.8.1 KEY RESOURCES

- Section 10. "I/O Ports" (DS70193)
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

11.9 Peripheral Pin Select Registers

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family of devices implement 27 registers for remappable peripheral configuration:

- 14 Input Remappable Peripheral Registers:
 - RPINR0-RPINR1, RPINR3-RPINR4, RPINR7, RPINR10-RPINR11, RPINR18-RPINR23 and PRINR26
- 13 Output Remappable Peripheral Registers:
 - RPOR0-RPOR12

Note: Input and Output Register values can only be changed if the IOLOCK bit (OSCCON<6>) is set to '0'. See Section 11.6.3.1 "Control Register Lock" for a specific command sequence.

REGISTER 11-17:	RPOR2: PERIPHERAL	PIN SELECT OUTPUT	REGISTERS 2
-----------------	--------------------------	-------------------	-------------

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_	—			RP5R<4:0>		
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP4R<4:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimplemen	ted: Read as '	ר י				

bit 12-8	RP5R<4:0>: Peripheral Output Function is Assigned to RP5 Output Pin bits (see Table 11-2 for
	peripheral function numbers)
bit 7-5	Unimplemented: Read as '0'

- bit 4-0
- RP4R<4:0>: Peripheral Output Function is Assigned to RP4 Output Pin bits (see Table 11-2 for peripheral function numbers)

REGISTER 11-18: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTERS 3

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP7R<4:0>		
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP6R<4:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 RP7R<4:0>: Peripheral Output Function is Assigned to RP7 Output Pin bits (see Table 11-2 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 RP6R<4:0>: Peripheral Output Function is Assigned to RP6 Output Pin bits (see Table 11-2 for peripheral function numbers)

14.1 Input Capture Resources

Many useful resources related to Input Capture are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en532315

14.1.1 KEY RESOURCES

- Section 12. "Input Capture" (DS70198)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

17.2 I²C Resources

Many useful resources related to I^2C are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwprod-
	ucts/Devices.aspx?dDoc-
	Name=en532315

17.2.1 KEY RESOURCES

- Section 19. "Inter-Integrated Circuit™ (I²C™)" (DS70195)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

17.3 I²C Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write:

- I2CxRSR is the shift register used for shifting data internal to the module and the user application has no access to it
- I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read
- I2CxTRN is the transmit register to which bytes are written during a transmit operation
- The I2CxADD register holds the slave address
- A status bit, ADD10, indicates 10-bit Address mode
- The I2CxBRG acts as the Baud Rate Generator (BRG) reload value

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

19.4 ECAN Resources

Many useful resources related to ECAN are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en532315

19.4.1 KEY RESOURCES

- Section 21. "Enhanced Controller Area Network (ECAN™)" (DS70185)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

21.2 Comparator Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIDL		C2EVT	C1EVT	C2EN	C1EN	C2OUTEN ⁽¹⁾	C1OUTEN ⁽²⁾
bit 15							bit 8
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C10UT	C2INV	C1INV	C2NEG	C2POS	C1NEG	C1POS
bit 7							bit 0
Legend:	L :1		L :4				
R = Readable		VV = VVritable	DIT	U = Unimpler	nented bit, read		
-n = value at P	UR	"I" = Bit is set		$0^{\circ} = Bit is cle$	ared	x = Bit is unkr	lown
bit 15	CMIDI · Stop	in Idle Mode					
bit 10	1 = When de	vice enters Idle	e mode, modu	le does not ae	nerate interrupt	s. Module is sti	ll enabled
	0 = Continue	normal module	e operation in	Idle mode			
bit 14	Unimplemen	ted: Read as '	כי				
bit 13	C2EVT: Comp	parator 2 Event	t				
	1 = Compara	tor output char	nged states	1			
bit 10		itor output aid r	iot change sta	ates			
DIL 12	1 = Compara	tor output char	Nand states				
	0 = Compara	tor output did r	ot change sta	ates			
bit 11	C2EN: Compa	arator 2 Enable	;				
	1 = Compara 0 = Compara	tor is enabled tor is disabled					
bit 10	C1EN: Compa	arator 1 Enable	;				
	1 = Compara	tor is enabled					
	0 = Compara	tor is disabled	,	4			
bit 9	C2OUTEN: C	omparator 2 O	utput Enable ⁽	1)			
	1 = Compara	itor output is dr	iven on the ou at driven on th	Itput pad			
bit 8	C10UTEN: C	comparator 1 O	utput Enable ⁽⁾	2)			
Sit C	1 = Compara	tor output is dr	iven on the ou	utput pad			
	0 = Compara	tor output is no	t driven on th	e output pad			
bit 7	C2OUT: Com	parator 2 Outp	ut bit				
	When C2INV	<u>= 0:</u>					
	1 = C2 VIN+2 $0 = C2 VIN+4$	> 02 VIN- < C2 VIN-					
	When C2INV	= 1:					
	0 = C2 VIN+ 2	> C2 VIN-					
	1 = C2 VIN+ •	< C2 VIN-					
Note 1: If C2OUTEN = 1, the C2OUT peripheral output must be configured to an available RPx pin. See							

REGISTER 21-1: CMCON: COMPARATOR CONTROL REGISTER

- Section 11.6 "Peripheral Pin Select" for more information.
 If C10UTEN = 1, the C10UT peripheral output must be configured to an available RPX pin. See
 - 2: If C1OUTEN = 1, the C1OUT peripheral output must be configured to an available RPx pin. See Section 11.6 "Peripheral Pin Select" for more information.

REGISTER 24-3:	PMADDR: PARALLEL PORT ADDRESS REGISTER
----------------	--

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR15	CS1			ADDF	R<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ADD	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15	ADDR15: Parallel Port Destination Address bits
bit 14	CS1: Chip Select 1 bit
	1 = Chip select 1 is active
	0 = Chip select 1 is inactive
bit 13-0	ADDR13:ADDR0: Parallel Port Destination Address bits

REGISTER 24-4: PMAEN: PARALLEL PORT ENABLE REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	PTEN14	—	—	—		PTEN<10:8> ⁽¹⁾	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		PTEN<	7:2> ⁽¹⁾			PTEN	<1:0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14	PTEN14: PMCS1 Strobe Enable bit
	 1 = PMA14 functions as either PMA<14> bit or PMCS1 0 = PMA14 pin functions as port I/O
bit 13-11	Unimplemented: Read as '0'
bit 10-2	PTEN<10:2>: PMP Address Port Enable bits ⁽¹⁾
	1 = PMA<10:2> function as PMP address lines0 = PMA<10:2> function as port I/O
bit 1-0	PTEN<1:0>: PMALH/PMALL Strobe Enable bits
	 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL 0 = PMA1 and PMA0 pads functions as port I/O

Note 1: Devices with 28 pins do not have PMA<10:2>.

25.2 On-Chip Voltage Regulator

All of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 Ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 25-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 28-13 located in Section 28.1 "DC Characteristics".

Note:	It is important for the low-ESR capacitor to
	be placed as close as possible to the VCAP
	pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 25-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



25.3 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 25-5: CODE FLASH SECURITY SEGMENT SIZES FOR 128 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K	BSS<2:0> = x10 1K	BSS<2:0> = x01 4K	BSS<2:0> = x00 8K
SSS<2:0> = x11 0K	VS = 256 IW 0x00000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h 0x0007FEh 0x002000h 0x00200h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x010000h 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh BS = 768 IW 0x0007FEh 0x0007FEh 0x000800h 0x00200h 0x0007FEh 0x000200h 0x0007FEh 0x002000h 0x0007FFEh 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x0007FFEh 0x010000h 0x010000h 0x0157FEh 0x0157FEh	VS = 256 IW 0x00000h 0x0001FEh 0x000200h BS = 3840 IW 0x0007FEh 0x0007FEh 0x0000h 0x0007FEh 0x002000h 0x0000h 0x003FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x001000h 0x01000h 0x01000h 0x0157FEh	VS = 256 IW 0x000000h BS = 7936 IW 0x000200h 0x0007FEh 0x0007FEh 0x0000800h 0x00200h 0x00200h 0x0000800h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x00000h 0x00000h 0x007FEh 0x00000h 0x007FFEh 0x008000h 0x008000h 0x007FFEh 0x010000h 0x010000h 0x0157FEh 0x0157FEh
SSS<2:0> = x10 4K	VS = 256 IW 0x000000h 0x0001FEh 0x000200h SS = 3840 IW 0x0007FEh 0x000800h 0x001FFEh 0x000800h 0x001FFEh 0x00400h 0x00200h 0x00000h 0x00200h 0x00400h 0x007FEh 0x00400h 0x007FFEh 0x00400h 0x007FFEh 0x00400h 0x00400h 0x007FFEh 0x00400h 0x007FFEh 0x00400h 0x007FFEh 0x00400h 0x007FFEh 0x00400h 0x007FFEh 0x00400h 0x00400h 0x00400h 0x00400h	VS = 256 IW 0x00000h 0x0001FEh 0x000200h BS = 768 IW 0x0007FEh 0x000800h SS = 3072 IW 0x001FEh 0x00200h 0x0007FEh 0x00200h 0x001FFEh 0x00200h 0x00157FEh 0x00800h 0x003FFEh 0x007FEh 0x007FEh 0x00400h 0x007FEh 0x00400h 0x007FEh 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x00407FEh 0x007FFEh	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x003FFEh 0x003FFEh 0x007FEh GS = 39936 IW 0x0157FEh	VS = 256 IW 0x000000h 0x0001EEh 0x000200h 0x000800h 0x001FEh 0x000800h 0x001FEh 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x00200h 0x00200h 0x00200h GS = 35840 IW 0x000000 0x00157EEh
SSS<2:0> = x01 8K	VS = 256 IW 0x00000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x00000h SS = 7936 IW 0x00400h 0x003FFEh 0x004000h 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x007FFEh 0x01000h 0x01000h 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh BS = 768 IW 0x000200h 0x0007FEh 0x0007FEh 0x0000h 0x001FFEh 0x00200h 0x0007FFEh 0x00200h 0x0007FFEh 0x00200h 0x003FFEh 0x007FFEh 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x00800h 0x007FFEh 0x0000h 0x007FFEh 0x0000h 0x007FFEh 0x001000h 0x010000h	VS = 256 IW 0x000000h BS = 3840 IW 0x000200h 0x000200h 0x0007FEh 0x000800h 0x000800h 0x00000h 0x0007FEh 0x00200h 0x000800h 0x00200h 0x000800h 0x002000h 0x002000h 0x00000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x002000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x007FFEh 0x00000h 0x007FFEh 0x0010000h 0x010000h 0x010000h 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x002000h BS = 7936 IW 0x0000200h 0x003FFEh 0x004000h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x007FFEh 0x0010000h GS = 35840 IW 0x0157FEh
SSS<2:0> = x00 16K	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x00200h 0x001FFEh 0x00200h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h SS = 16128 IW 0x000FFEh 0x008000h 0x007FFEh 0x008000h GS = 27648 IW 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x000800h 0x0007FEh BS = 768 IW 0x000800h 0x0007FEh 0x00200h 0x003FFEh SS = 15360 IW 0x004000h 0x007FEh GS = 27648 IW 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x000800h 0x001FFEh 0x00200h 0x003FFEh 0x00200h 0x003FFEh 0x004000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h 0x007FFEh 0x008000h GS = 12288 IW 0x004000h 0x007FFEh 0x008000h GS = 27648 IW 0x0157FEh	VS = 256 IW 0x000000h 0x0001FEh 0x000200h 0x0007FEh 0x00800h 0x001FEFh 0x002000h 0x002000h 0x002000h 0x002000h 0x007FEh 0x004000h 0x007FFEh 0x004000h 0x007FFEh 0x004000h 0x007FFEh 0x004000h SS = 8192 IW 0x007FFEh 0x004000h 0x007FFEh 0x0010000h GS = 27648 IW 0x0157FEh

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NOTES:

			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions
		ADC Accuracy (12-bit Mode	e) – Meas	uremen	ts with e	xternal	VREF+/VREF-
AD20a	Nr	Resolution ⁽¹⁾	1	2 data bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22a	DNL	Differential Nonlinearity	> -1	-	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23a	Gerr	Gain Error	—	3.4	10	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
AD24a	EOFF	Offset Error	—	0.9	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25a	—	Monotonicity	_	_	—	_	Guaranteed
		ADC Accuracy (12-bit Mode	e) – Meas	uremen	ts with i	nternal V	VREF+/VREF-
AD20a	Nr	Resolution ⁽¹⁾	1	2 data bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2		+2	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22a	DNL	Differential Nonlinearity	> -1		< 1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23a	Gerr	Gain Error	2	10.5	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	EOFF	Offset Error	2	3.8	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25a	—	Monotonicity			—	—	Guaranteed
		Dynamic	Performa	ance (12	-bit Mod	e)	
AD30a	THD	Total Harmonic Distortion	—		-75	dB	—
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	—	dB	_
AD32a	SFDR	Spurious Free Dynamic Range	80	_	_	dB	_
AD33a	Fnyq	Input Signal Bandwidth	_		250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	_

TABLE 28-40: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Injection currents > |0| can affect the ADC results by approximately 4 to 6 counts (i.e., VIH source > (VDD + 0.3V) or VIL source < (Vss – 0.3V).

AC Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) CHARACTERISTICS Operating temperature -40°C ≤TA ≤+150°C for High Temperature				tated)			
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period ⁽¹⁾	147		_	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate ⁽¹⁾			400	Ksps	_

TABLE 29-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 29-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period ⁽¹⁾	104	—	—	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate ⁽¹⁾	_	_	800	Ksps	

Note 1: These parameters are characterized but not tested in manufacturing.

Revision C (May 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSCI to OSC1 and OSCO to OSC2
- Changed all instances of VDDCORE and VDDCORE/ VCAP to VCAP/VDDCORE

The other changes are referenced by their respective section in the following table.

TABLE A-2:	MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Microcontrollers"	Updated all pin diagrams to denote the pin voltage tolerance (see " Pin Diagrams ").
	Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to Vss.
Section 1.0 "Device Overview"	Updated AVDD in the PINOUT I/O Descriptions (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Microcontrollers"	Added new section to the data sheet that provides guidelines on getting started with 16-bit Digital Signal Controllers.
	Added Peripheral Pin Select (PPS) capability column to Pinout I/O Descriptions (see Table 1-1).
Section 3.0 "CPU"	Updated CPU Core Block Diagram with a connection from the DSP Engine to the Y Data Bus (see Figure 3-1).
Section 4.0 "Memory Organization"	Updated Reset value for CORCON in the CPU Core Register Map (see Table 4-1).
	Updated Reset value for IPC15 in the Interrupt Controller Register Map (see Table 4-4).
	Removed the FLTA1IE bit (IEC3) from the Interrupt Controller Register Map (see Table 4-4).
	Updated bit locations for RPINR25 in the Peripheral Pin Select Input Register Map (see Table 4-19).
	Updated the Reset value for CLKDIV in the System Control Register Map (see Table 4-31).
Section 5.0 "Flash Program Memory"	Updated Section 5.3 "Programming Operations" with programming time formula.
Section 9.0 "Oscillator Configuration"	Updated the Oscillator System Diagram and added Note 2 (see Figure 9-1).
	Updated default bit values for DOZE<2:0> and FRCDIV<2:0> in the Clock Divisor (CLKDIV) Register (see Register 9-2).
	Added a paragraph regarding FRC accuracy at the end of Section 9.1.1 " System Clock Sources ".
	Added Note 3 to Section 9.2.2 "Oscillator Switching Sequence".
	Added Note 1 to the FRC Oscillator Tuning (OSCTUN) Register (see Register 9-4).

TABLE A-4:	MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 "High Temperature Electrical Characteristics"	Updated all ambient temperature end range values to +150°C throughout the chapter.
	Updated the storage temperature end range to +160°C.
	Updated the maximum junction temperature from +145°C to +155°C.
	Updated the maximum values for High Temperature Devices in the Thermal Operating Conditions (see Table 29-2).
	Updated the ADC Module Specifications (12-bit Mode), removing all parameters with the exception of HAD33a (see Table 29-14).
	Updated the ADC Module Specifications (10-bit Mode), removing all parameters with the exception of HAD33b (see Table 29-16).
"Product Identification System"	Updated the end range temperature value for H (High) devices.