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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj64gp502-i-sp

Table of Contents

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 Product Families	2
1.0 Device Overview	9
2.0 Guidelines for Getting Started with 16-bit Microcontrollers	13
3.0 CPU	17
4.0 Memory Organization	25
5.0 Flash Program Memory	53
6.0 Resets	59
7.0 Interrupt Controller	69
8.0 Direct Memory Access (DMA)	107
9.0 Oscillator Configuration	119
10.0 Power-Saving Features	129
11.0 I/O Ports	135
12.0 Timer1	161
13.0 Timer2/3 And Timer4/5 Feature	165
14.0 Input Capture	171
15.0 Output Compare	175
16.0 Serial Peripheral Interface (SPI)	179
17.0 Inter-Integrated Circuit™ (I ² C™)	185
18.0 Universal Asynchronous Receiver Transmitter (UART)	193
19.0 Enhanced CAN (ECAN™) Module	199
20.0 10-bit/12-bit Analog-to-Digital Converter (ADC1)	227
21.0 Comparator Module	241
22.0 Real-Time Clock and Calendar (RTCC)	247
23.0 Programmable Cyclic Redundancy Check (CRC) Generator	259
24.0 Parallel Master Port (PMP)	265
25.0 Special Features	273
26.0 Instruction Set Summary	283
27.0 Development Support	291
28.0 Electrical Characteristics	295
29.0 High Temperature Electrical Characteristics	345
32.0 DC and AC Device Characteristics Graphs	357
33.0 Packaging Information	361
Appendix A: Revision History	371
The Microchip Web Site	385
Customer Change Notification Service	385
Customer Support	385
Reader Response	386
Product Identification System	387

FIGURE 7-1: PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 INTERRUPT VECTOR TABLE

Decreasing Natural Order Priority ↓	Reset – GOTO Instruction	0x000000	Interrupt Vector Table (IVT) ⁽¹⁾
	Reset – GOTO Address	0x000002	
	Reserved	0x000004	
	Oscillator Fail Trap Vector		
	Address Error Trap Vector		
	Stack Error Trap Vector		
	Math Error Trap Vector		
	DMA Error Trap Vector		
	Reserved		
	Reserved		
	Interrupt Vector 0	0x000014	
	Interrupt Vector 1		
	~		
	~		
	~		
	Interrupt Vector 52	0x00007C	
	Interrupt Vector 53	0x00007E	
	Interrupt Vector 54	0x000080	
	~		
	~		
	~		
	Interrupt Vector 116	0x0000FC	Alternate Interrupt Vector Table (AIVT) ⁽¹⁾
	Interrupt Vector 117	0x0000FE	
	Reserved	0x000100	
	Reserved	0x000102	
	Reserved		
	Oscillator Fail Trap Vector		
	Address Error Trap Vector		
	Stack Error Trap Vector		
	Math Error Trap Vector		
	DMA Error Trap Vector		
	Reserved		
	Reserved		
	Interrupt Vector 0	0x000114	
	Interrupt Vector 1		
	~		
	~		
	~		
	Interrupt Vector 52	0x00017C	
	Interrupt Vector 53	0x00017E	
	Interrupt Vector 54	0x000180	
	~		
	~		
	~		
	Interrupt Vector 116		
	Interrupt Vector 117	0x0001FE	
	Start of Code	0x000200	

Note 1: See Table 7-1 for the list of implemented interrupt vectors.

TABLE 7-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
0	0x000004	0x000104	Reserved
1	0x000006	0x000106	Oscillator Failure
2	0x000008	0x000108	Address Error
3	0x00000A	0x00010A	Stack Error
4	0x00000C	0x00010C	Math Error
5	0x00000E	0x00010E	DMA Error
6-7	0x000010-0x000012	0x000110-0x000112	Reserved
8	0x000014	0x000114	INT0 – External Interrupt 0
9	0x000016	0x000116	IC1 – Input Capture 1
10	0x000018	0x000118	OC1 – Output Compare 1
11	0x00001A	0x00011A	T1 – Timer1
12	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	0x00001E	0x00011E	IC2 – Input Capture 2
14	0x000020	0x000120	OC2 – Output Compare 2
15	0x000022	0x000122	T2 – Timer2
16	0x000024	0x000124	T3 – Timer3
17	0x000026	0x000126	SPI1E – SPI1 Error
18	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	0x00002A	0x00012A	U1RX – UART1 Receiver
20	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	0x00002E	0x00012E	ADC1 – ADC 1
22	0x000030	0x000130	DMA1 – DMA Channel 1
23	0x000032	0x000132	Reserved
24	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	0x000038	0x000138	CM – Comparator Interrupt
27	0x00003A	0x00013A	CN – Change Notification Interrupt
28	0x00003C	0x00013C	INT1 – External Interrupt 1
29	0x00003E	0x00013E	Reserved
30	0x000040	0x000140	IC7 – Input Capture 7
31	0x000042	0x000142	IC8 – Input Capture 8
32	0x000044	0x000144	DMA2 – DMA Channel 2
33	0x000046	0x000146	OC3 – Output Compare 3
34	0x000048	0x000148	OC4 – Output Compare 4
35	0x00004A	0x00014A	T4 – Timer4
36	0x00004C	0x00014C	T5 – Timer5
37	0x00004E	0x00014E	INT2 – External Interrupt 2
38	0x000050	0x000150	U2RX – UART2 Receiver
39	0x000052	0x000152	U2TX – UART2 Transmitter
40	0x000054	0x000154	SPI2E – SPI2 Error
41	0x000056	0x000156	SPI2 – SPI2 Transfer Done
42	0x000058	0x000158	C1RX – ECAN1 RX Data Ready
43	0x00005A	0x00015A	C1 – ECAN1 Event
44	0x00005C	0x00015C	DMA3 – DMA Channel 3
45-52	0x00005E-0x00006C	0x00015E-0x00016C	Reserved
53	0x00006E	0x00016E	PMP – Parallel Master Port
54	0x000070	0x000170	DMA – DMA Channel 4

TABLE 7-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	IVT Address	AIVT Address	Interrupt Source
55-68	0x000072-0x00008C	0x000172-0x00018C	Reserved
69	0x00008E	0x00018E	DMA5 – DMA Channel 5
70	0x000090	0x000190	RTCC – Real Time Clock
71-72	0x000092-0x000094	0x000192-0x000194	Reserved
73	0x000096	0x000196	U1E – UART1 Error
74	0x000098	0x000198	U2E – UART2 Error
75	0x00009A	0x00019A	CRC – CRC Generator Interrupt
76	0x00009C	0x00019C	DMA6 – DMA Channel 6
77	0x00009E	0x00019E	DMA7 – DMA Channel 7
78	0x0000A0	0x0001A0	C1TX – ECAN1 TX Data Request
79-126	0x0000A2-0x0000FE	0x0001A2-0x0001FE	Reserved

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

- bit 2 **CMIF:** Comparator Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 1 **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 0 **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred

REGISTER 7-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	C1TXIF ⁽¹⁾	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-7 **Unimplemented:** Read as '0'
- bit 6 **C1TXIF:** ECAN1 Transmit Data Request Interrupt Flag Status bit⁽¹⁾
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 5 **DMA7IF:** DMA Channel 7 Data Transfer Complete Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 4 **DMA6IF:** DMA Channel 6 Data Transfer Complete Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 3 **CRCIF:** CRC Generator Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 2 **U2EIF:** UART2 Error Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 1 **U1EIF:** UART1 Error Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 0 **Unimplemented:** Read as '0'

Note 1: Interrupts disabled on devices without ECAN™ modules.

REGISTER 7-23: IPC8: INTERRUPT PRIORITY CONTROL REGISTER 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	C1IP<2:0> ⁽¹⁾			—	C1RXIP<2:0> ⁽¹⁾		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI2IP<2:0>			—	SPI2EIP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **C1IP<2:0>:** ECAN1 Event Interrupt Priority bits⁽¹⁾
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **C1RXIP<2:0>:** ECAN1 Receive Data Ready Interrupt Priority bits⁽¹⁾
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI2IP<2:0>:** SPI2 Event Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SPI2EIP<2:0>:** SPI2 Error Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

Note 1: Interrupts disabled on devices without ECAN™ modules.

REGISTER 8-5: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PAD<15:0>**: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-6: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CNT<9:8> ⁽²⁾	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **CNT<9:0>**: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: Number of DMA transfers = CNT<9:0> + 1.

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 39. "Oscillator (Part III)"** (DS70216) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

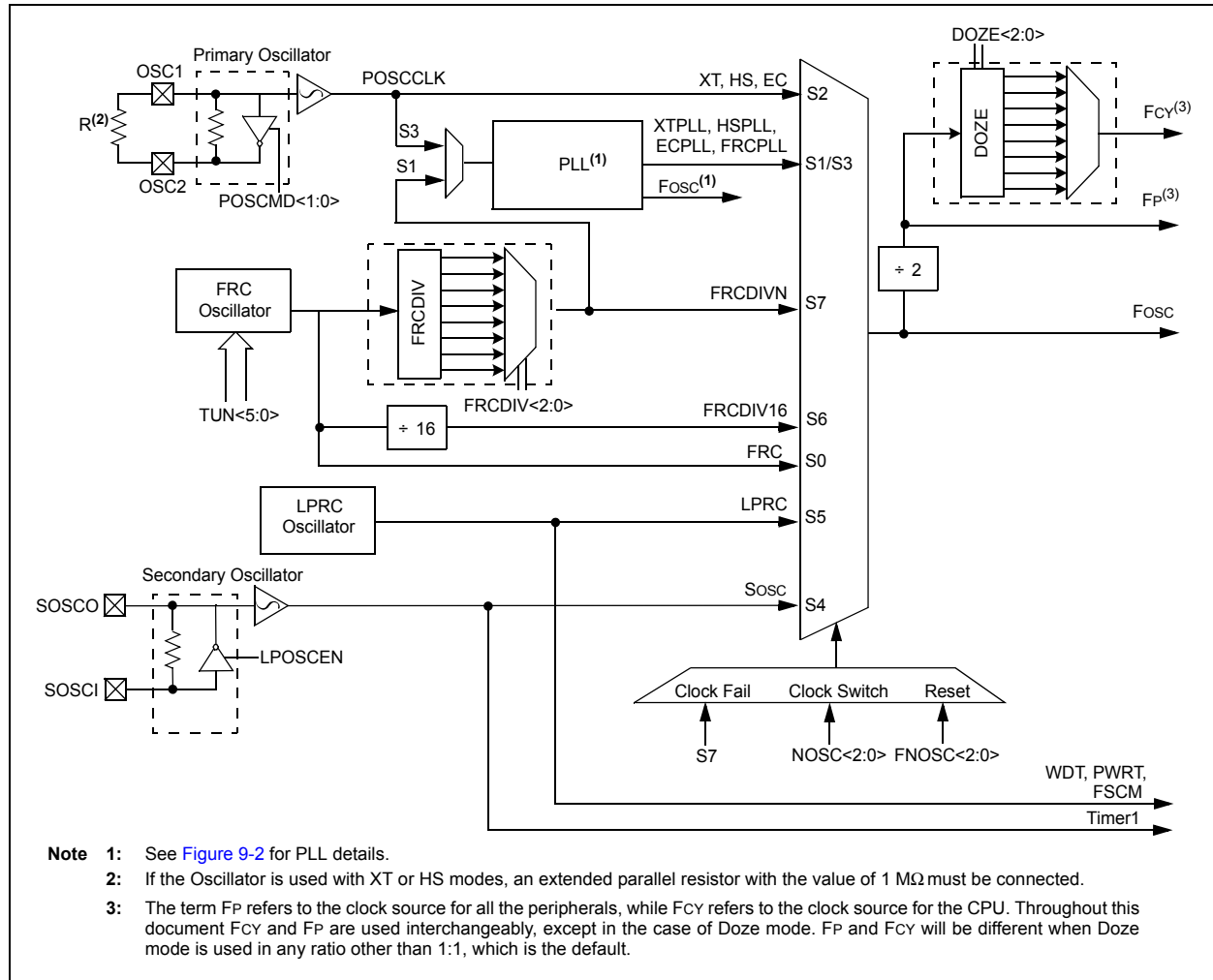
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 oscillator system provides:

- External and internal oscillator options as clock sources
- An on-chip Phase-Locked Loop (PLL) to scale the internal operating frequency to the required system clock frequency
- An internal FRC oscillator that can also be used with the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- An Oscillator Control register (OSCCON)
- Nonvolatile Configuration bits for main oscillator selection.

A simplified diagram of the oscillator system is shown in **Figure 9-1**.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



11.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24H devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

11.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) the IOLOCK bit as a single operation.

Note: MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:

```
__builtin_write_OSCCONL(value)
__builtin_write_OSCCONH(value)
```

See MPLAB Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

11.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset is triggered.

11.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY Configuration bit (FOSC<5>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

15.3 Output Compare Control Registers

REGISTER 15-1: OCxCON: OUTPUT COMPAREx CONTROL REGISTER (x = 1, 2, 3 OR 4)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	R-0 HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM<2:0>		
bit 7						bit 0	

Legend:	HC = Cleared in Hardware	HS = Set in Hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **OCSIDL:** Stop Output Compare in Idle Mode Control bit
 1 = Output Compare x halts in CPU Idle mode
 0 = Output Compare x continues to operate in CPU Idle mode
- bit 12-5 **Unimplemented:** Read as '0'
- bit 4 **OCFLT:** PWM Fault Condition Status bit
 1 = PWM Fault condition has occurred (cleared in hardware only)
 0 = No PWM Fault condition has occurred
 (This bit is only used when OCM<2:0> = 111)
- bit 3 **OCTSEL:** Output Compare Timer Select bit
 1 = Timer3 is the clock source for Compare x
 0 = Timer2 is the clock source for Compare x
- bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
 111 = PWM mode on OCx, Fault pin enabled
 110 = PWM mode on OCx, Fault pin disabled
 101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
 100 = Initialize OCx pin low, generate single output pulse on OCx pin
 011 = Compare event toggles OCx pin
 010 = Initialize OCx pin high, compare event forces OCx pin low
 001 = Initialize OCx pin low, compare event forces OCx pin high
 000 = Output compare channel is disabled

18.3 UART Control Registers

REGISTER 18-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾	—	USIDL	IREN ⁽²⁾	RTSMD	—	UEN<1:0>	
bit 15							bit 8

R/W-0 HC	R/W-0	R/W-0 HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL
bit 7							bit 0

Legend:	HC = Hardware cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **UARTEN:** UARTx Enable bit⁽¹⁾
 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽²⁾
 1 = IrDA encoder and decoder enabled
 0 = IrDA encoder and decoder disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
 1 = UxRTS pin in Simplex mode
 0 = UxRTS pin in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Enable bits
 11 = UxTX, UxRX and BCLK pins are enabled and used; UxCTS pin controlled by port latches
 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin controlled by port latches
 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLK pins controlled by port latches
- bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
 1 = UARTx continues to sample the UxRX pin; interrupt generated on falling edge; bit cleared in hardware on following rising edge
 0 = No wake-up enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
 1 = Enable Loopback mode
 0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
 0 = Baud rate measurement disabled or completed

Note 1: Refer to **Section 17. “UART”** (DS70232) in the “*dsPIC33F/PIC24H Family Reference Manual*” for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

19.5 ECAN Control Registers

REGISTER 19-1: CICTRL1: ECAN™ CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	—	REQOP<2:0>		
bit 15					bit 8		

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7				bit 0			

Legend:	C = Writable bit, but only '0' can be written to clear the bit			r = Bit is Reserved			
R = Readable bit	W = Writable bit			U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set			'0' = Bit is cleared		x = Bit is unknown	

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
 1 = Signal all transmit buffers to abort transmission
 0 = Module will clear this bit when all transmissions are aborted
- bit 11 **Reserved:** Do not use
- bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
 000 = Set Normal Operation mode
 001 = Set Disable mode
 010 = Set Loopback mode
 011 = Set Listen Only Mode
 100 = Set Configuration mode
 101 = Reserved
 110 = Reserved
 111 = Set Listen All Messages mode
- bit 7-5 **OPMODE<2:0>:** Operation Mode bits
 000 = Module is in Normal Operation mode
 001 = Module is in Disable mode
 010 = Module is in Loopback mode
 011 = Module is in Listen Only mode
 100 = Module is in Configuration mode
 101 = Reserved
 110 = Reserved
 111 = Module is in Listen All Messages mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
 1 = Enable input capture based on CAN message receive
 0 = Disable CAN capture
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
 1 = Use filter window
 0 = Use buffer window

25.2 On-Chip Voltage Regulator

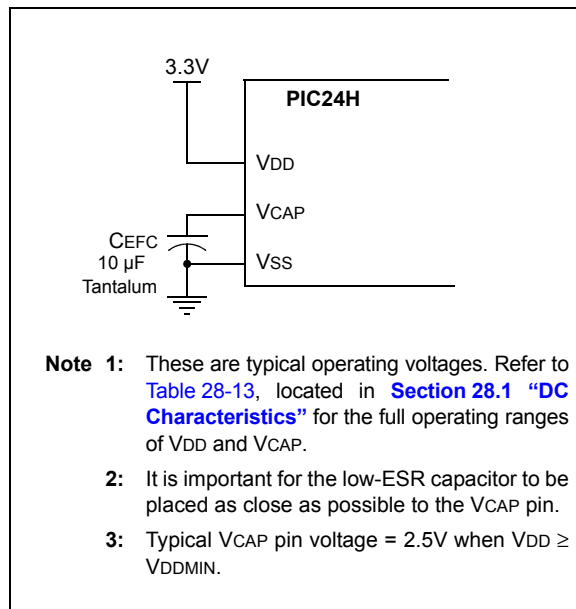
All of the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 family incorporate an on-chip voltage regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 Ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 25-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 28-13 located in Section 28.1 “DC Characteristics”.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 25-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



25.3 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is ‘1’.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 28-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DI10	V _{IL}	Input Low Voltage I/O pins	V _{SS}	—	0.2 V _{DD}	V	PMPTTL = 1
DI11		PMP pins	V _{SS}	—	0.15 V _{DD}	V	
DI15		MCLR	V _{SS}	—	0.2 V _{DD}	V	
DI16		I/O Pins with OSC1 or SOSC1	V _{SS}	—	0.2 V _{DD}	V	
DI18		I/O Pins with SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	
DI19		I/O Pins with SDAx, SCLx	V _{SS}	—	0.8	V	
DI20	V _{IH}	Input High Voltage I/O Pins Not 5V Tolerant ⁽⁴⁾	0.7 V _{DD}	—	V _{DD}	V	—
		I/O Pins 5V Tolerant ⁽⁴⁾	0.7 V _{DD}	—	5.5	V	
DI21		I/O Pins Not 5V Tolerant with PMP ⁽⁴⁾	0.24 V _{DD} + 0.8	—	V _{DD}	V	
		I/O Pins 5V Tolerant with PMP ⁽⁴⁾	0.24 V _{DD} + 0.8	—	5.5	V	
DI28		SDAx, SCLx	0.7 V _{DD}	—	5.5	V	
DI29		SDAx, SCLx	2.1	—	5.5	V	
DI30	ICNPU	CNx Pull-up Current	50	250	400	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See “[Pin Diagrams](#)” for the 5V tolerant I/O pins.
- 5:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 7:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 28-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(5,8)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , M _{CLR} , V _{CAP} , SOSC _I , SOSC _O , and RB14
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(6,7,8)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , M _{CLR} , V _{CAP} , SOSC _I , SOSC _O , RB14, and digital 5V-tolerant designated pins
DI60c	I _{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁹⁾	—	+20 ⁽⁹⁾	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins $(I_{ICL} + I_{ICH}) \leq I_{ICT}$

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

- 2:** The leakage current on the M_{CLR} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See “[Pin Diagrams](#)” for the 5V tolerant I/O pins.
- 5:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 7:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 8:** Injection currents > |0| can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 28-17: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

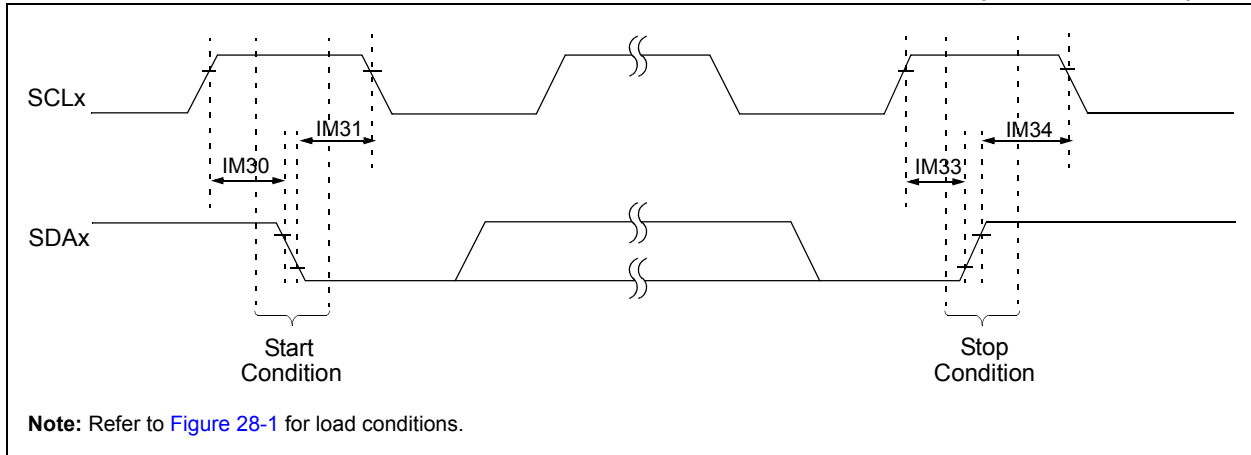
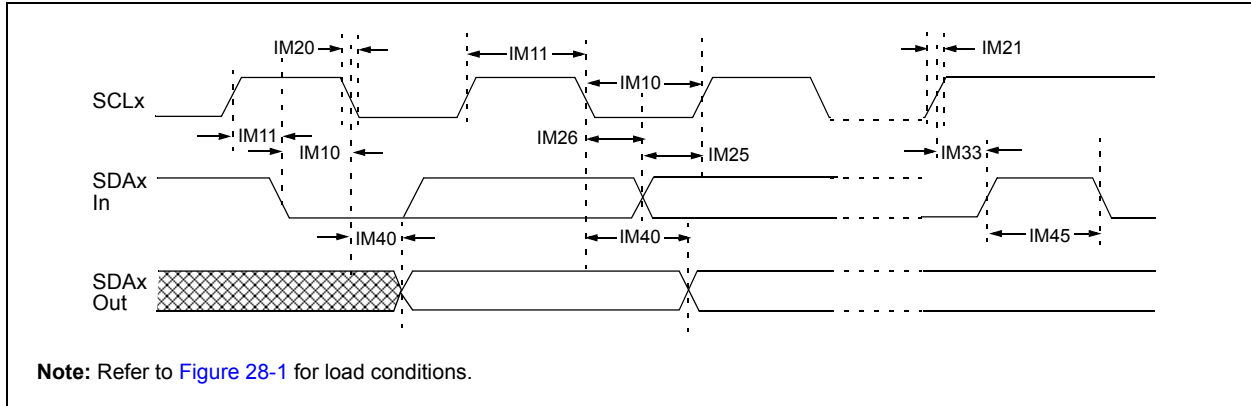


FIGURE 28-18: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: V_{OH} – 2x DRIVER PINS

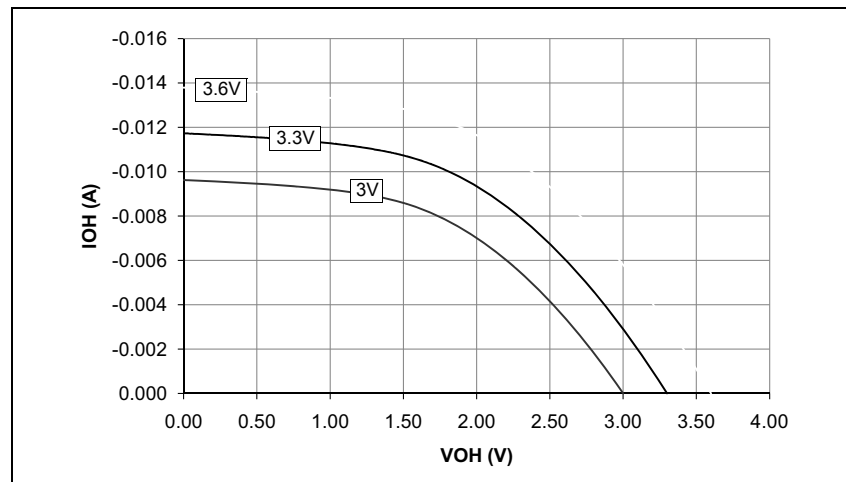


FIGURE 32-3: V_{OH} – 8x DRIVER PINS

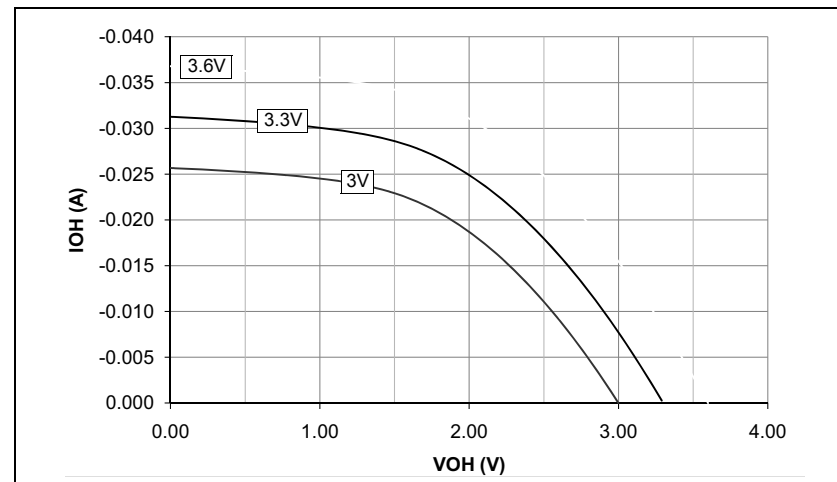


FIGURE 32-2: V_{OH} – 4x DRIVER PINS

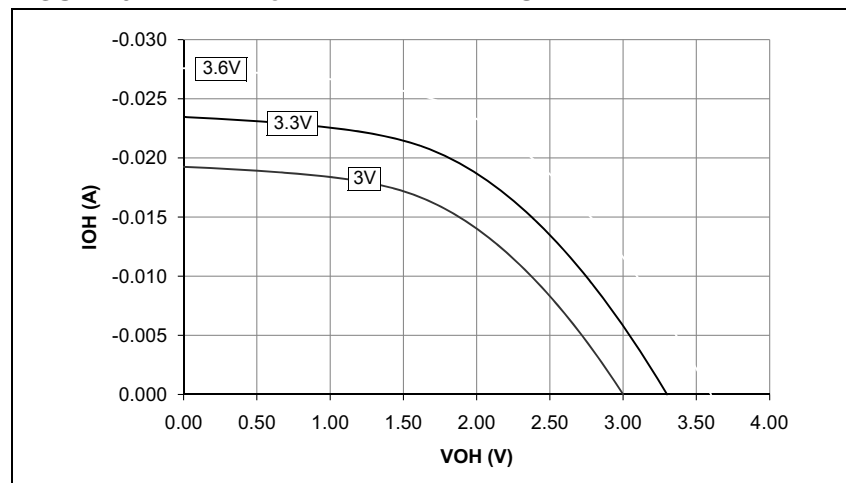


FIGURE 32-4: V_{OH} – 16x DRIVER PINS

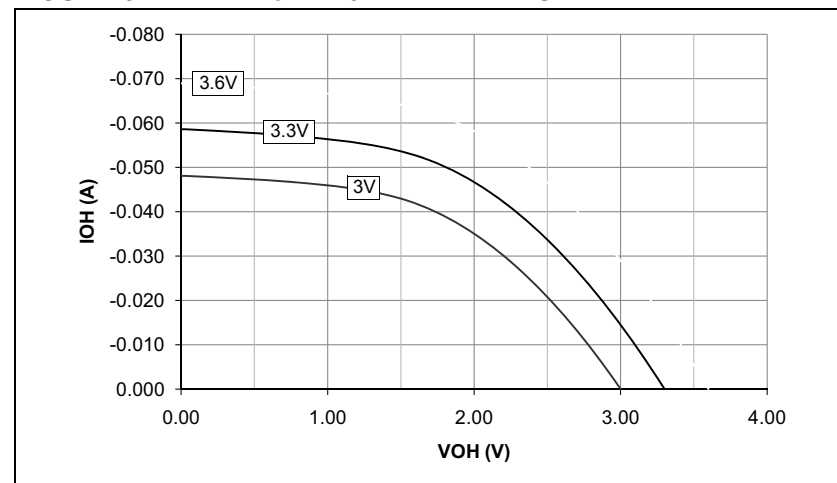


TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 28.0 “Electrical Characteristics”	<p>Updated Typical values for Thermal Packaging Characteristics (see Table 28-3).</p> <p>Updated Min and Max values for parameter DC12 (RAM Data Retention Voltage) and added Note 4 (see Table 28-4).</p> <p>Updated Power-Down Current Max values for parameters DC60b and DC60c (see Table 28-7).</p> <p>Updated Characteristics for I/O Pin Input Specifications (see Table 28-9).</p> <p>Updated Program Memory values for parameters 136, 137 and 138 (renamed to 136a, 137a and 138a), added parameters 136b, 137b and 138b, and added Note 2 (see Table 28-12).</p> <p>Added parameter OS42 (GM) to the External Clock Timing Requirements (see Table 28-16).</p> <p>Updated Watchdog Timer Time-out Period parameter SY20 (see Table 28-21).</p>

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<div style="text-align: center; margin-bottom: 10px;"> PIC 24 HJ 32 GP3 02 T E / SP - XXX </div> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Microchip Trademark _____</p> <p>Architecture _____</p> <p>Flash Memory Family _____</p> <p>Program Memory Size (KB) _____</p> <p>Product Group _____</p> <p>Pin Count _____</p> <p>Tape and Reel Flag (if applicable) _____</p> <p>Temperature Range _____</p> <p>Package _____</p> <p>Pattern _____</p> </div> <div style="width: 5%; text-align: center;"> </div> <div style="width: 50%; border-left: 1px solid black; padding-left: 10px;"> <p>Examples:</p> <p>a) PIC24HJ32GP302-E/SP: General Purpose PIC24H, 32 KB program memory, 28-pin, Extended temperature, SPDIP package.</p> </div> </div>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%;">Architecture:</td> <td style="width: 10%;">24</td> <td style="width: 10%;">=</td> <td>16-bit Microcontroller</td> </tr> <tr> <td>Flash Memory Family:</td> <td>HJ</td> <td>=</td> <td>Flash program memory, 3.3V</td> </tr> <tr> <td>Product Group:</td> <td>GP2</td> <td>=</td> <td>General Purpose family</td> </tr> <tr> <td></td> <td>GP3</td> <td>=</td> <td>General Purpose family</td> </tr> <tr> <td></td> <td>GP8</td> <td>=</td> <td>General Purpose family</td> </tr> <tr> <td>Pin Count:</td> <td>02</td> <td>=</td> <td>28-pin</td> </tr> <tr> <td></td> <td>04</td> <td>=</td> <td>44-pin</td> </tr> <tr> <td>Temperature Range:</td> <td>I</td> <td>=</td> <td>-40° C to +85° C (Industrial)</td> </tr> <tr> <td></td> <td>E</td> <td>=</td> <td>-40° C to +125° C (Extended)</td> </tr> <tr> <td></td> <td>H</td> <td>=</td> <td>-40° C to +150° C (High)</td> </tr> <tr> <td>Package:</td> <td>SP</td> <td>=</td> <td>Skinny Plastic Dual In-Line - 300 mil body (SPDIP)</td> </tr> <tr> <td></td> <td>SO</td> <td>=</td> <td>Plastic Small Outline - Wide - 300 mil body (SOIC)</td> </tr> <tr> <td></td> <td>ML</td> <td>=</td> <td>Plastic Quad, No Lead Package - 8x8 mm body (QFN)</td> </tr> <tr> <td></td> <td>MM</td> <td>=</td> <td>Plastic Quad, No Lead Package - 6x6x0.9 mm body (QFN-S)</td> </tr> <tr> <td></td> <td>PT</td> <td>=</td> <td>Plastic Thin Quad Flatpack - 10x10x1 mm body (TQFP)</td> </tr> </table>	Architecture:	24	=	16-bit Microcontroller	Flash Memory Family:	HJ	=	Flash program memory, 3.3V	Product Group:	GP2	=	General Purpose family		GP3	=	General Purpose family		GP8	=	General Purpose family	Pin Count:	02	=	28-pin		04	=	44-pin	Temperature Range:	I	=	-40° C to +85° C (Industrial)		E	=	-40° C to +125° C (Extended)		H	=	-40° C to +150° C (High)	Package:	SP	=	Skinny Plastic Dual In-Line - 300 mil body (SPDIP)		SO	=	Plastic Small Outline - Wide - 300 mil body (SOIC)		ML	=	Plastic Quad, No Lead Package - 8x8 mm body (QFN)		MM	=	Plastic Quad, No Lead Package - 6x6x0.9 mm body (QFN-S)		PT	=	Plastic Thin Quad Flatpack - 10x10x1 mm body (TQFP)
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