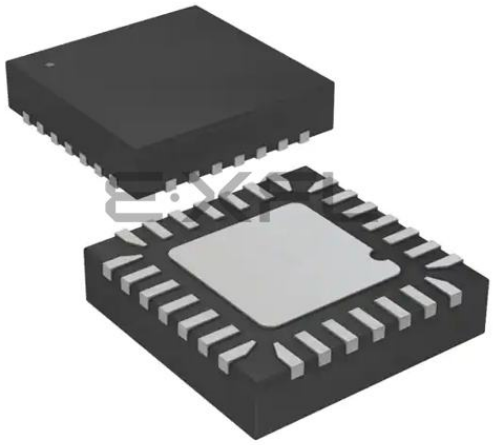


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | I²C, SPI |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 4KB (2K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VFQFN Exposed Pad |
| Supplier Device Package | 28-VQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/attiny48-mmhr |

# 1. Pin Configurations

**Figure 1-1.** Pinout of ATtiny48/88

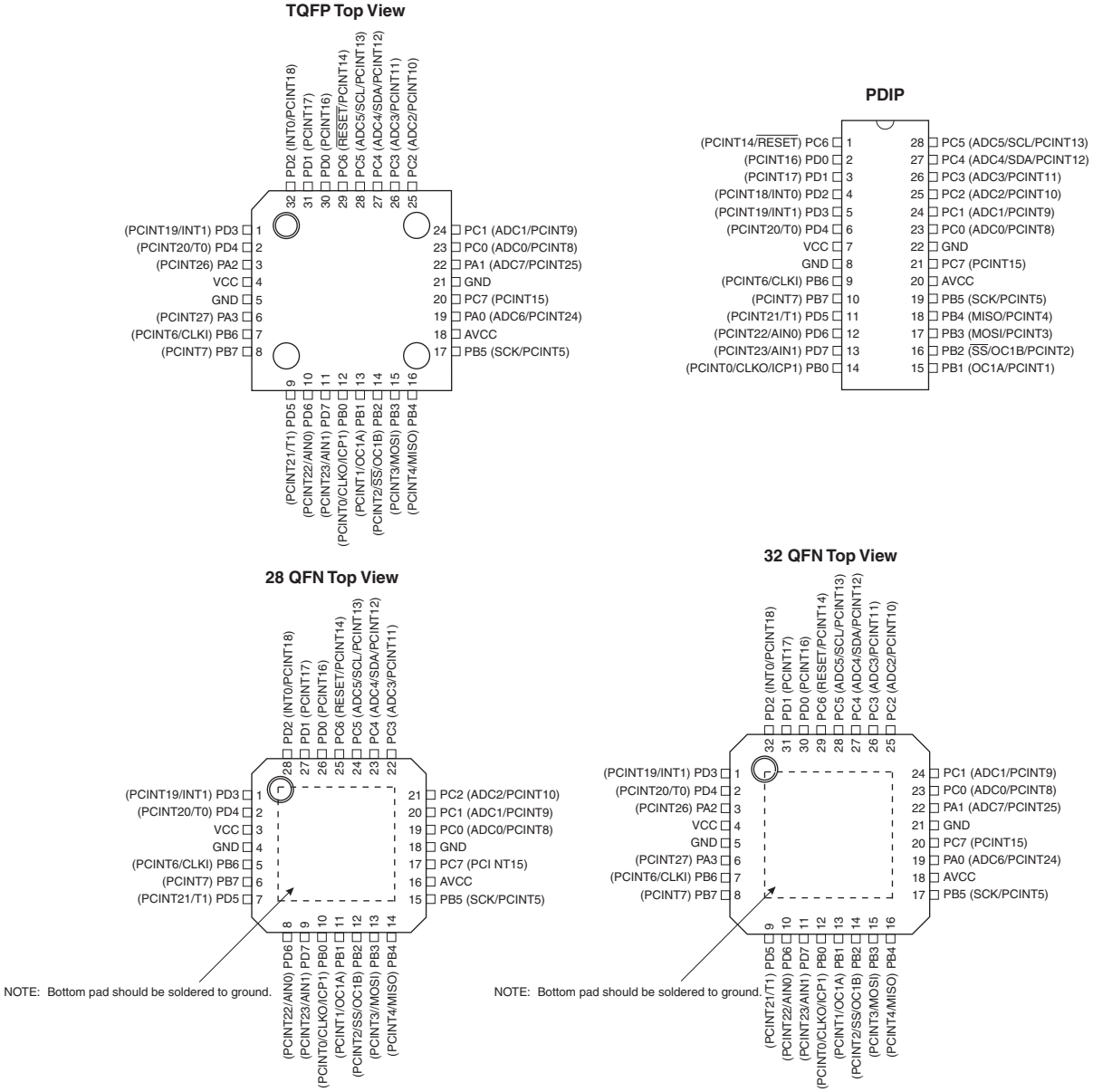



**Table 1-1.** 32 UFBGA Top View. See page 288.

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | PD2 | PD1 | PC6 | PC4 | PC2 | PC1 |
| **B** | PD3 | PD4 | PD0 | PC5 | PC3 | PC0 |
| **C** | GND | PA2 | | | PA1 | GND |
| **D** | VCC | PA3 | | | PC7 | PA0 |
| **E** | PB6 | PD6 | PB0 | PB2 | AVCC | PB5 |
| **F** | PB7 | PD5 | PD7 | PB1 | PB3 | PB4 |

minimum pulse length is given in Table 22-3 on page 209. Shorter pulses are not guaranteed to generate a reset.

The various special features of Port C are elaborated in "Alternate Functions of Port C" on page 72.

### 1.1.8 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PD[7:4] output buffers have symmetrical drive characteristics with both sink and source capabilities, while the PD[3:0] output buffers have high sink capabilities. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

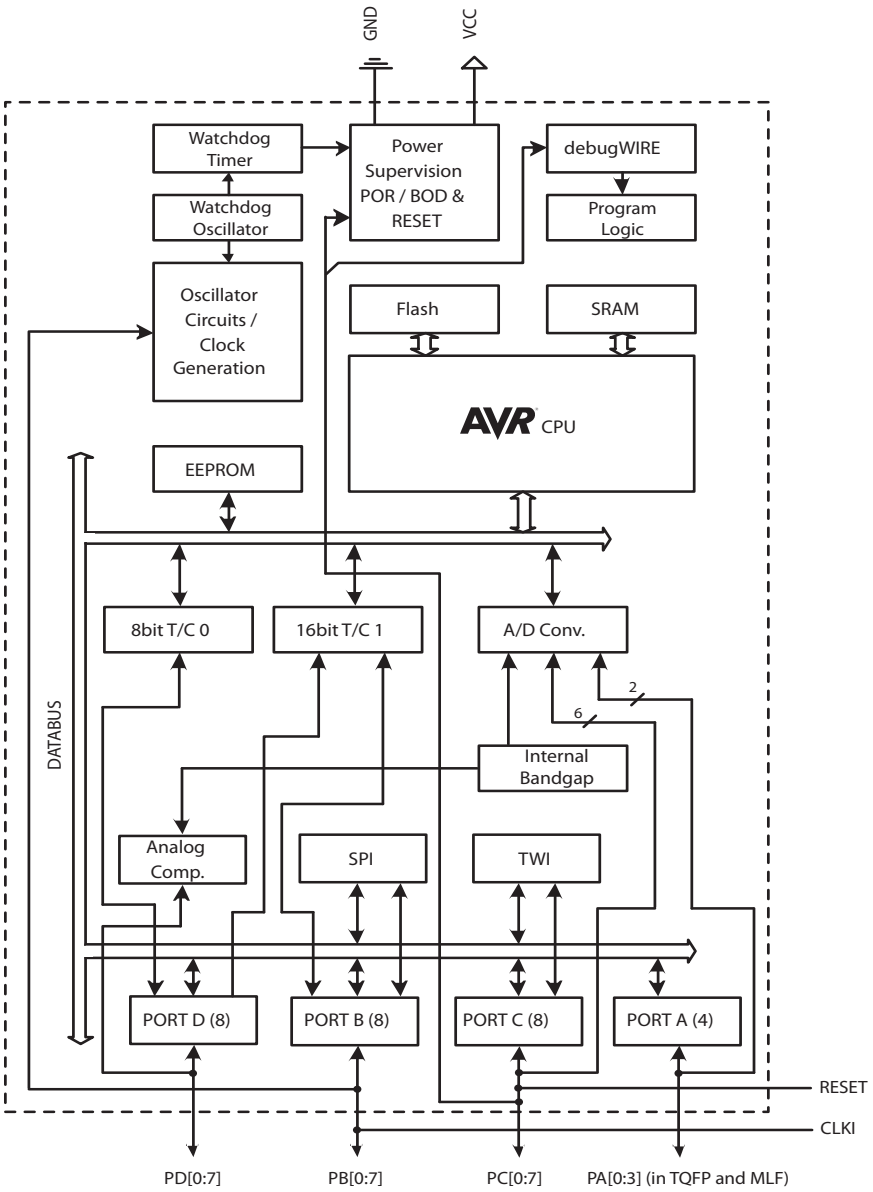
The various special features of Port D are elaborated in "Alternate Functions of Port D" on page 75.

# 2. Overview

The ATtiny48/88 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny48/88 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## 2.1 Block Diagram

**Figure 2-1.** Block Diagram




The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny48/88 provides the following features:

- 4/8K bytes of In-System Programmable Flash
- 64/64 bytes EEPROM
- 256/512 bytes SRAM
- 24 general purpose I/O lines
  - 28 in 32-lead TQFP, 32-pad QFN, and 32-ball UFBGA packages
- 32 general purpose working registers
- Two flexible Timer/Counters with compare modes
- Internal and external interrupts
- A byte-oriented, 2-wire serial interface
- An SPI serial port
- A 6-channel, 10-bit ADC
  - 8 in 32-lead TQFP, 32-pad QFN, and 32-ball UFBGA packages
- A programmable Watchdog Timer with internal oscillator
- Three software selectable power saving modes.

The device includes the following modes for saving power:

- Idle mode: stops the CPU while allowing the timer/counter, ADC, analog comparator, SPI, TWI, and interrupt system to continue functioning
- ADC Noise Reduction mode: minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC
- Power-down mode: registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an on-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Flash memory. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny48/88 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny48/88 AVR is supported by a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators and evaluation kits.

## 2.2 Comparison Between ATtiny48 and ATtiny88

The ATtiny48 and ATtiny88 differ only in memory sizes, as summarised in Table 2-1, below.

**Table 2-1.** Memory Size Summary

| Device | Flash | EEPROM | RAM |
|---|---|---|---|
| ATtiny48 | 4K Bytes | 64 Bytes | 256 Bytes |
| ATtiny88 | 8K Bytes | 64 Bytes | 512 Bytes |

# 4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0xFF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xED) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBF) | Reserved | – | – | – | – | – | – | – | – | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0xBE) | TWHSR | – | – | – | – | – | – | – | TWHS | 160 |
| (0xBD) | TWAMR | TWAM6 | TWAM5 | TWAM4 | TWAM3 | TWAM2 | TWAM1 | TWAM0 | – | 160 |
| (0xBC) | TWCR | TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | – | TWIE | 156 |
| (0xBB) | TWDR | 2-wire Serial Interface Data Register | | | | | | | | 159 |
| (0xBA) | TWAR | TWA6 | TWA5 | TWA4 | TWA3 | TWA2 | TWA1 | TWA0 | TWGCE | 159 |
| (0xB9) | TWSR | TWS7 | TWS6 | TWS5 | TWS4 | TWS3 | – | TWPS1 | TWPS0 | 158 |
| (0xB8) | TWBR | 2-wire Serial Interface Bit Rate Register | | | | | | | | 156 |
| (0xB7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA0) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9B) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9A) | Reserved | – | – | – | – | – | – | – | – | |
| (0x99) | Reserved | – | – | – | – | – | – | – | – | |
| (0x98) | Reserved | – | – | – | – | – | – | – | – | |
| (0x97) | Reserved | – | – | – | – | – | – | – | – | |
| (0x96) | Reserved | – | – | – | – | – | – | – | – | |
| (0x95) | Reserved | – | – | – | – | – | – | – | – | |
| (0x94) | Reserved | – | – | – | – | – | – | – | – | |
| (0x93) | Reserved | – | – | – | – | – | – | – | – | |
| (0x92) | Reserved | – | – | – | – | – | – | – | – | |
| (0x91) | Reserved | – | – | – | – | – | – | – | – | |
| (0x90) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8B) | OCR1BH | Timer/Counter1 – Output Compare Register B High Byte | | | | | | | | 114 |
| (0x8A) | OCR1BL | Timer/Counter1 – Output Compare Register B Low Byte | | | | | | | | 114 |
| (0x89) | OCR1AH | Timer/Counter1 – Output Compare Register A High Byte | | | | | | | | 114 |
| (0x88) | OCR1AL | Timer/Counter1 – Output Compare Register A Low Byte | | | | | | | | 114 |
| (0x87) | ICR1H | Timer/Counter1 – Input Capture Register High Byte | | | | | | | | 114 |
| (0x86) | ICR1L | Timer/Counter1 – Input Capture Register Low Byte | | | | | | | | 114 |
| (0x85) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | 113 |
| (0x84) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | 113 |
| (0x83) | Reserved | – | – | – | – | – | – | – | – | |
| (0x82) | TCCR1C | FOC1A | FOC1B | – | – | – | – | – | – | 113 |
| (0x81) | TCCR1B | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | 112 |
| (0x80) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | – | – | WGM11 | WGM10 | 110 |
| (0x7F) | DIDR1 | – | – | – | – | – | – | AIN1D | AIN0D | 163 |
| (0x7E) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D | 180 |
| (0x7D) | Reserved | – | – | – | – | – | – | – | – | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0x7C) | ADMUX | – | REFS0 | ADLAR | – | MUX3 | MUX2 | MUX1 | MUX0 | 176 |
| (0x7B) | ADCSRB | – | ACME | – | – | – | ADTS2 | ADTS1 | ADTS0 | 162, 179 |
| (0x7A) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 178 |
| (0x79) | ADCH | ADC Data Register High byte | | | | | | | | 179 |
| (0x78) | ADCL | ADC Data Register Low byte | | | | | | | | 179 |
| (0x77) | Reserved | – | – | – | – | – | – | – | – | |
| (0x76) | Reserved | – | – | – | – | – | – | – | – | |
| (0x75) | Reserved | – | – | – | – | – | – | – | – | |
| (0x74) | Reserved | – | – | – | – | – | – | – | – | |
| (0x73) | Reserved | – | – | – | – | – | – | – | – | |
| (0x72) | Reserved | – | – | – | – | – | – | – | – | |
| (0x71) | Reserved | – | – | – | – | – | – | – | – | |
| (0x70) | Reserved | – | – | – | – | – | – | – | – | |
| (0x6F) | TIMSK1 | – | – | ICIE1 | – | – | OCIE1B | OCIE1A | TOIE1 | 114 |
| (0x6E) | TIMSK0 | – | – | – | – | – | OCIE0B | OCIE0A | TOIE0 | 87 |
| (0x6D) | PCMSK2 | PCINT23 | PCINT22 | PCINT21 | PCINT20 | PCINT19 | PCINT18 | PCINT17 | PCINT16 | 59 |
| (0x6C) | PCMSK1 | PCINT15 | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9 | PCINT8 | 59 |
| (0x6B) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | 59 |
| (0x6A) | PCMSK3 | – | – | - | - | PCINT27 | PCINT26 | PCINT25 | PCINT24 | 59 |
| (0x69) | EICRA | – | – | – | – | ISC11 | ISC10 | ISC01 | ISC00 | 55 |
| (0x68) | PCICR | – | – | – | – | PCIE3 | PCIE2 | PCIE1 | PCIE0 | 57 |
| (0x67) | Reserved | – | – | – | – | – | – | – | – | |
| (0x66) | OSCCAL | Oscillator Calibration Register | | | | | | | | 34 |
| (0x65) | Reserved | – | – | – | – | – | – | – | – | |
| (0x64) | PRR | PRTWI | – | PRTIM0 | – | PRTIM1 | PRSPI | – | PRADC | 40 |
| (0x63) | Reserved | – | – | – | – | – | – | – | – | |
| (0x62) | Reserved | – | – | – | – | – | – | – | – | |
| (0x61) | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | 34 |
| (0x60) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | 49 |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 9 |
| 0x3E (0x5E) | SPH | – | – | – | – | – | – | SP9 | SP8 | 11 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 11 |
| 0x3C (0x5C) | Reserved | – | – | – | – | – | – | – | – | |
| 0x3B (0x5B) | Reserved | – | – | – | – | – | – | – | – | |
| 0x3A (0x5A) | Reserved | – | – | – | – | – | – | – | – | |
| 0x39 (0x59) | Reserved | – | – | – | – | – | – | – | – | |
| 0x38 (0x58) | Reserved | – | – | – | – | – | – | – | – | |
| 0x37 (0x57) | SPMCSR | – | RWWSB | – | CTPB | RFLB | PGWRT | PGERS | SELFPRGEN | 186 |
| 0x36 (0x56) | Reserved | – | | | | – | – | – | – | |
| 0x35 (0x55) | MCUCR | – | BODS | BODSE | PUD | – | – | – | – | 40, 77 |
| 0x34 (0x54) | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | 49 |
| 0x33 (0x53) | SMCR | – | – | – | – | – | SM1 | SM0 | SE | 39 |
| 0x32 (0x52) | Reserved | – | – | – | – | – | – | – | – | |
| 0x31 (0x51) | DWDR | debugWire Data Register | | | | | | | | 182 |
| 0x30 (0x50) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 162 |
| 0x2F (0x4F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2E (0x4E) | SPDR | SPI Data Register | | | | | | | | 128 |
| 0x2D (0x4D) | SPSR | SPIF | WCOL | – | – | – | – | – | SPI2X | 127 |
| 0x2C (0x4C) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 126 |
| 0x2B (0x4B) | GPIOR2 | General Purpose I/O Register 2 | | | | | | | | 27 |
| 0x2A (0x4A) | GPIOR1 | General Purpose I/O Register 1 | | | | | | | | 27 |
| 0x29 (0x49) | Reserved | – | – | – | – | – | – | – | – | |
| 0x28 (0x48) | OCR0B | Timer/Counter0 Output Compare Register B | | | | | | | | 87 |
| 0x27 (0x47) | OCR0A | Timer/Counter0 Output Compare Register A | | | | | | | | 86 |
| 0x26 (0x46) | TCNT0 | Timer/Counter0 (8-bit) | | | | | | | | 86 |
| 0x25 (0x45) | TCCR0A | – | – | – | – | CTC0 | CS02 | CS01 | CS00 | 85 |
| 0x24 (0x44) | Reserved | – | – | – | – | – | – | – | – | |
| 0x23 (0x43) | GTCCR | TSM | – | – | – | – | – | – | PSRSYNC | 118 |
| 0x22 (0x42) | Reserved | – | – | – | – | – | – | – | – | |
| 0x21 (0x41) | EEARL | EEPROM Address Register Low Byte | | | | | | | | 25 |
| 0x20 (0x40) | EEDR | EEPROM Data Register | | | | | | | | 25 |
| 0x1F (0x3F) | EECR | – | – | EEPM1 | EEPM0 | EERIE | EEMPE | EEPE | EERE | 25 |
| 0x1E (0x3E) | GPIOR0 | General Purpose I/O Register 0 | | | | | | | | 27 |
| 0x1D (0x3D) | EIMSK | – | – | – | – | – | – | INT1 | INT0 | 56 |
| 0x1C (0x3C) | EIFR | – | – | – | – | – | – | INTF1 | INTF0 | 56 |
| 0x1B (0x3B) | PCIFR | – | – | – | – | PCIF3 | PCIF2 | PCIF1 | PCIF0 | 58 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1A (0x3A) | Reserved | – | – | – | – | – | – | – | – | |
| 0x19 (0x39) | Reserved | – | – | – | – | – | – | – | – | |
| 0x18 (0x38) | Reserved | – | – | – | – | – | – | – | – | |
| 0x17 (0x37) | Reserved | – | – | – | – | – | – | – | – | |
| 0x16 (0x36) | TIFR1 | – | – | ICF1 | – | – | OCF1B | OCF1A | TOV1 | 115 |
| 0x15 (0x35) | TIFR0 | – | – | – | – | – | OCF0B | OCF0A | TOV0 | 87 |
| 0x14 (0x34) | Reserved | – | – | – | – | – | – | – | – | |
| 0x13 (0x33) | Reserved | – | – | – | – | – | – | – | – | |
| 0x12 (0x32) | PORTCR | BBMD | BBMC | BBMB | BBMA | PUDD | PUDC | PUDB | PUDA | 77 |
| 0x11 (0x31) | Reserved | – | – | – | – | – | – | – | – | |
| 0x10 (0x30) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0F (0x2F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0E (0x2E) | PORTA | – | – | – | – | PORTA3 | PORTA2 | PORTA1 | PORTA0 | 78 |
| 0x0D (0x2D) | DDRA | – | – | – | – | DDA3 | DDA2 | DDA1 | DDA0 | 78 |
| 0x0C (0x2C) | PINA | – | – | – | – | PINA3 | PINA2 | PINA1 | PINA0 | 78 |
| 0x0B (0x2B) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | 79 |
| 0x0A (0x2A) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | 79 |
| 0x09 (0x29) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | 79 |
| 0x08 (0x28) | PORTC | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | 78 |
| 0x07 (0x27) | DDRC | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | 78 |
| 0x06 (0x26) | PINC | PINC7 | PINC6 | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | 79 |
| 0x05 (0x25) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 78 |
| 0x04 (0x24) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 78 |
| 0x03 (0x23) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 78 |
| 0x02 (0x22) | Reserved | – | – | – | – | – | – | – | – | |
| 0x01 (0x21) | Reserved | – | – | – | – | – | – | – | – | |
| 0x00 (0x20) | Reserved | – | – | – | – | – | – | – | – | |

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 – 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 – 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATtiny48/88 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 – 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

# 5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **ARITHMETIC AND LOGIC INSTRUCTIONS** | | | | | |
| ADD | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One's Complement | Rd ← 0xFF – Rd | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | Rd ← 0x00 – Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |
| **BRANCH INSTRUCTIONS** | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |
| **BIT AND BIT-TEST INSTRUCTIONS** | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |

# 6. Ordering Information

## 6.1 ATtiny48

| Speed (MHz) | Power Supply | Ordering Code[1] | Package[2] | Operational Range |
|---|---|---|---|---|
| 12 | 1.8 – 5.5V | ATtiny48-MMU<br>ATtiny48-MMUR<br>ATtiny48-MMH<br>ATtiny48-MMHR<br>ATtiny48-PU<br>ATtiny48-AU<br>ATtiny48-AUR<br>ATtiny48-CCU<br>ATtiny48-CCUR<br>ATtiny48-MU<br>ATtiny48-MUR | 28M1<br>28M1<br>28M1<br>28M1<br>28P3<br>32A<br>32A<br>32CC1<br>32CC1<br>32M1-A<br>32M1-A | Industrial<br>(-40°C to +85°C)[3] |

Notes: 1. Code indicators:

- H: NiPdAu lead finish
- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

| Package Type | |
|---|---|
| **28M1** | 28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm, Quad Flat No-Lead (QFN) |
| **28P3** | 28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP) |
| **32A** | 32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP) |
| **32CC1** | 32-ball (6 x 6 Array), 0.50 mm Pitch, 4 x 4 x 0.6 mm, Ultra Thin, Fine-Pitch Ball Grid Array Package (UFBGA) |
| **32M1-A** | 32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm, Quad Flat No-Lead (QFN) |

## 6.2 ATtiny88

| Speed (MHz) | Power Supply | Ordering Code[1] | Package[2] | Operational Range |
|---|---|---|---|---|
| 12 | 1.8 – 5.5V | ATtiny88-MMU<br>ATtiny88-MMUR<br>ATtiny88-MMH<br>ATtiny88-MMHR<br>ATtiny88-PU<br>ATtiny88-AU<br>ATtiny88-AUR<br>ATtiny88-CCU<br>ATtiny88-CCUR<br>ATtiny88-MU<br>ATtiny88-MUR | 28M1<br>28M1<br>28M1<br>28M1<br>28P3<br>32A<br>32A<br>32CC1<br>32CC1<br>32M1-A<br>32M1-A | Industrial<br>(-40°C to +85°C)[3] |

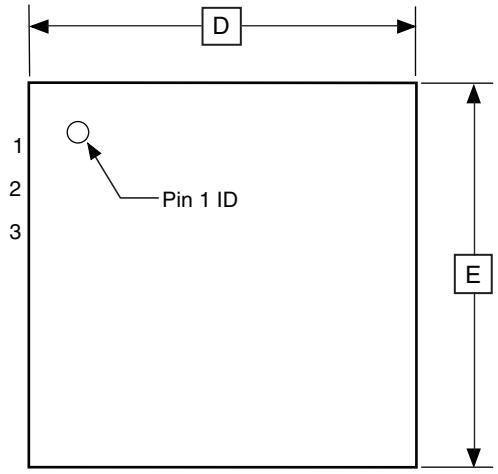
Notes: 1. Code indicators:
- H: NiPdAu lead finish
- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

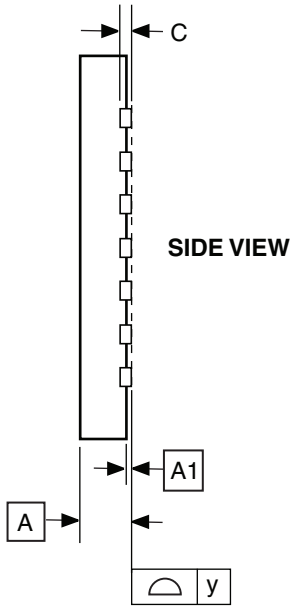
| Package Type | |
|---|---|
| **28M1** | 28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm, Quad Flat No-Lead (QFN) |
| **28P3** | 28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP) |
| **32A** | 32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP) |
| **32CC1** | 32-ball (6 x 6 Array), 0.50 mm Pitch, 4 x 4 x 0.6 mm, Ultra Thin, Fine-Pitch Ball Grid Array Package (UFBGA) |
| **32M1-A** | 32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm, Quad Flat No-Lead (QFN) |

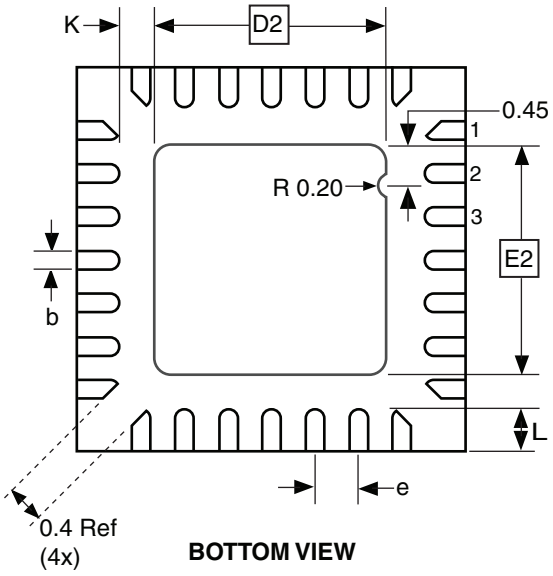
# 7. Packaging Information

## 7.1 28M1




TOP VIEW




BOTTOM VIEW

Note: The terminal #1 ID is a Laser-marked Feature.

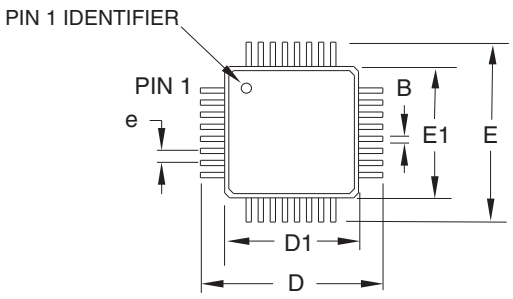
**COMMON DIMENSIONS**
(Unit of Measure = mm)

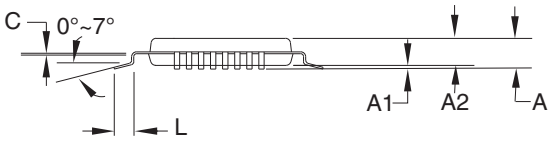
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.17 | 0.22 | 0.27 | |
| C | | 0.20 REF | | |
| D | 3.95 | 4.00 | 4.05 | |
| D2 | 2.35 | 2.40 | 2.45 | |
| E | 3.95 | 4.00 | 4.05 | |
| E2 | 2.35 | 2.40 | 2.45 | |
| e | | 0.45 | | |
| L | 0.35 | 0.40 | 0.45 | |
| y | 0.00 | – | 0.08 | |
| K | 0.20 | – | – | |

10/24/08

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:** packagedrawings@atmel.com | **28M1,** 28-pad, 4 x 4 x 1.0 mm Body, Lead Pitch 0.45 mm, 2.4 x 2.4 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN) | ZBV | 28M1 | B |

## 7.3 32A




**COMMON DIMENSIONS**
(Unit of Measure = mm)

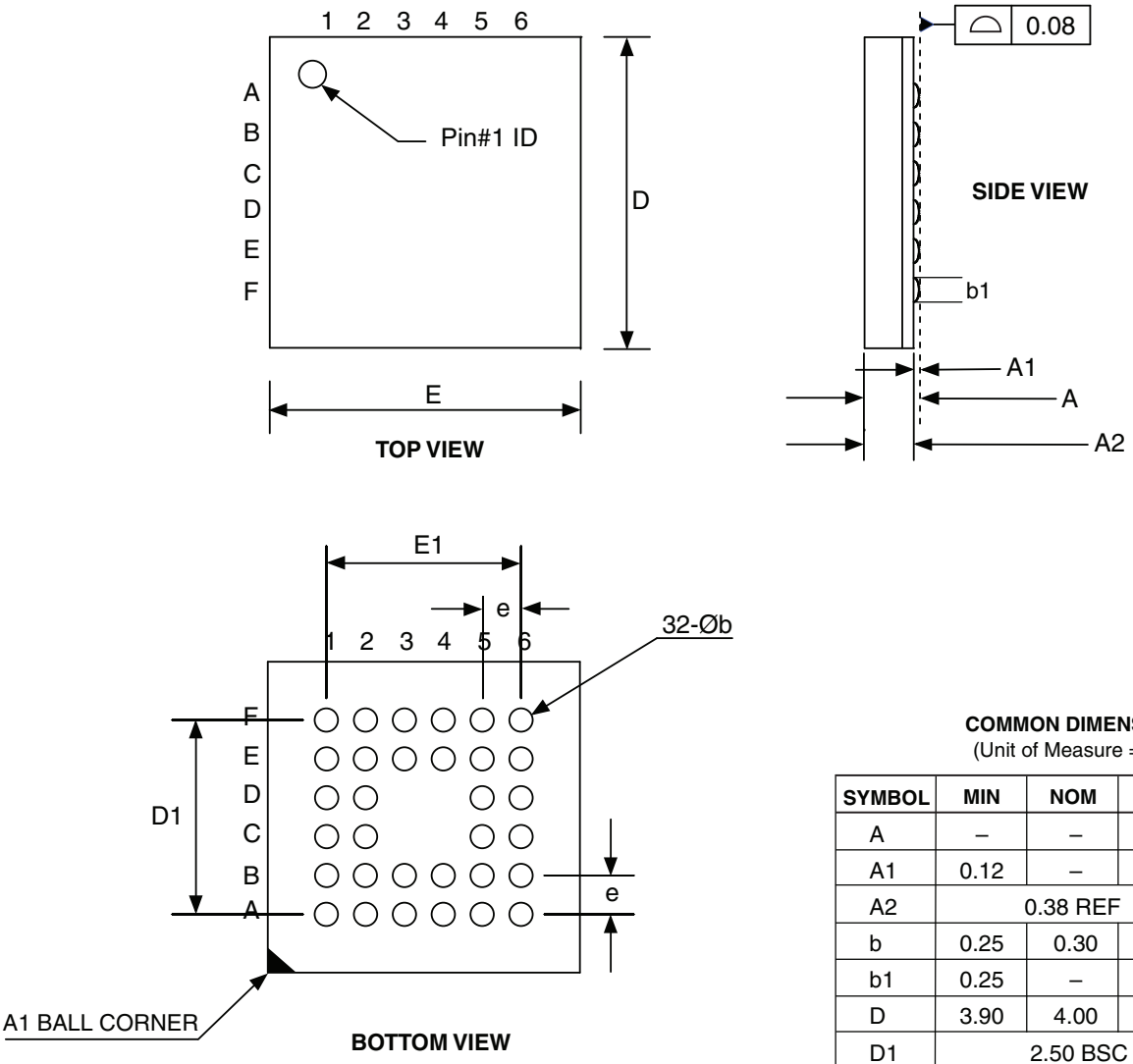
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 8.75 | 9.00 | 9.25 | |
| D1 | 6.90 | 7.00 | 7.10 | Note 2 |
| E | 8.75 | 9.00 | 9.25 | |
| E1 | 6.90 | 7.00 | 7.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

2010-10-20

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness,<br>0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 32A | C |

## 7.4 32CC1




**COMMON DIMENSIONS**
(Unit of Measure = mm)

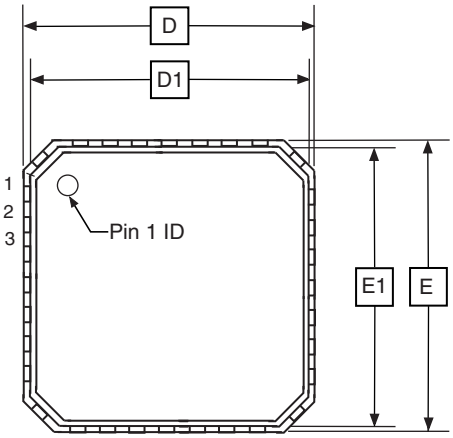
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 0.60 | |
| A1 | 0.12 | – | – | |
| A2 | | 0.38 REF | | |
| b | 0.25 | 0.30 | 0.35 | 1 |
| b1 | 0.25 | – | – | 2 |
| D | 3.90 | 4.00 | 4.10 | |
| D1 | | 2.50 BSC | | |
| E | 3.90 | 4.00 | 4.10 | |
| E1 | | 2.50 BSC | | |
| e | | 0.50 BSC | | |

Note1: Dimension "b" is measured at the maximum ball dia. in a plane parallel to the seating plane.
Note2: Dimension "b1" is the solderable surface defined by the opening of the solder resist layer.

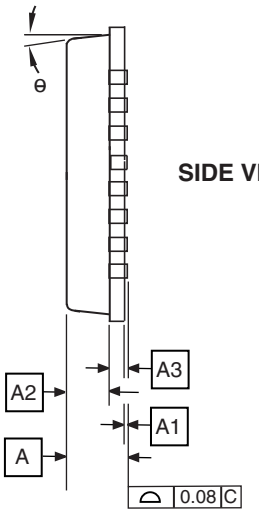
07/06/10

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:** packagedrawings@atmel.com | **32CC1**, 32-ball (6 x 6 Array), 4 x 4 x 0.6 mm package, ball pitch 0.50 mm, Ultra Thin, Fine-Pitch Ball Grid Array (UFBGA) | CAG | 32CC1 | B |

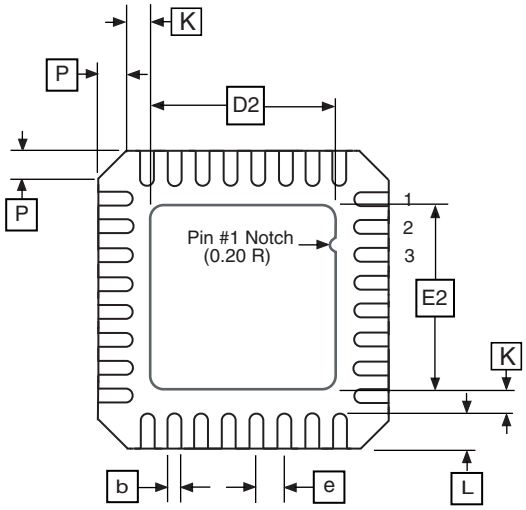
## 7.5 32M1-A




TOP VIEW




SIDE VIEW




BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| A2 | – | 0.65 | 1.00 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 4.90 | 5.00 | 5.10 | |
| D1 | 4.70 | 4.75 | 4.80 | |
| D2 | 2.95 | 3.10 | 3.25 | |
| E | 4.90 | 5.00 | 5.10 | |
| E1 | 4.70 | 4.75 | 4.80 | |
| E2 | 2.95 | 3.10 | 3.25 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 | |
| P | – | – | 0.60 | |
| θ | – | – | $12^{o}$ | |
| K | 0.20 | – | – | |

5/25/06

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,<br>3.10 mm Exposed Pad, Micro Lead Frame Package (MLF) | 32M1-A | E |

# 8. Errata

## 8.1 ATtiny48

### 8.1.1 Rev. C

No known errata.

### 8.1.2 Rev. B

Not sampled.

### 8.1.3 Rev. A

Not sampled.

## 8.2 ATtiny88

### 8.2.1 Rev. C

No known errata.

### 8.2.2 Rev. B

No known errata.

### 8.2.3 Rev. A

Not sampled.

# 9. Datasheet Revision History

## 9.1 Rev. 8008H - 04/11

1. Updated:
   – “Ordering Information” on page 283, added tape & reel code -MMUR

## 9.2 Rev. 8008G - 04/11

1. Updated:
   – “Block Diagram” on page 5
   – “Memories” on page 17
   – “Clock System” on page 28
   – “Lock Bits, Fuse Bits and Device Signature” on page 188
   – “External Programming” on page 191
   – “Speed” on page 208
   – “Two-Wire Serial Interface Characteristics” on page 212
2. Added:
   – “Capacitive Touch Sensing” on page 7
   – “Register Description” on page 15
   – “Overview” on page 129
   – “Compatibility with SMBus” on page 156
3. Changed document status from “Preliminary” to “Final”.

## 9.3 Rev. 8008F - 06/10

1. Updated notes 1 and 10 in table in Section 22.2 “DC Characteristics” on page 206.
2. Updated package drawing in Section 27.4 “32CC1” on page 288.
3. Updated bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0].

## 9.4 Rev. 8008E - 05/10

1. Section 24. “Register Summary” on page 277, added SPH at address 0x3E.
2. Section 27.1 “28M1” on page 285 updated with correct package drawing.

## 9.5 Rev. 8008D - 03/10

1. Separated Typical Characteristic plots, added Section 23.2 “ATtiny88” on page 248.
2. Updated:
   – Section 1.1 “Pin Descriptions” on page 3, Port D, adjusted texts ‘sink and source’ and ‘high sink’.
   – Table 6-3 on page 28 adjusted, to fix TBD.
   – Section 6.2.3 “Internal 128 kHz Oscillator” on page 31 adjusted, to fix TBD.
   – Section 8.4 “Watchdog Timer” on page 46, updated.
   – Section 22.2 “DC Characteristics” on page 206, updated TBD in notes 5 and 8.
3. Added:

- UFBGA package (32CC1) in, “Features” on page 1, “Pin Configurations” on page 2, Section 26. “Ordering Information” on page 283, and Section 27. “Packaging Information” on page 285
- Addresses in all Register Desc. tables, with cross-references to Register Summary
- Tape and reel in Section 26. “Ordering Information” on page 283

## 9.6 Rev. 8008C - 03/09

1. Updated sections:
   - “Features” on page 1
   - “Reset and Interrupt Handling” on page 12
   - “EECR – EEPROM Control Register” on page 25
   - “Features” on page 129
   - “Bit Rate Generator Unit” on page 135
   - “TWBR – TWI Bit Rate Register” on page 156
   - “TWHSR – TWI High Speed Register” on page 160
   - “Analog Comparator” on page 161
   - “Overview” on page 164
   - “Operation” on page 165
   - “Starting a Conversion” on page 166
   - “Programming the Lock Bits” on page 199
   - “Absolute Maximum Ratings*” on page 206
   - “DC Characteristics” on page 206
   - “Speed” on page 208
   - “Register Summary” on page 277
2. Added sections
   - “High-Speed Two-Wire Interface Clock – $clk_{TWIHS}$” on page 29
   - “Analog Comparator Characteristics” on page 210
3. Updated Figure 6-1 on page 28.
4. Updated order codes on page 283 and page 284 to reflect changes in leadframe composition.

## 9.7 Rev. 8008B - 06/08

1. Updated introduction of “I/O-Ports” on page 60.
2. Updated “DC Characteristics” on page 206.
3. Added “Typical Characteristics” on page 219.

## 9.8 Rev. 8008A - 06/08

1. Initial revision.

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