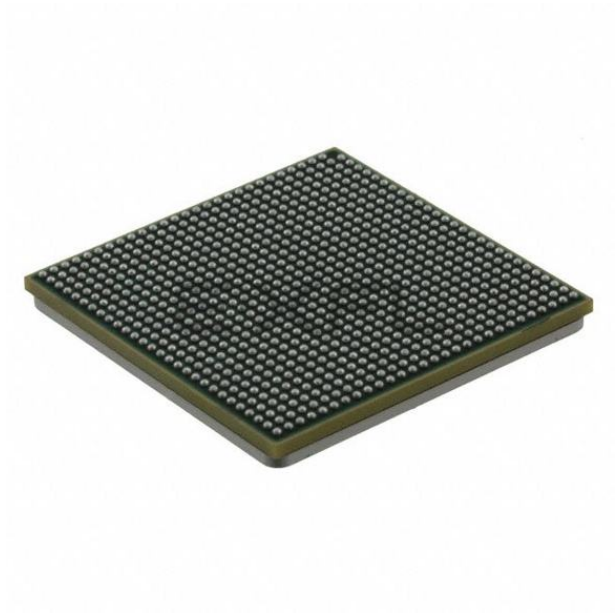

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8555evtalf

1 Overview

The following section provides a high-level overview of the MPC8555E features. Figure 1 shows the major functional units within the MPC8555E.

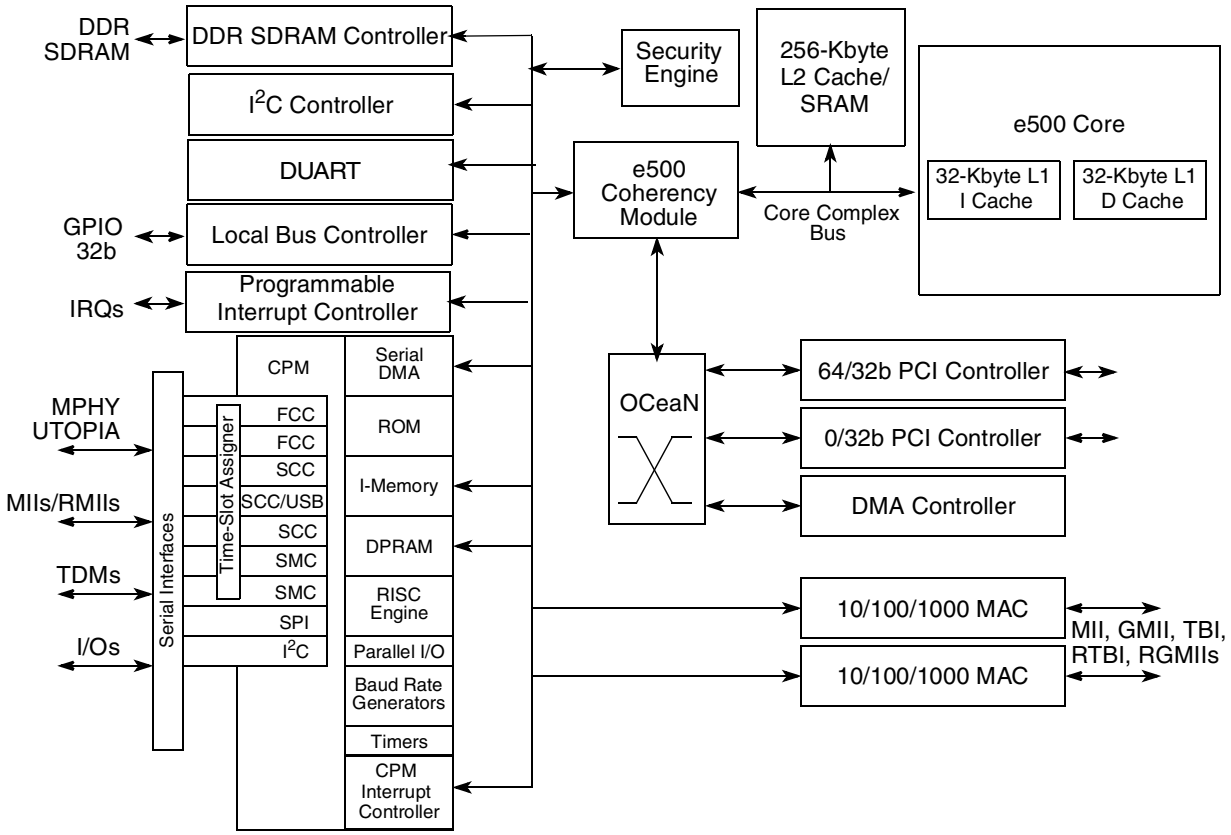


Figure 1. MPC8555E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8555E feature set.

- Embedded e500 Book E-compatible core
  - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
  - Dual-issue superscalar, 7-stage pipeline design
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
  - Lockable L1 caches—entire cache or on a per-line basis
  - Separate locking for instructions and data
  - Single-precision floating-point operations
  - Memory management unit especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Dynamic power management
  - Performance monitor facility

  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency
  - Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power save modes: doze, nap, and sleep
  - Employs dynamic power management
  - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8555E. The MPC8555E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8555E.

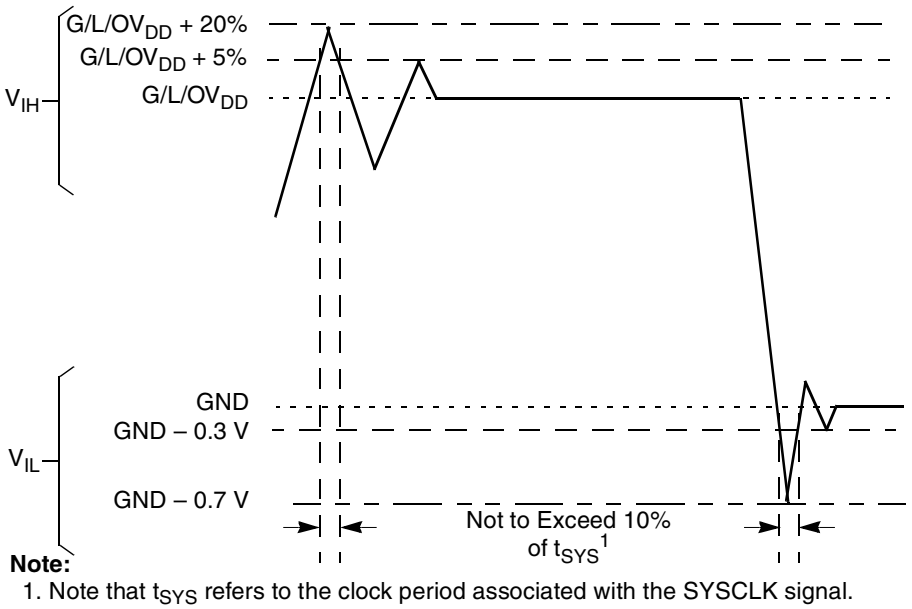


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8555E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8555E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8555E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	–10	10	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	5	µA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{MCS}$(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCX}	 2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHMH}	 –0.9 –1.1 –1.2	 0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.9$	$-0.5 \times t_{MCK} + 0.3$	ns	7
MDQS epilogue end	t_{DDKLME}	–0.9	0.3	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{MCK}$ can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns. t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this typically is set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8555E.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8555E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

Table 20. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise and fall times	t_{GTXR}[3], t_{GTXR}[2,4]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

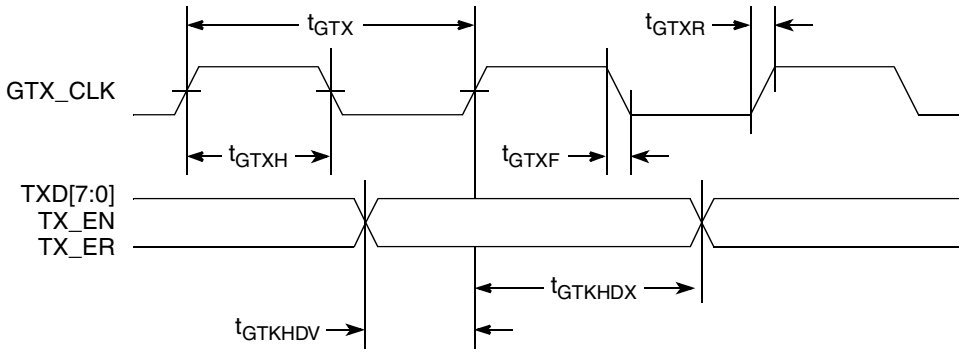


Figure 7. GMII Transmit AC Timing Diagram

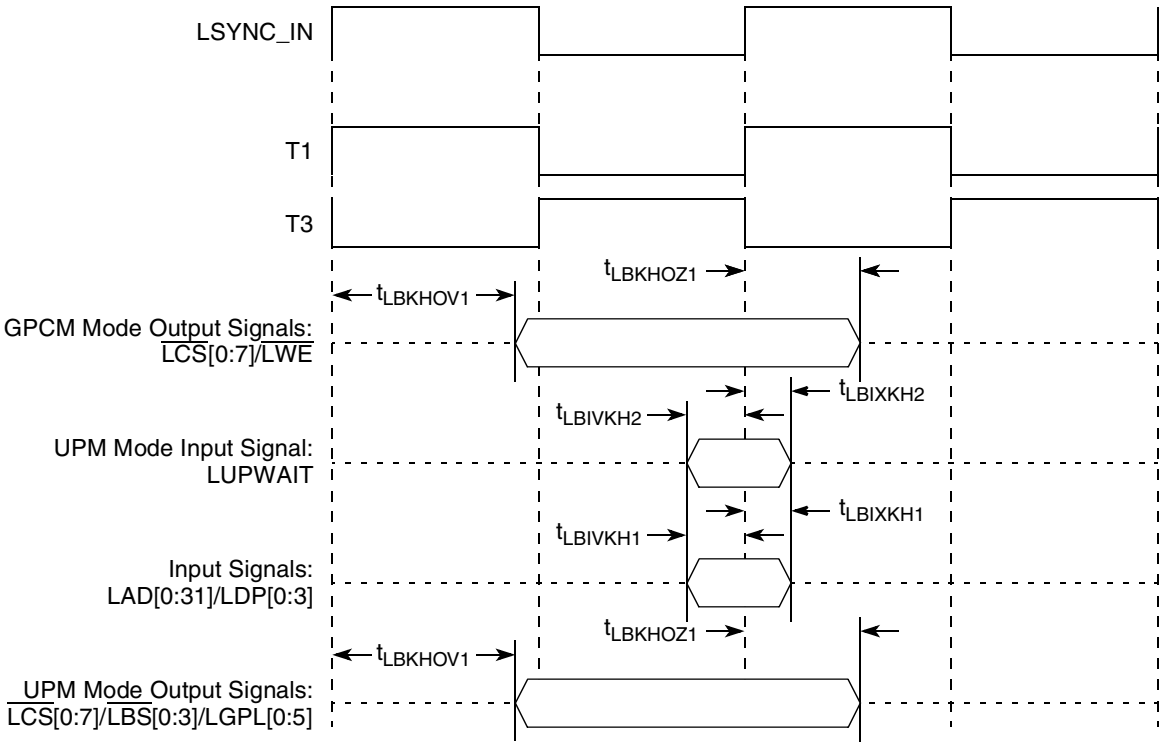


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8555E.

10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

Table 32. CPM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	3.465	V	1
Input low voltage	V_{IL}		GND	0.8	V	1, 2
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	1
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1

Note:
1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. V_{IL}(max) for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

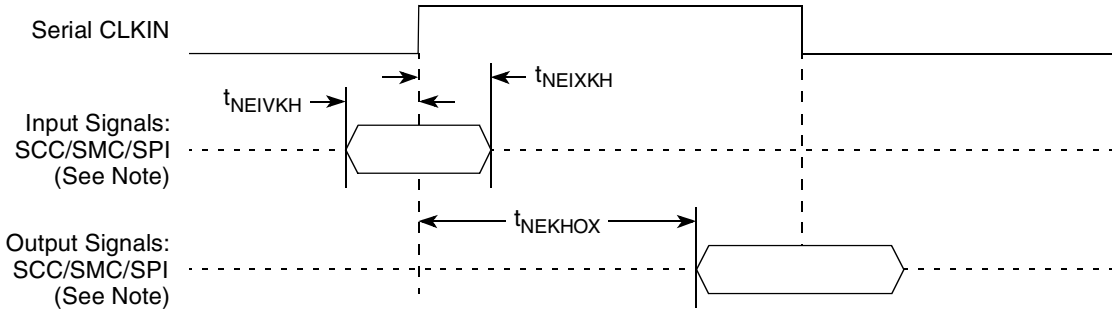
NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 33. CPM Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min[3]	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	6	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	t_{FEIXKH}b	2	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	6	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SMC/SPI inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SMC/SPI inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	4	ns

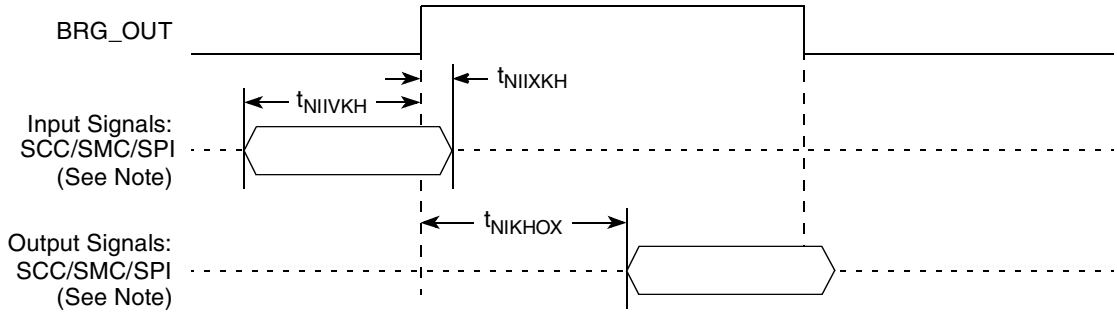
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

[1] SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

[2] SPI AC timings refer always to SPICLK.

11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8555E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 — —	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 16 provides the AC test load for the I^2C.

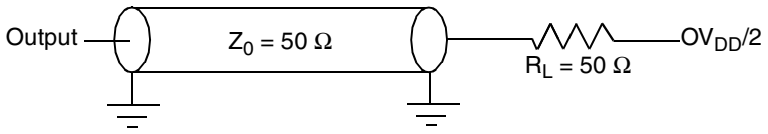


Figure 37. I^2C AC Test Load

Figure 38 shows the AC timing diagram for the I^2C bus.

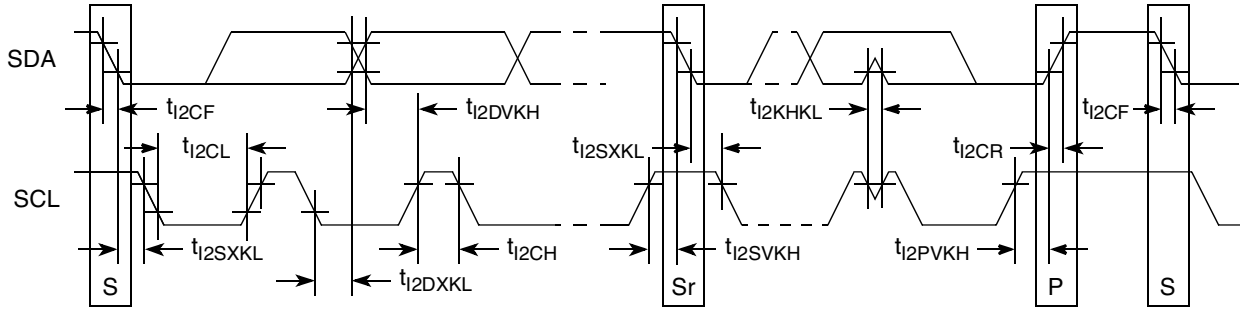


Figure 38. I^2C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8555E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8555E.

Table 41. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$	—	±5	µA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:
1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, “Clocking.”
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.
9. Guaranteed by characterization.
10. Guaranteed by design.

Figure 16 provides the AC test load for PCI.

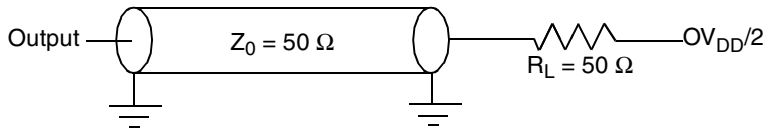


Figure 39. PCI AC Test Load

Figure 40 shows the PCI input AC timing conditions.

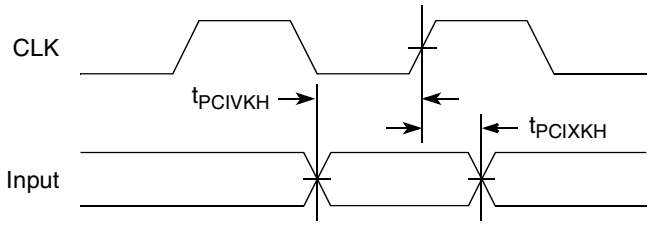


Figure 40. PCI Input AC Timing Measurement Conditions

Figure 41 shows the PCI output AC timing conditions.

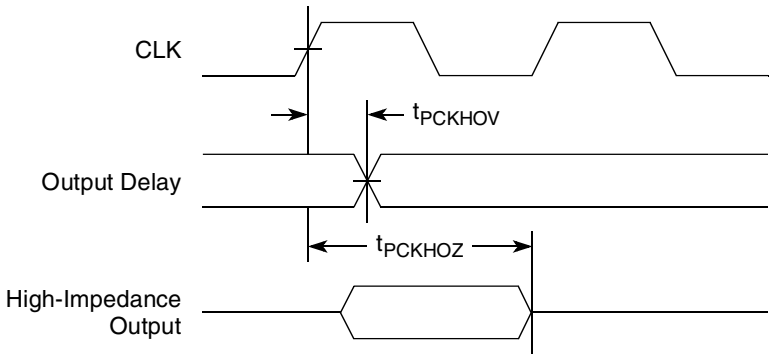


Figure 41. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8555E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	5, 7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	5, 8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	—
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	P27	O	OV_{DD}	1
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	—
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	U22	O	OV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	V28	O	OV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	V27	O	OV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	21
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	—
LSYNC_OUT	T28	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:1]/LSDDQM[0:1]/ $\overline{\text{LBS}}$[0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
$\overline{\text{LWE}}$[2:3]/LSDDQM[2:3]/ $\overline{\text{LBS}}$[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
$\overline{\text{DMA\_DREQ}}$[0:1]	H5, G4	I	OV_{DD}	—
$\overline{\text{DMA\_DACK}}$[0:1]	H6, G5	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0:1]	H7, G6	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP}}$	AG17	I	OV_{DD}	—
$\overline{\text{UDE}}$	AG16	I	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_CRS	D9	I	LV_{DD}	—
TSEC2_COL	F8	I	LV_{DD}	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	—
TSEC2_RX_DV	H8	I	LV_{DD}	—
TSEC2_RX_ER	A8	I	LV_{DD}	—
TSEC2_RX_CLK	E10	I	LV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0,1]	Y2, Y3	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0,1]	Y1, AD1	O	OV_{DD}	—
UART_SIN[0,1]	P11, AD5	I	OV_{DD}	—
UART_SOUT[0,1]	N6, AD2	O	OV_{DD}	—
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 19
IIC_SCL	AH23	I/O	OV_{DD}	4, 19
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	18
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	—
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 18
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:3]	F3, F5	O	OV_{DD}	6
MSRCID4	F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	—
RTC	AB23	I	OV_{DD}	—
CLK_OUT	AF22	O	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV_{DD}	—
TDI	AG21	I	OV_{DD}	12
TDO	AF19	O	OV_{DD}	11
TMS	AF23	I	OV_{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV_{DD}	12
DFT				
$\overline{\text{LSSD\_MODE}}$	AG19	I	OV_{DD}	20
L1_TSTCLK	AB22	I	OV_{DD}	20
L2_TSTCLK	AG22	I	OV_{DD}	20
$\overline{\text{TEST\_SEL0}}$	AH20	I	OV_{DD}	3
TEST_SEL1	AG26	I	OV_{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
$AV_{DD}1$	AH19	Power for e500 PLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	AH18	Power for CCB PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}3$	AH17	Power for CPM PLL (1.2 V)	$AV_{DD}3$	—
$AV_{DD}4$	AF28	Power for PCI1 PLL (1.2 V)	$AV_{DD}4$	—
$AV_{DD}5$	AE28	Power for PCI2 PLL (1.2 V)	$AV_{DD}5$	—

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Table 47. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8555E to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8555E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid ($11 \times 11 \times 1$ mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance ($8.7 \times 9.3 \times 0.05$ mm)		
k_z	1.07	
Die ($8.7 \times 9.3 \times 0.75$ mm)		
Bump/Underfill—Collapsed resistance ($8.7 \times 9.3 \times 0.07$ mm)		
k_z	4.4	
Substrate and Solder Balls ($25 \times 25 \times 1.6$ mm)		
k_x	14.2	
k_y	14.2	
k_z	1.2	

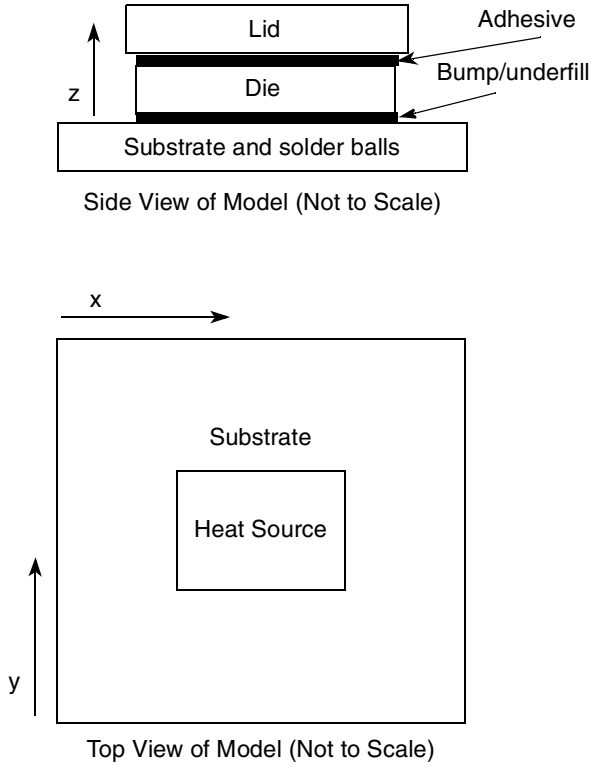


Figure 44. MPC8555E Thermal Model

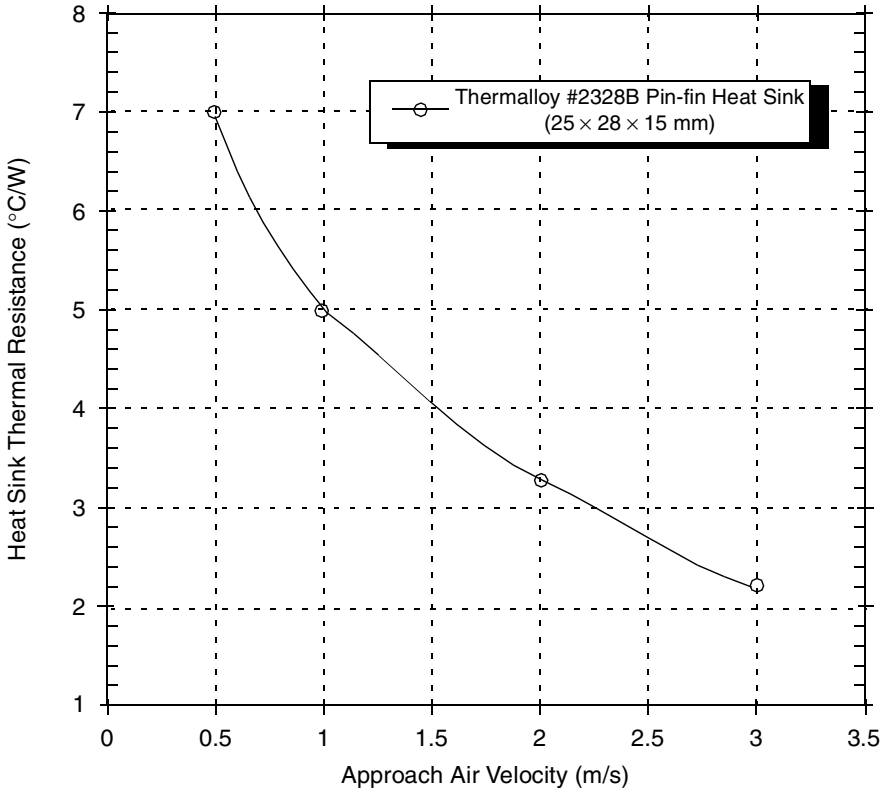


Figure 47. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in Table 49 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 48 and Figure 49. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	7/2007	Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Added footnote 2 about junction temperature in Table 4. Added max. power values for 1000 MHz core frequency in Table 4. Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30. Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values inTable 30. Added note 3 to $t_{LBKHOV1}$ in Table 30. Modified note 3 in Table 30 and Table 31. Added note 3 to $t_{LBKLOV1}$ in Table 31. Modified values for t_{LBKHKT}, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31. Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21. Modified note for signal CLK_OUT in Table 43. PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43. Added column for Encryption Acceleration in Table 52.
3	8/2005	Modified max. power values in Table 4. Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43.
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31. Added note 2 in Table 7. Modified min and max values for t_{DDKHMP} in Table 14.
1	6/2005	Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface in Table 27. Modified footnote 4 and changed typical power for the 1000 MHz core frequency inTable 4. Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31.
0	6/2005	Initial release.