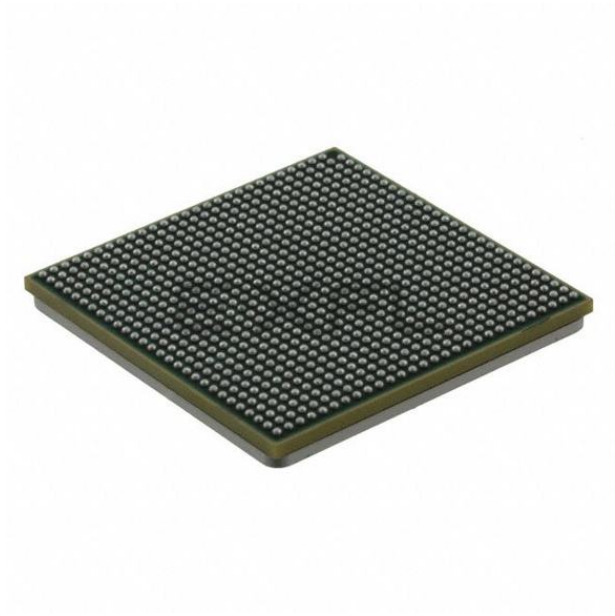

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8555evtaqf

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
  - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses

- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI
    - Four inbound windows
    - Four outbound windows plus default translation for PCI
- DDR memory controller
  - Programmable timing supporting first generation DDR SDRAM
  - 64-bit data interface, up to MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self refresh DDR SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8555E.

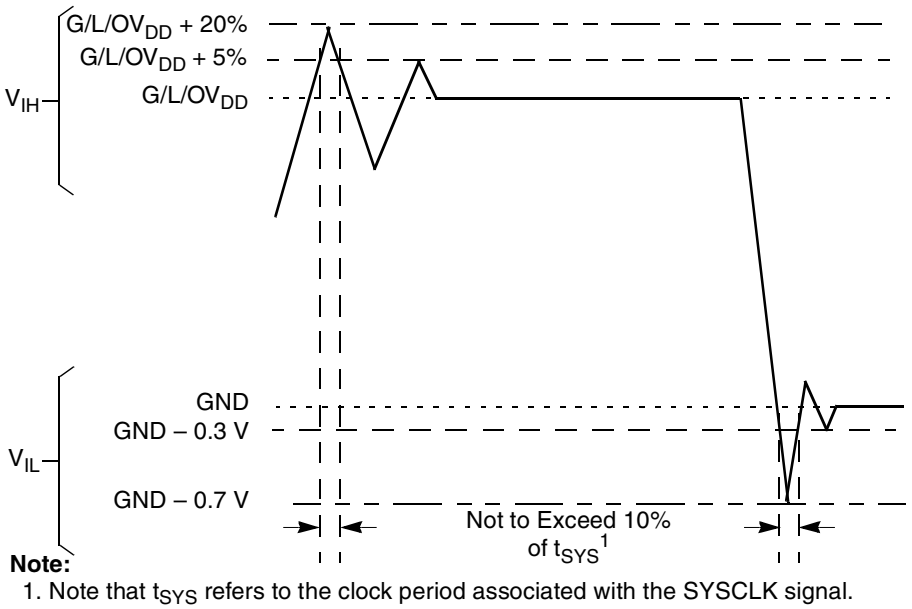


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8555E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8555E for the 3.3-V signals, respectively.

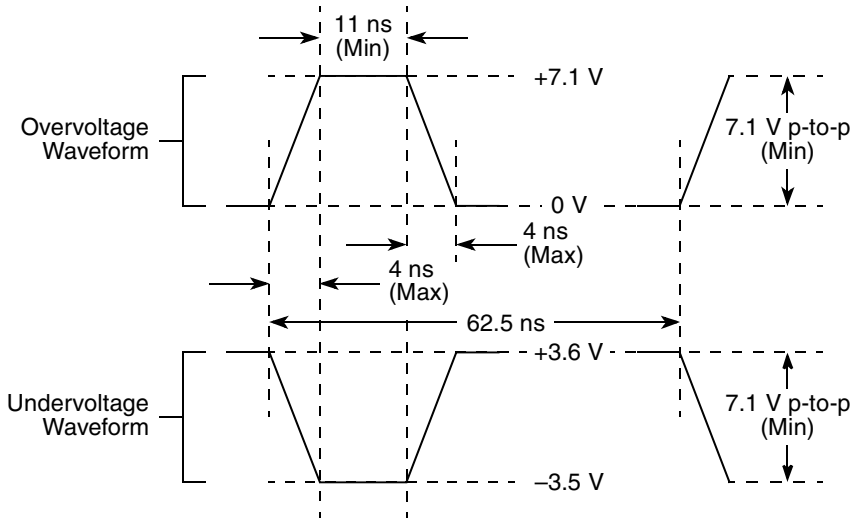


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	OV_{DD} = 3.3 V	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	
TSEC/10/100 signals	42	LV_{DD} = 2.5/3.3 V	
DUART, system control, I2C, JTAG	42	OV_{DD} = 3.3 V	

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

3 Power Characteristics

The estimated typical power dissipation for this family of PowerQUICC III devices is shown in Table 4.

Table 4. Power Dissipation(1) (2)

CCB Frequency (MHz)	Core Frequency (MHz)	V_{DD}	Typical Power(3)(4) (W)	Maximum Power(5) (W)
200	400	1.2	4.9	6.6
	500	1.2	5.2	7.0
	600	1.2	5.5	7.3
267	533	1.2	5.4	7.2
	667	1.2	5.9	7.7
	800	1.2	6.3	9.1
333	667	1.2	6.0	7.9
	833	1.2	6.5	9.3
	1000(6)	1.3	9.6	12.8

Notes:

1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 degrees junction temperature is not exceeded on this device.
3. Typical power is based on a nominal voltage of V_{DD} = 1.2V, a nominal process, a junction temperature of T_j = 105° C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions likely need to design to a value higher than Typical Power based on the end application, T_A target, and I/O power
5. Maximum power is based on a nominal voltage of V_{DD} = 1.2V, worst case process, a junction temperature of T_j = 105° C, and an artificial smoke test.
6. The nominal recommended V_{DD} = 1.3V for this speed grade.

Notes:

1.

2.

3.

4.

5.

6.

Table 5. Typical I/O Power Dissipation

Interface	Parameters	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	—
	CCB = 266 MHz	0.59	—	—	—	W	—
	CCB = 300 MHz	0.66	—	—	—	W	—
	CCB = 333 MHz	0.73	—	—	—	W	—
PCI I/O	64b, 66 MHz	—	0.14	—	—	W	—
	64b, 33 MHz	—	0.08	—	—	W	—
	32b, 66 MHz	—	0.07	—	—	W	Multiply by 2 if using two 32b ports
	32b, 33 MHz	—	0.04	—	—	W	
Local Bus I/O	32b, 167 MHz	—	0.30	—	—	W	—
	32b, 133 MHz	—	0.24	—	—	W	—
	32b, 83 MHz	—	0.16	—	—	W	—
	32b, 66 MHz	—	0.13	—	—	W	—
	32b, 33 MHz	—	0.07	—	—	W	—
TSEC I/O	MII	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	0.07	—	W	
	RGMII or RTBI	—	—	—	0.04	W	
CPM - FCC	MII	—	0.015	—	—	W	—
	RMII	—	0.013	—	—	W	—
	HDLC 16 Mbps	—	0.009	—	—	W	—
	UTOPIA-8 SPHY	—	0.06	—	—	W	—
	UTOPIA-8 MPHY	—	0.1	—	—	W	—
	UTOPIA-16 SPHY	—	0.094	—	—	W	—
	UTOPIA-16 MPHY	—	0.135	—	—	W	—
CPM - SCC	HDLC 16 Mbps	—	0.004	—	—	W	—
TDMA or TDMB	Nibble Mode	—	0.01	—	—	W	—
TDMA or TDMB	Per Channel	—	0.005	—	—	W	Up to 4 TDM channels, multiply by number of TDM channels.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR ≤ 266 MHz	t_{DISKEW}	—	 750 1125	ps	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	 –1000 –1100 –1200	 200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	 2.8 3.45 4.6	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	 2.0 2.65 3.8	—	ns	4
$\overline{\text{MCS}}$(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	 2.8 3.45 4.6	—	ns	4

Figure 6 provides the AC test load for the DDR bus.

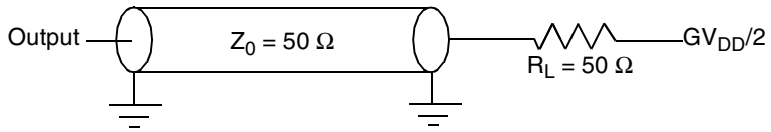


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8555E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8555E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF} [2,3]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

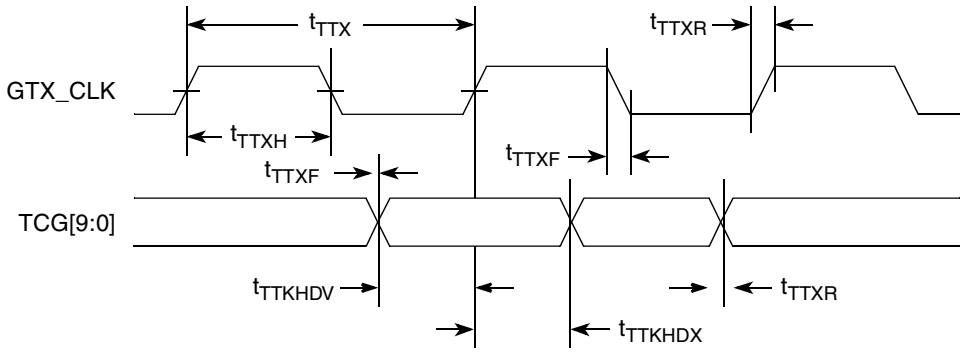


Figure 12. TBI Transmit AC Timing Diagram

Table 27. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input high current	I_{IH}	LV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}			$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
3. This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
4. Guaranteed by design.

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL enabled.

Table 30. Local Bus General Timing Parameters—DLL Enabled

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	3, 4, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	3, 4, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOV1}$	—	2.3	ns	3, 8
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			3.8		
Local bus clock to data valid for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOV2}$	—	2.5	ns	3, 8
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			4.0		
Local bus clock to address valid for LAD	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOV3}$	—	2.6	ns	3, 8
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			4.1		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOX1}$	0.7	—	ns	3, 8
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		1.6			
Output hold from local bus clock for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOX2}$	0.7	—	ns	3, 8
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOZ1}$	—	2.8	ns	5, 9
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			4.2		

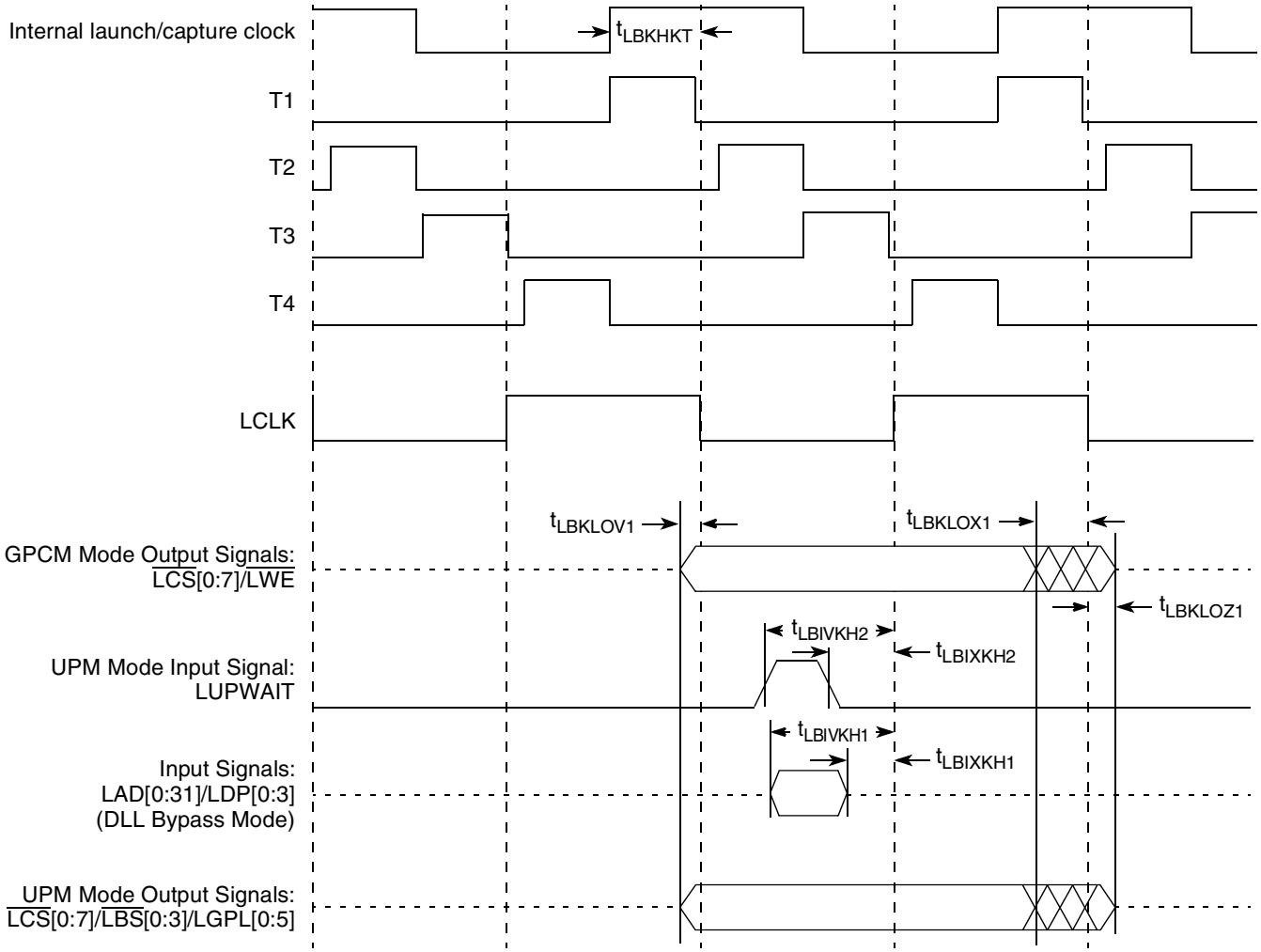


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

Figure 16 provides the AC test load for the I^2C.

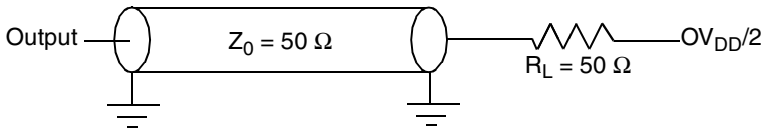


Figure 37. I^2C AC Test Load

Figure 38 shows the AC timing diagram for the I^2C bus.

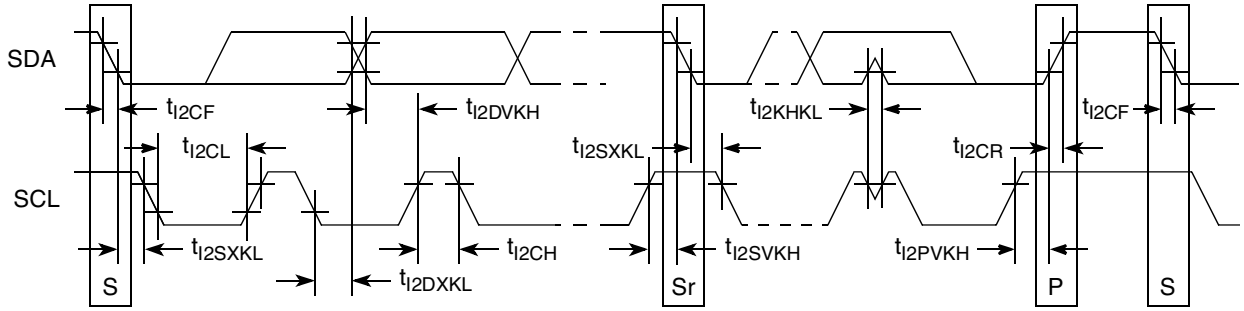


Figure 38. I^2C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8555E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8555E.

Table 41. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$	—	±5	µA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 40 shows the PCI input AC timing conditions.

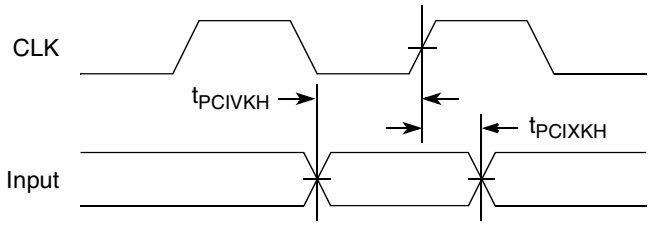


Figure 40. PCI Input AC Timing Measurement Conditions

Figure 41 shows the PCI output AC timing conditions.

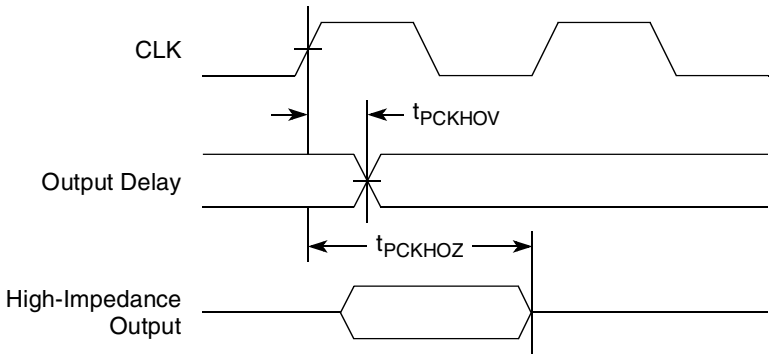


Figure 41. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8555E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 45 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

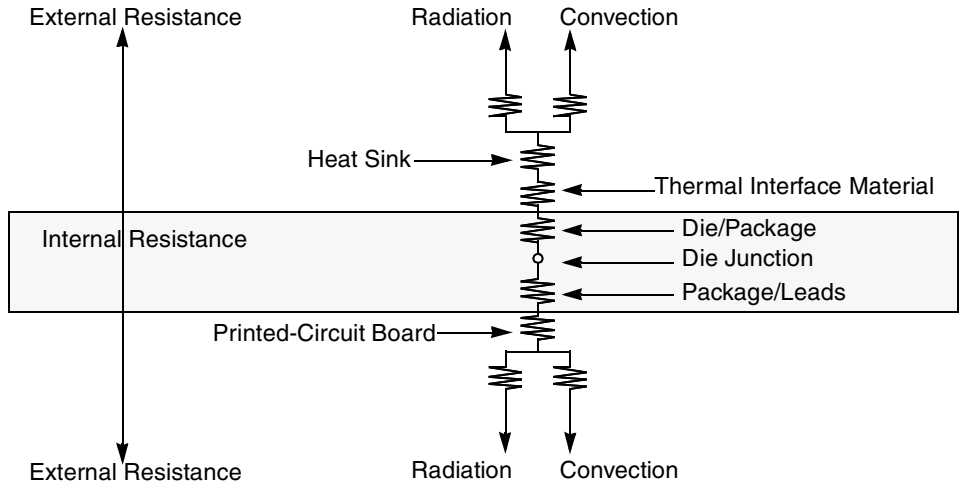


Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 46 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 42). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

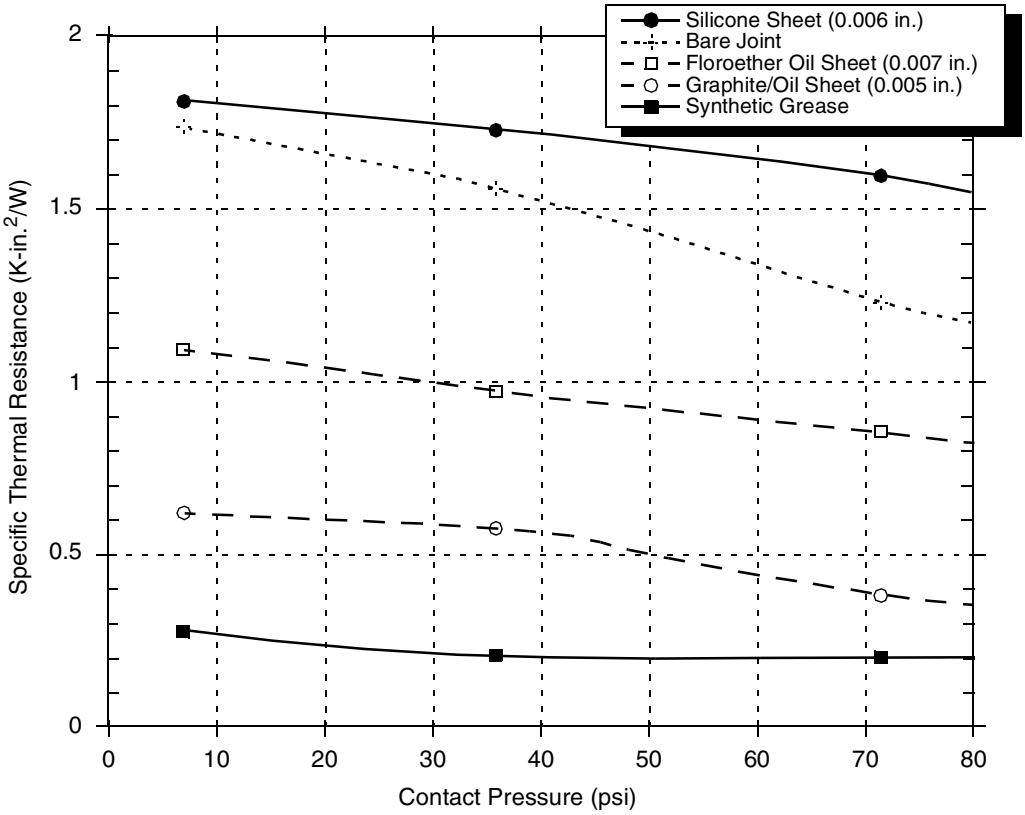


Figure 46. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St.	800-347-4572

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 48 and provide exploded views of the plastic fence, heat sink, and spring clip.

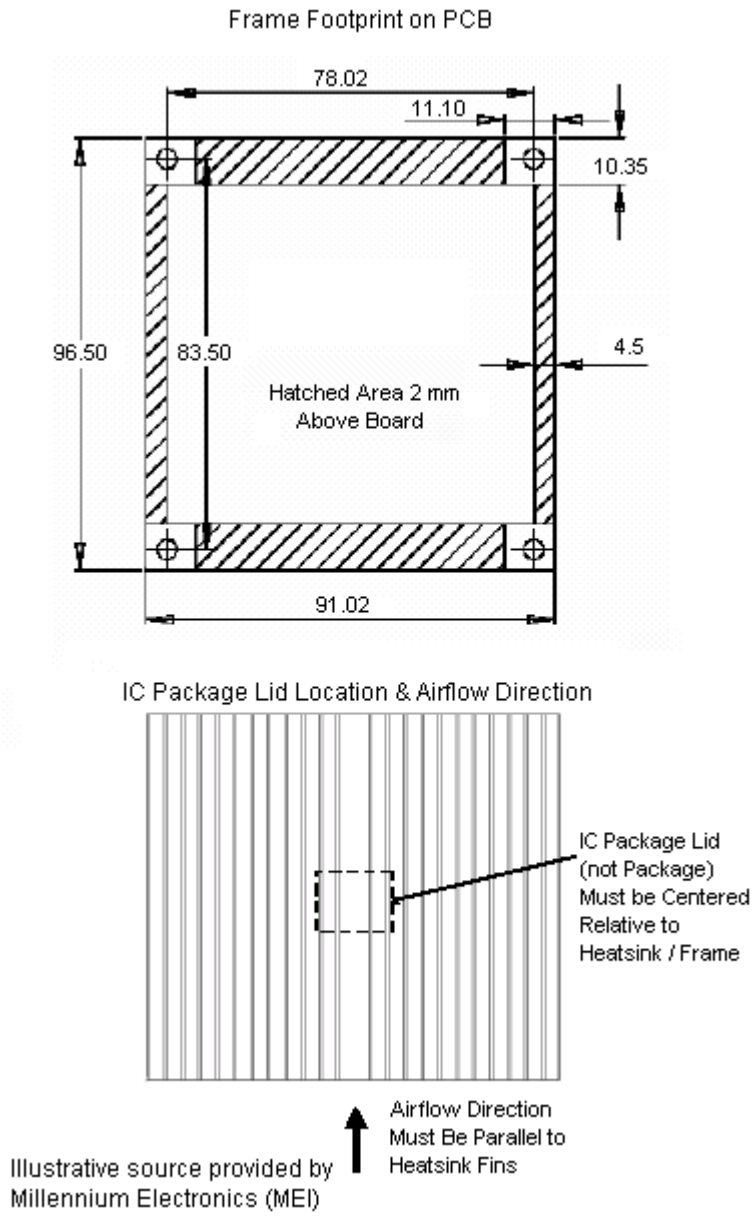


Figure 48. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, "Platform/System PLL Ratio."
2. The e500 Core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, "e500 Core PLL Ratio."
3. The CPM PLL ($AV_{DD}3$) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL ($AV_{DD}4$) generates the clocking for the first PCI bus.
5. The PCI2 PLL ($AV_{DD}5$) generates the clock for the second PCI bus.

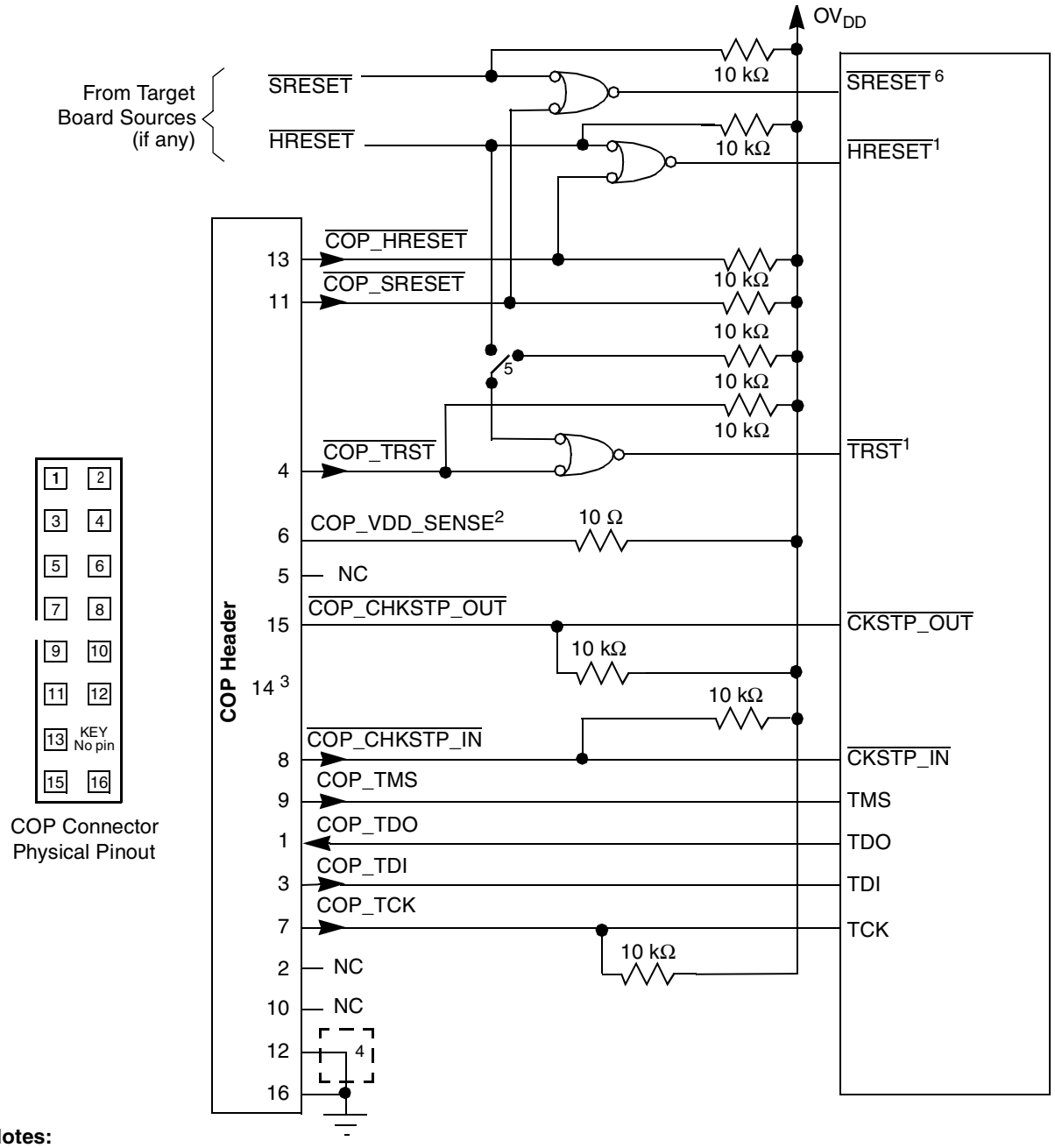
17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, and $AV_{DD}5$ respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 50, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	7/2007	Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Added footnote 2 about junction temperature in Table 4. Added max. power values for 1000 MHz core frequency in Table 4. Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30. Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values inTable 30. Added note 3 to $t_{LBKHOV1}$ in Table 30. Modified note 3 in Table 30 and Table 31. Added note 3 to $t_{LBKLOV1}$ in Table 31. Modified values for t_{LBKHKT}, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31. Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21. Modified note for signal CLK_OUT in Table 43. PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43. Added column for Encryption Acceleration in Table 52.
3	8/2005	Modified max. power values in Table 4. Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43.
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31. Added note 2 in Table 7. Modified min and max values for t_{DDKHMP} in Table 14.
1	6/2005	Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface in Table 27. Modified footnote 4 and changed typical power for the 1000 MHz core frequency inTable 4. Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31.
0	6/2005	Initial release.

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Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
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Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

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