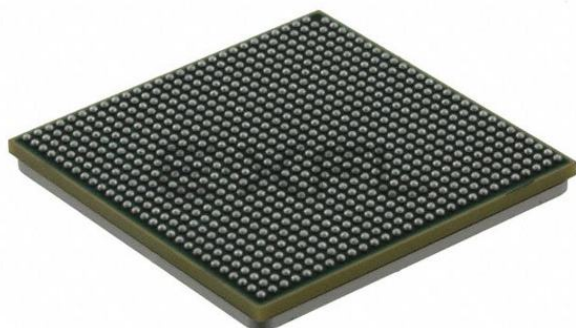




Welcome to [E-XFL.COM](#)

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8555vtalf

- Security Engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std 802.11i™, iSCSI, and IKE processing. The Security Engine contains 4 Crypto-channels, a Controller, and a set of crypto Execution Units (EUs). The Execution Units are:
 - Public Key Execution Unit (PKEU) supporting the following:
 - RSA and Diffie-Hellman
 - Programmable field size up to 2048-bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511-bits
 - Data Encryption Standard Execution Unit (DEU)
 - DES, 3DES
 - Two key (K1, K2) or Three Key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced Encryption Standard Unit (AESU)
 - Implements the Rijndael symmetric key cipher
 - Key lengths of 128, 192, and 256 bits. Two key
 - ECB, CBC, CCM, and Counter modes
 - ARC Four execution unit (AFEU)
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message Digest Execution Unit (MDEU)
 - SHA with 160-bit or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random Number Generator (RNG)
 - 4 Crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 Bytes for each execution unit, with flow control for large data sizes
- High-performance RISC CPM operating at up to 333 MHz
 - CPM software compatibility with previous PowerQUICC families
 - One instruction per clock
 - Executes code from internal ROM or instruction RAM
 - 32-bit RISC architecture
 - Tuned for communication environments: instruction set supports CRC computation and bit manipulation.
 - Internal timer
 - Interfaces with the embedded e500 core processor through a 32-Kbyte dual-port RAM and virtual DMA channels for each peripheral controller
 - Handles serial protocols and virtual DMA

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
 - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 32-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI
 - Four inbound windows
 - Four outbound windows plus default translation for PCI
- DDR memory controller
 - Programmable timing supporting first generation DDR SDRAM
 - 64-bit data interface, up to MHz data rate
 - Four banks of memory supported, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Sleep mode support for self refresh DDR SDRAM
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access via JTAG port
 - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages

- 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
 - Three-port crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no-snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI Controllers
 - PCI 2.2 compatible
 - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
 - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8555E for the 3.3-V signals, respectively.

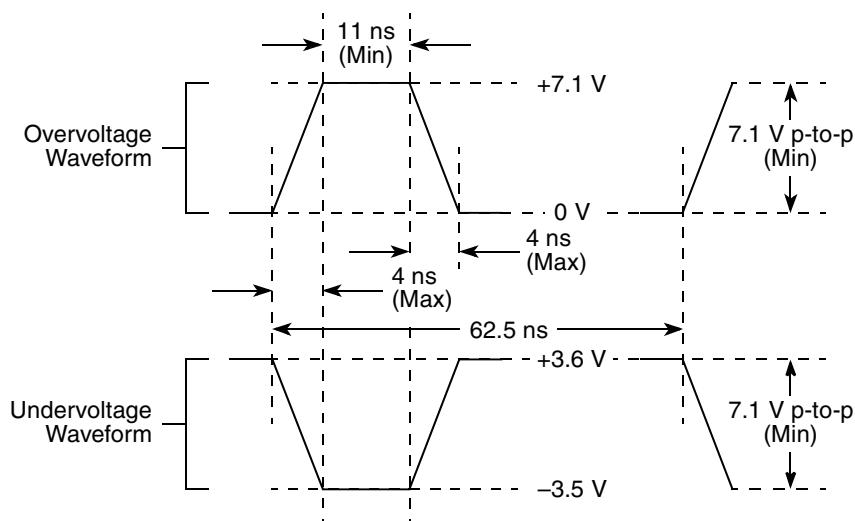


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	$OV_{DD} = 3.3\text{ V}$	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	$GV_{DD} = 2.5\text{ V}$	
TSEC/10/100 signals	42	$LV_{DD} = 2.5/3.3\text{ V}$	
DUART, system control, I2C, JTAG	42	$OV_{DD} = 3.3\text{ V}$	

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the PCI interface is determined by the setting of the `PCI_GNT1` signal at reset.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	$GV_{DD} + 0.3$	V	—
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR $\leq$ 266 MHz	t_{DISKEW}	—	750 1125	ps	1

Note:

- Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$) or ECC (MECC[{0...7}] if $n = 8$).

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	–1000 –1100 –1200	200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	2.8 3.45 4.6	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	2.0 2.65 3.8	—	ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.8 3.45 4.6	—	ns	4

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

Table 20. GMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise and fall times	$t_{GTXR}^3, t_{GTXF}^{2,4}$	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

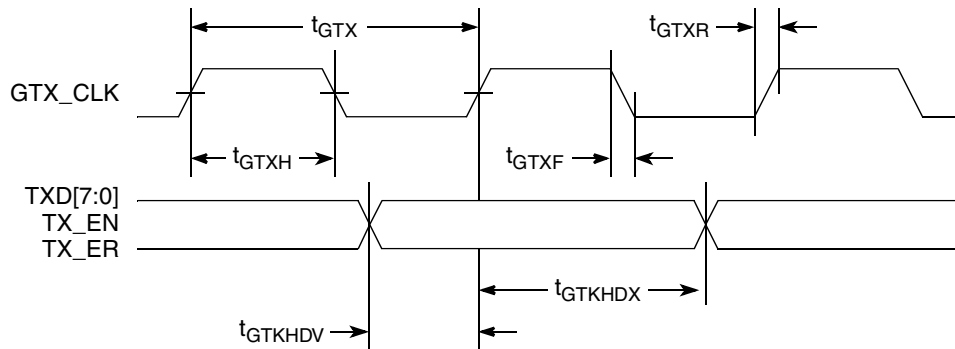


Figure 7. GMII Transmit AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}^2	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR} , $t_{MTXF}^{2,3}$	1.0	—	4.0	ns

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

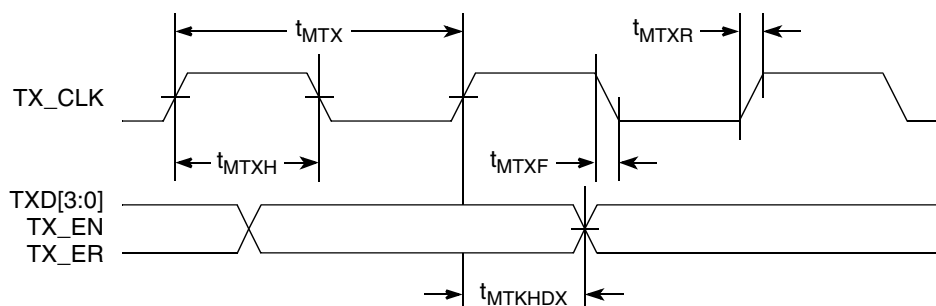


Figure 10. MII Transmit AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}^{5}	–500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}^{6}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ⁴	t_{RGTH}/t_{RGT}^{6}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ³	t_{RGTH}/t_{RGT}^{6}	40	50	60	%
Rise and fall times	$t_{RGTR}^{6,7}, t_{RGTF}^{6,7}$	—	—	0.75	ns

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Guaranteed by characterization.
- Guaranteed by design.
- Signal timings are measured at 0.5 and 2.0 V voltage levels.

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKHOZ2}	—	2.8	ns	5, 9
	$\overline{\text{LWE}}[0:1] = 11$ (default)			4.2		

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC_IN for DLL enabled mode.
- All signals are measured from $\text{OV}_{\text{DD}}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times \text{OV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{OV}_{\text{DD}}/2$.
- Guaranteed by characterization.
- Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHK1}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		t_{LBKSKEW}	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		t_{LBIVKH1}	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock		t_{LBIVKH2}	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		t_{LBIXKH1}	−1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock		t_{LBIXKH2}	−0.8	—	ns	3, 4
LAL output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LAL)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV1}	—	0.5	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV2}	—	0.7	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.2		

Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to address valid for LAD	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV3}	—	0.8	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.3		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOX1}	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)		–1.8			
Output hold from local bus clock for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOX2}	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)		–1.8			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOZ1}	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.4		
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOZ2}	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.4		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $\text{OV}_{\text{DD}}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times \text{OV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{OV}_{\text{DD}}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.

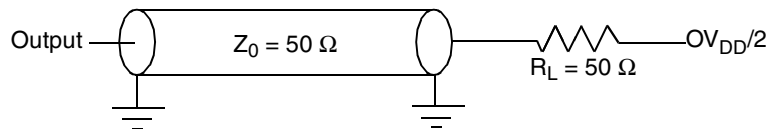

Figure 16. Local Bus C Test Load

Figure 36 provides the test access port timing diagram.

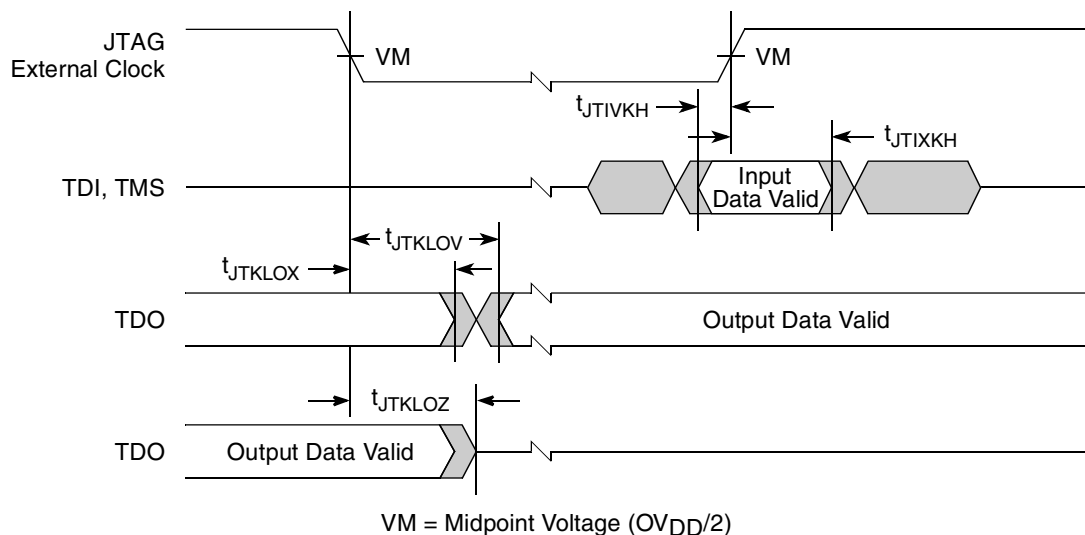


Figure 36. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8555E.

12.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8555E.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$)	I_I	-10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]	T18, T19, T20, T21	O	OV _{DD}	5, 7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV _{DD}	—
LALE	V21	O	OV _{DD}	5, 8, 9
LBCTL	V20	O	OV _{DD}	9
LCKE	U23	O	OV _{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV _{DD}	—
LCS[0:4]	Y27, Y28, W27, W28, R27	O	OV _{DD}	—
LCS5/DMA_DREQ2	R28	I/O	OV _{DD}	1
LCS6/DMA_DACK2	P27	O	OV _{DD}	1
LCS7/DMA_DDONE2	P28	O	OV _{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV _{DD}	—
LGPL0/LSDA10	U19	O	OV _{DD}	5, 9
LGPL1/LSDWE	U22	O	OV _{DD}	5, 9
LGPL2/LOE/LSDRAS	V28	O	OV _{DD}	5, 8, 9
LGPL3/LSDCAS	V27	O	OV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	V23	I/O	OV _{DD}	21
LGPL5	V22	O	OV _{DD}	5, 9
LSYNC_IN	T27	I	OV _{DD}	—
LSYNC_OUT	T28	O	OV _{DD}	—
LWE[0:1]/LSDDQM[0:1]/LBS[0:1]	AB28, AB27	O	OV _{DD}	1, 5, 9
LWE[2:3]/LSDDQM[2:3]/LBS[2:3]	T23, P24	O	OV _{DD}	1, 5, 9
DMA				
DMA_DREQ[0:1]	H5, G4	I	OV _{DD}	—
DMA_DACK[0:1]	H6, G5	O	OV _{DD}	—
DMA_DDONE[0:1]	H7, G6	O	OV _{DD}	—
Programmable Interrupt Controller				
MCP	AG17	I	OV _{DD}	—
UDE	AG16	I	OV _{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV _{DD}	—
IRQ8	AB20	I	OV _{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV _{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV _{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV _{DD}	1
IRQ_OUT	AB21	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV _{DD}	5, 9
EC_MDIO	E1	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV _{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV _{DD}	9, 18
TSEC1_TX_EN	C8	O	LV _{DD}	11
TSEC1_TX_ER	B8	O	LV _{DD}	—
TSEC1_TX_CLK	C6	I	LV _{DD}	—
TSEC1_GTX_CLK	B6	O	LV _{DD}	—
TSEC1_CRS	C3	I	LV _{DD}	—
TSEC1_COL	G7	I	LV _{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV _{DD}	—
TSEC1_RX_DV	D2	I	LV _{DD}	—
TSEC1_RX_ER	E5	I	LV _{DD}	—
TSEC1_RX_CLK	D6	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV _{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV _{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV _{DD}	11
TSEC2_TX_ER	D11	O	LV _{DD}	—
TSEC2_TX_CLK	D10	I	LV _{DD}	—
TSEC2_GTX_CLK	C10	O	LV _{DD}	—

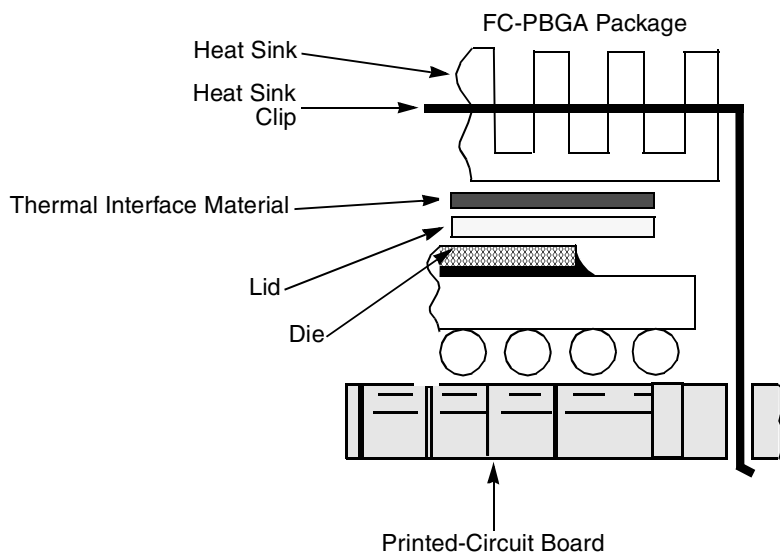


Figure 43. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8555E. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 45 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

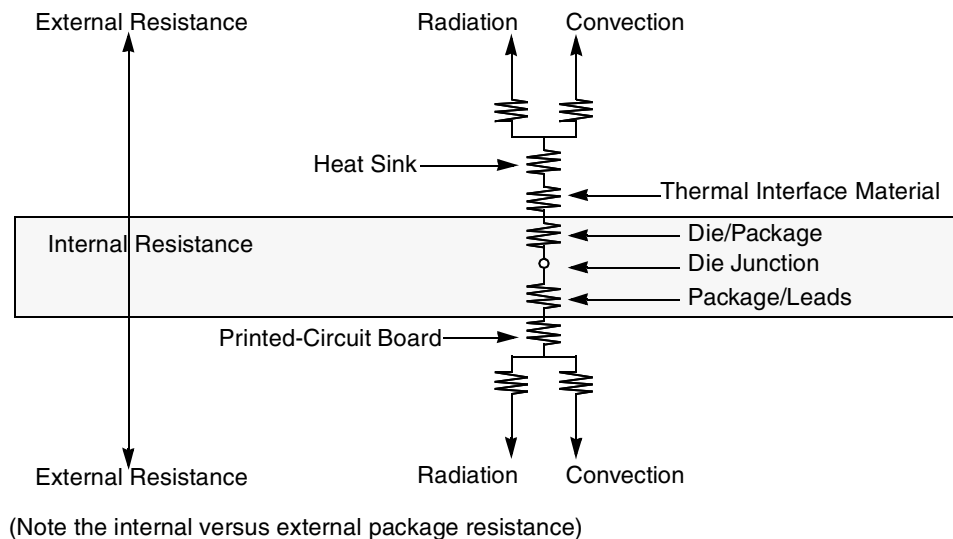


Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 46 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 42). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

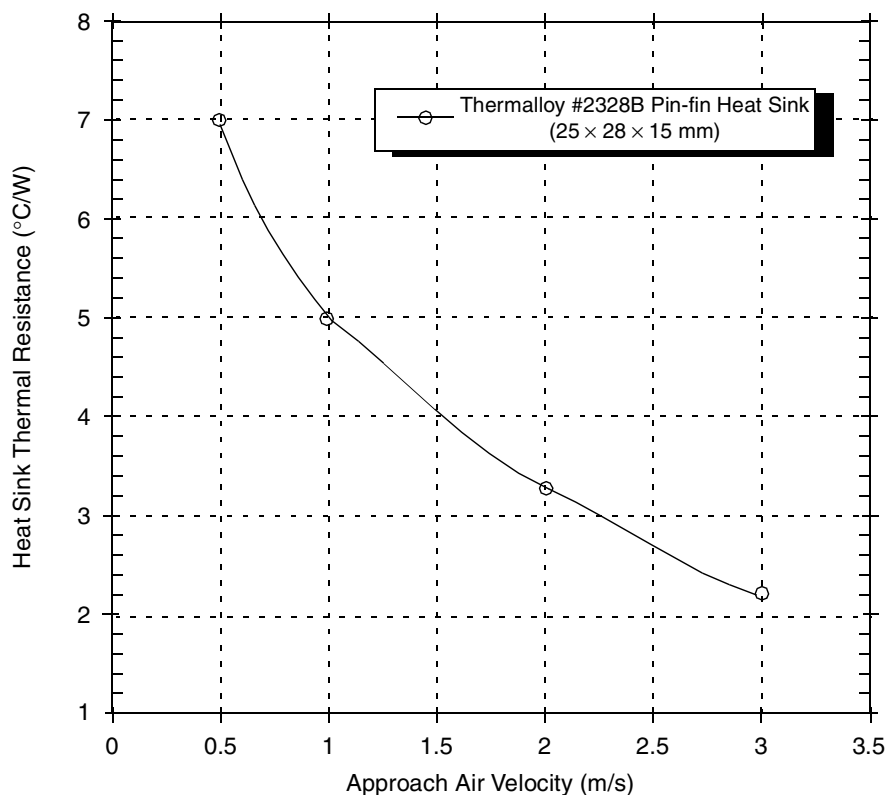


Figure 47. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in [Table 49](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

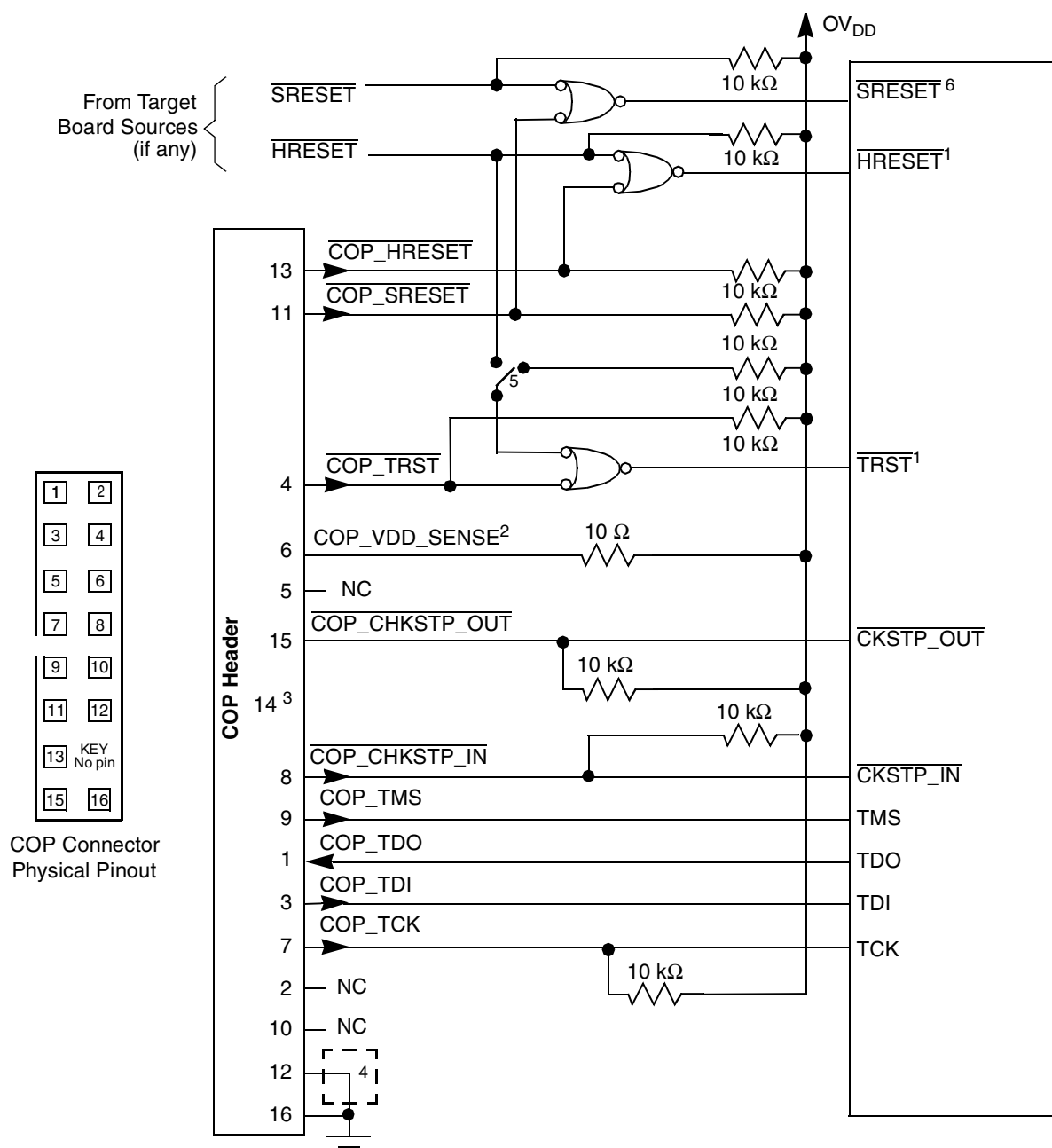
Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 48](#) and [Figure 49](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



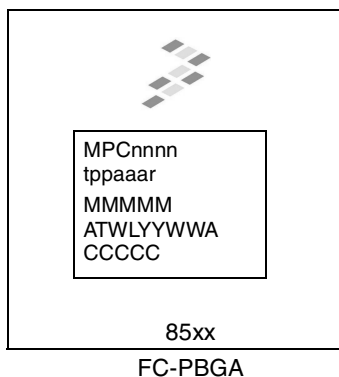
Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

19.2 Part Marking

Parts are marked as the example shown in [Figure 54](#).



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. IEEE 802.3 and 1149.1 are registered trademarks of the Institute of Electrical and Electronics Engineers, Inc. (IEEE). This product is not endorsed or approved by the IEEE. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2008. All rights reserved.

