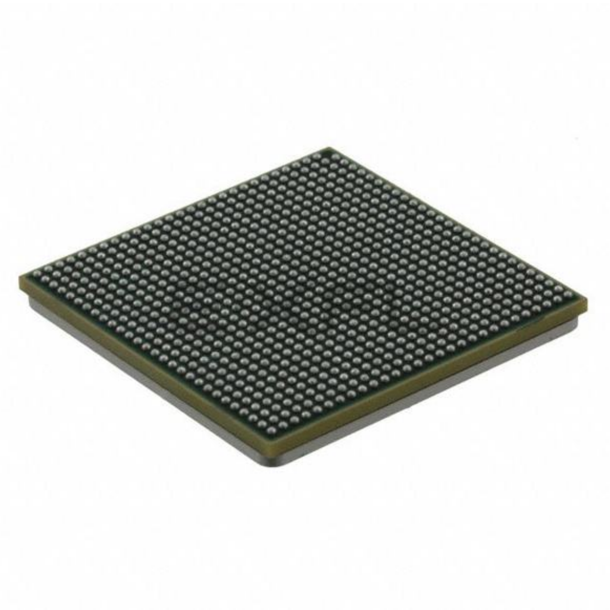

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8555vtaqf

- Two full-duplex fast communications controllers (FCCs) that support the following protocols:
  - ATM protocol through two UTOPIA level 2 interfaces
  - IEEE Std 802.3™/Fast Ethernet (10/100)
  - HDLC
  - Totally transparent operation
- Three full-duplex serial communications controllers (SCCs) support the following protocols:
  - High level/synchronous data link control (HDLC/SDLC)
  - LocalTalk (HDLC-based local area network protocol)
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART (1x clock mode)
  - Binary synchronous communication (BISYNC)
  - Totally transparent operation
  - QMC support, providing 64 channels per SCC using only one physical TDM interface
- Universal serial bus (USB) controller that is full/low-speed compliant (multiplexed on an SCC)
  - USB host mode
  - Supports USB slave mode
- Serial peripheral interface (SPI) support for master or slave
- I^2C bus controller
- Two serial management controllers (SMCs) supporting:
  - UART
  - Transparent
  - General-circuit interfaces (GCI)
- Time-slot assigner supports multiplexing of data from any of the SCCs and FCCs onto eight time-division multiplexed (TDM) interfaces. The time-slot assigner supports the following TDM formats:
  - T1/CEPT lines
  - T3/E3
  - Pulse code modulation (PCM) highway interface
  - ISDN primary rate
  - Freescale interchip digital link (IDL)
  - General circuit interface (GCI)
- User-defined interfaces
- Eight independent baud rate generators (BRGs)
- Four general-purpose 16-bit timers or two 32-bit timers
- General-purpose parallel ports—16 parallel I/O lines with interrupt capability

• 256 Kbytes of on-chip memory
- Can act as a 256-Kbyte level-2 cache
- Can act as a 256-Kbyte or two 128-Kbyte memory-mapped SRAM arrays

    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1000 Mbps RGMII/RTBI
  - Full- and half-duplex support
  - Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - 2-Kbyte internal transmit and receive FIFOs
  - MII management interface for control and status
  - Programmable CRC generation and checking
- OCeaN switch fabric
  - Three-port crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no-snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI Controllers
  - PCI 2.2 compatible
  - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
  - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8555E may drive a logic one or zero during power-up.

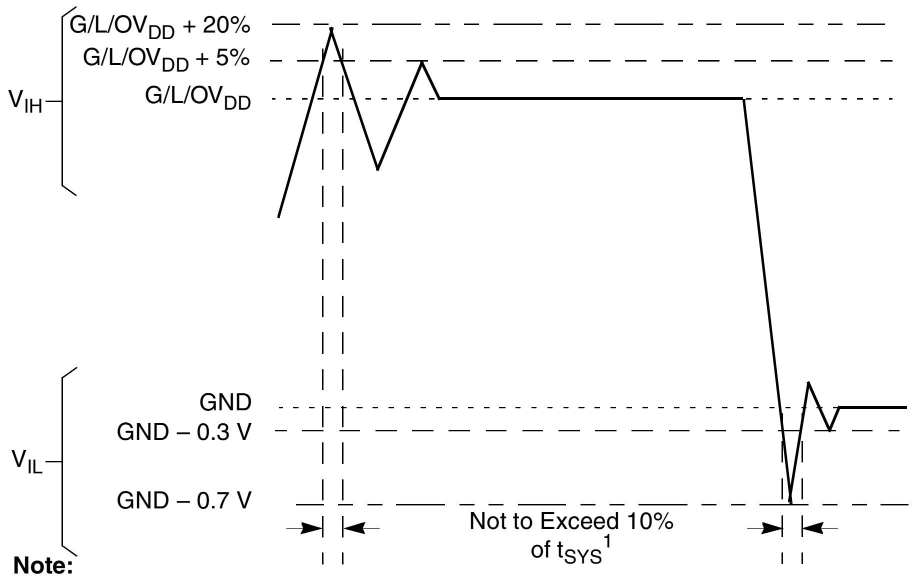
2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8555E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V ± 60 mV 1.3 V± 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V ± 60 mV 1.3 V ± 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8555E.



Note:
1. Note that t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8555E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Table 5. Typical I/O Power Dissipation

Interface	Parameters	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	—
	CCB = 266 MHz	0.59	—	—	—	W	—
	CCB = 300 MHz	0.66	—	—	—	W	—
	CCB = 333 MHz	0.73	—	—	—	W	—
PCI I/O	64b, 66 MHz	—	0.14	—	—	W	—
	64b, 33 MHz	—	0.08	—	—	W	—
	32b, 66 MHz	—	0.07	—	—	W	Multiply by 2 if using two 32b ports
	32b, 33 MHz	—	0.04	—	—	W	
Local Bus I/O	32b, 167 MHz	—	0.30	—	—	W	—
	32b, 133 MHz	—	0.24	—	—	W	—
	32b, 83 MHz	—	0.16	—	—	W	—
	32b, 66 MHz	—	0.13	—	—	W	—
	32b, 33 MHz	—	0.07	—	—	W	—
TSEC I/O	MII	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	0.07	—	W	
	RGMII or RTBI	—	—	—	0.04	W	
CPM - FCC	MII	—	0.015	—	—	W	—
	RMII	—	0.013	—	—	W	—
	HDLC 16 Mbps	—	0.009	—	—	W	—
	UTOPIA-8 SPHY	—	0.06	—	—	W	—
	UTOPIA-8 MPHY	—	0.1	—	—	W	—
	UTOPIA-16 SPHY	—	0.094	—	—	W	—
	UTOPIA-16 MPHY	—	0.135	—	—	W	—
CPM - SCC	HDLC 16 Mbps	—	0.004	—	—	W	—
TDMA or TDMB	Nibble Mode	—	0.01	—	—	W	—
TDMA or TDMB	Per Channel	—	0.005	—	—	W	Up to 4 TDM channels, multiply by number of TDM channels.

7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8555E.

Table 17. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB_CLK} / 1048576	baud	3
Maximum baud rate	f_{CCB_CLK} / 16	baud	1, 3
Oversample rate	16	—	2, 3

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
3. Guaranteed by design.

8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 18 and Table 19. The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (for example, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

Table 21. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

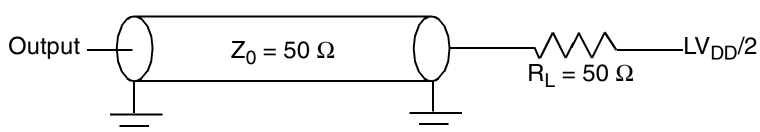


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

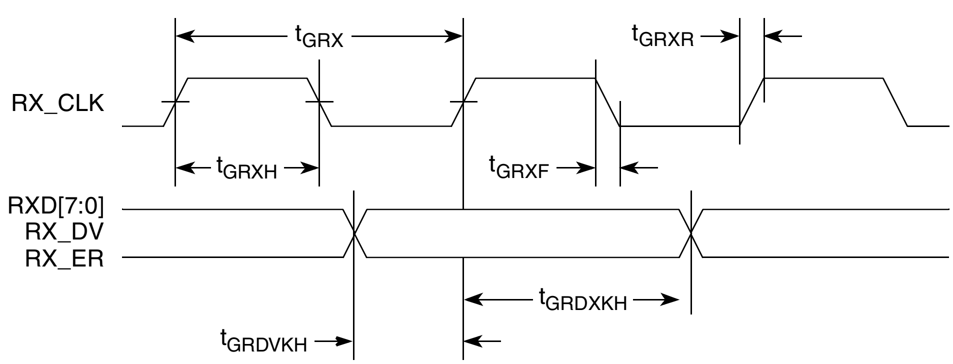


Figure 9. GMII Receive AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 25 provides the TBI receive AC timing specifications.

Table 25. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}		16.0		ns
RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF} [2,3]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

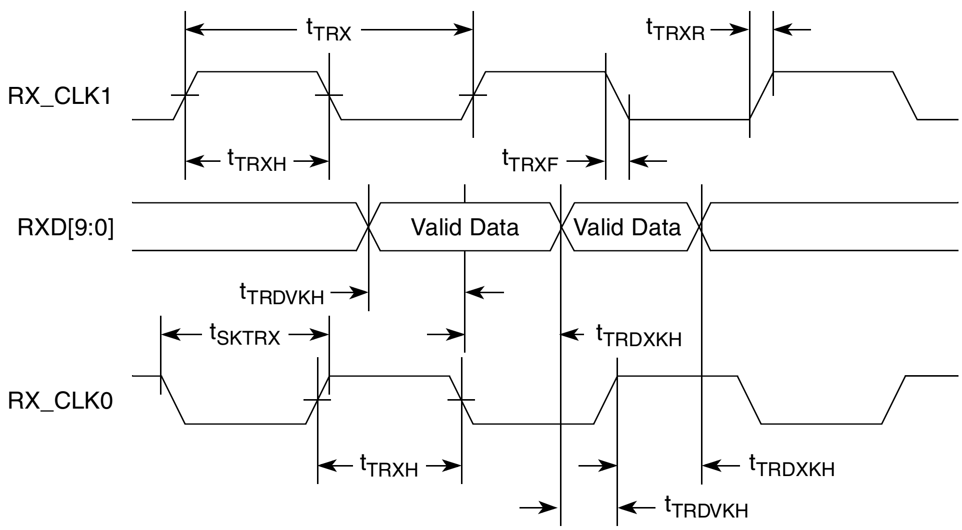


Figure 13. TBI Receive AC Timing Diagram

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOZ2}$	—	2.8	ns	5, 9
	$\overline{LWE[0:1]}$ = 11 (default)			4.2		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{LWE[0:1]}$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHKT}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	–1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	–0.8	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKLOV1}$	—	0.5	ns	3
	$\overline{LWE[0:1]}$ = 11 (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKLOV2}$	—	0.7	ns	3
	$\overline{LWE[0:1]}$ = 11 (default)			2.2		

Figure 17 to Figure 22 show the local bus signals.

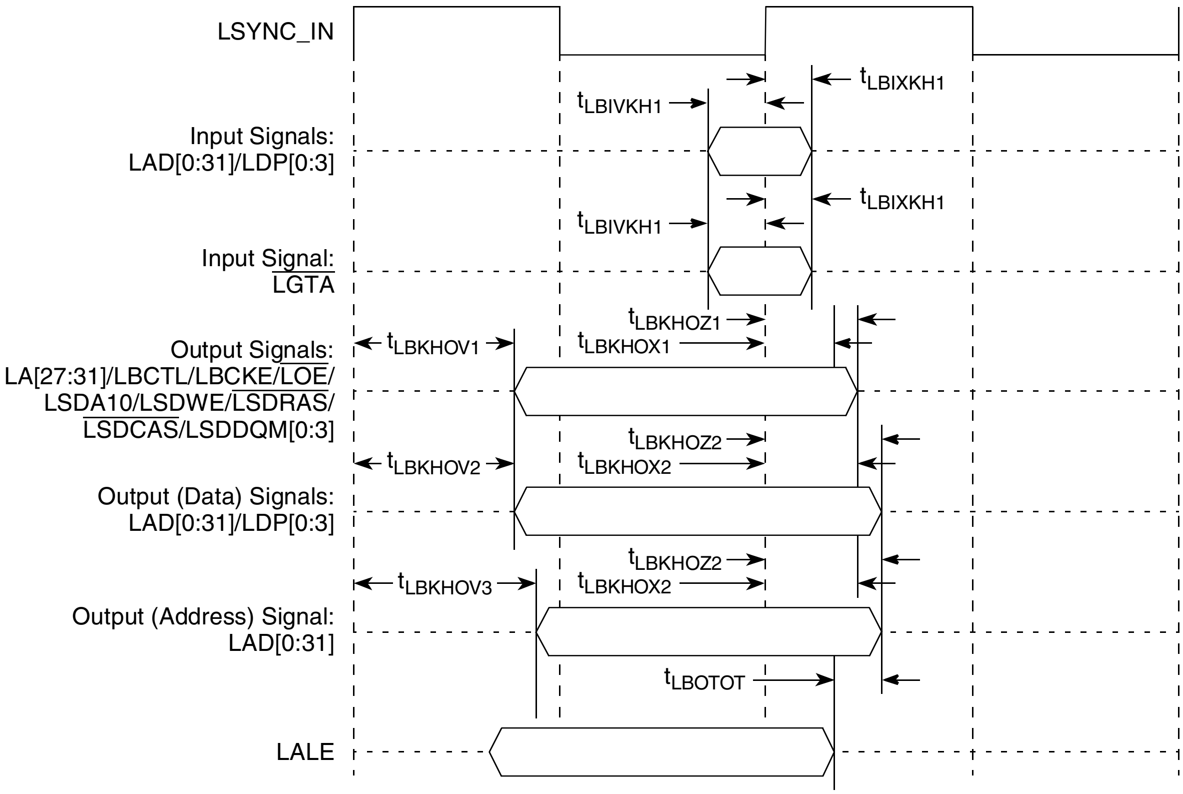


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

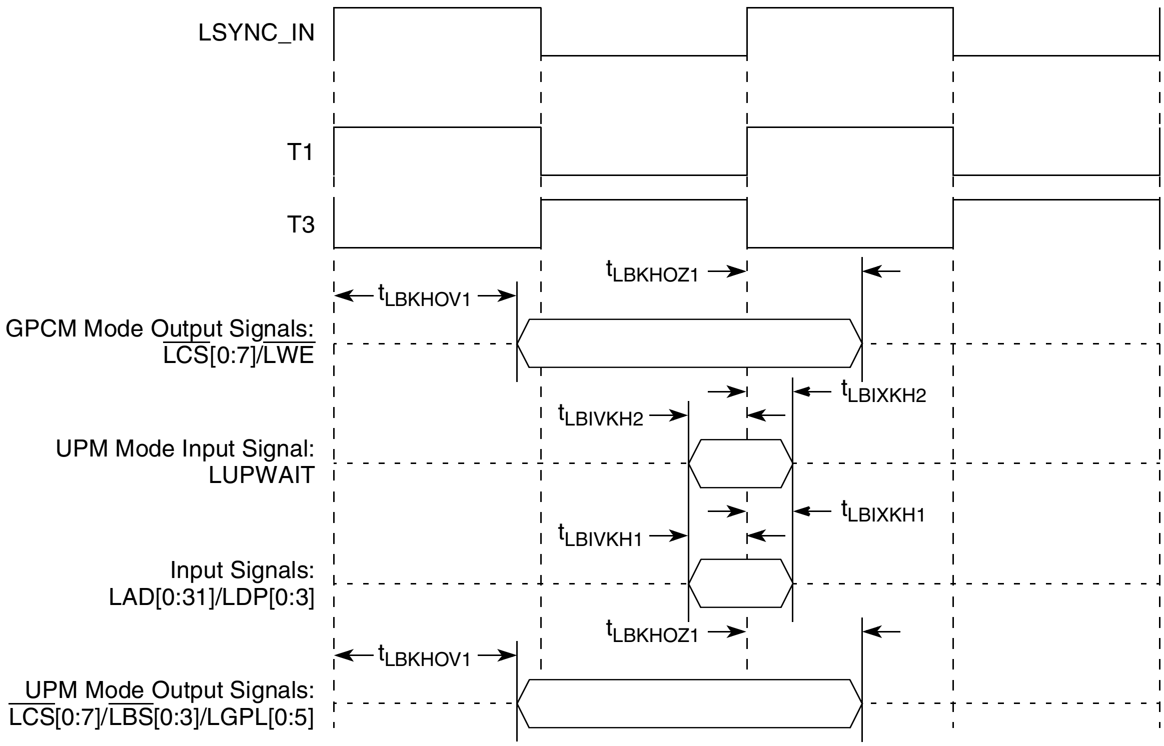


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

Table 33. CPM Input AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min[3]	Unit
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns
PIO inputs—input setup time	t_{PIIVKH}	8	ns
PIO inputs—input hold time	t_{PIIXKH}	1	ns
COL width high (FCC)	t_{FCCH}	1.5	CLK

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time. And t_{TDIXKH} symbolizes the TDM timing (TD) with respect to the time the input signals (I) reach the invalid state (X) relative to the reference clock t_{FCC} (K) going to the high (H) state or hold time.
3. PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Table 34. CPM Output AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t_{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t_{FEKHOX}	2	8	ns
SCC/SMC/SPI outputs—internal clock (NMSI) delay	t_{NIKHOX}	0.5	10	ns
SCC/SMC/SPI outputs—external clock (NMSI) delay	t_{NEKHOX}	2	8	ns
TDM outputs/SI delay	t_{TDKHOX}	2.5	11	ns
PIO outputs delay	t_{PIKHOX}	1	11	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the CPM.

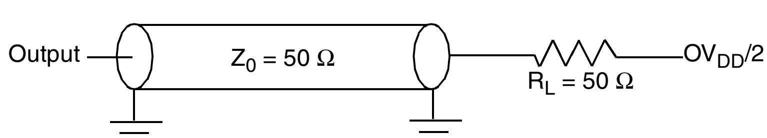
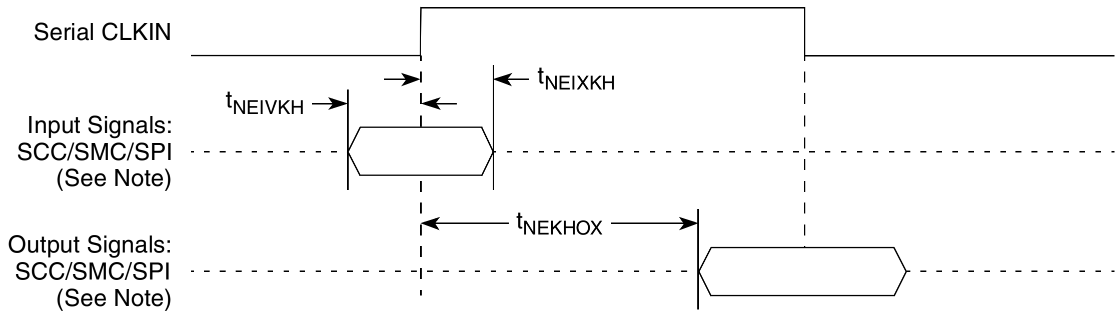


Figure 23. CPM AC Test Load

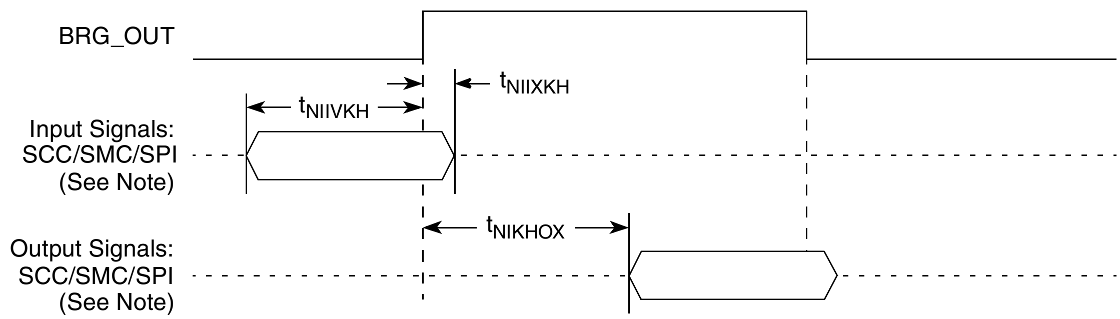
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

[1] SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

[2] SPI AC timings refer always to SPICLK.

12.2 I²C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I²C interface of the MPC8555E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [6]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [6]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [6]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [6]	0.6	—	µs
Data setup time	t_{I2DVKH} [6]	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	µs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$ [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8555E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
9. Guaranteed by characterization.
10. Guaranteed by design.

Figure 16 provides the AC test load for PCI.

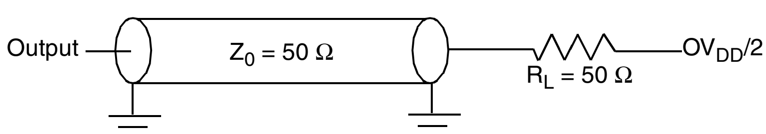


Figure 39. PCI AC Test Load

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	5, 7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	5, 8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	—
$\overline{\text{LCS5}}$/DMA_DREQ2	R28	I/O	OV_{DD}	1
$\overline{\text{LCS6}}$/DMA_DACK2	P27	O	OV_{DD}	1
$\overline{\text{LCS7}}$/DMA_DDONE2	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	—
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	U22	O	OV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	V28	O	OV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	V27	O	OV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	21
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	—
LSYNC_OUT	T28	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:1]/LSDDQM[0:1]/ $\overline{\text{LBS}}$[0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
$\overline{\text{LWE}}$[2:3]/LSDDQM[2:3]/ $\overline{\text{LBS}}$[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
$\overline{\text{DMA\_DREQ}}$[0:1]	H5, G4	I	OV_{DD}	—
$\overline{\text{DMA\_DACK}}$[0:1]	H6, G5	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0:1]	H7, G6	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP}}$	AG17	I	OV_{DD}	—
$\overline{\text{UDE}}$	AG16	I	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	—
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/0	OV_{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/0	OV_{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/0	OV_{DD}	—

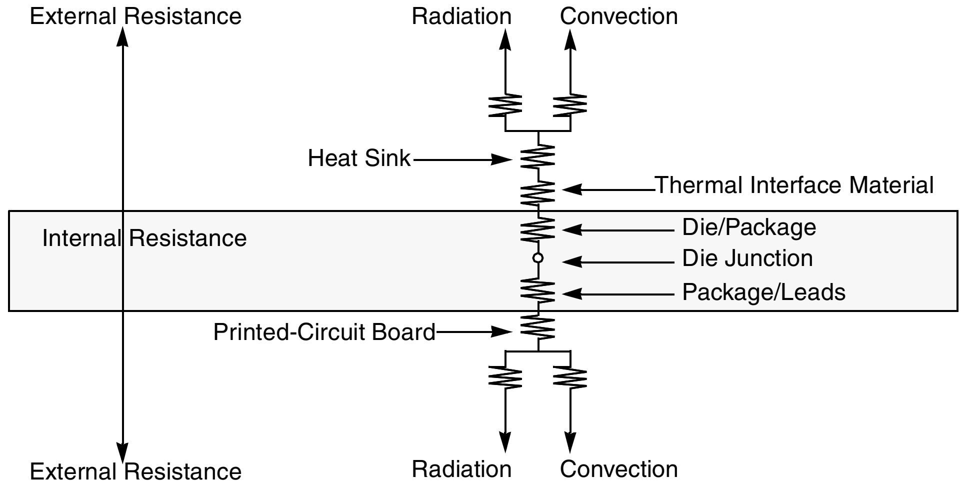
Notes:
1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA\_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
3. TEST_SEL0 must be pulled-high, TEST_SEL1 must be tied to ground.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8555E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 15.2, "Platform/System PLL Ratio."
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 15.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2\_C\_BE}}$[7:4]).
18. If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
19. Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OV_{DD}.
20. These are test signals for factory use only and must be pulled up (100Ω to 1kΩ) to OV_{DD} for normal machine operation.
21. If this signal is used as both an input and an output, a weak pull-up (~10kΩ) is required on this pin.
22. MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 45 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

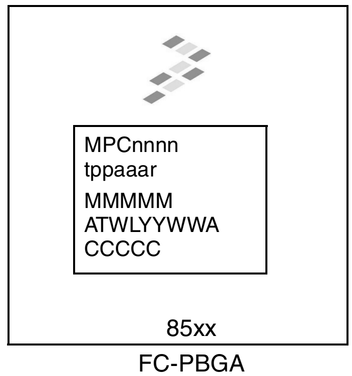
A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 46 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 42). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

19.2 Part Marking

Parts are marked as the example shown in Figure 54.



Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device