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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555cvtajd

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
 - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 32-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI
 - Four inbound windows
 - Four outbound windows plus default translation for PCI
- DDR memory controller
 - Programmable timing supporting first generation DDR SDRAM
 - 64-bit data interface, up to MHz data rate
 - Four banks of memory supported, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Sleep mode support for self refresh DDR SDRAM
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access via JTAG port
 - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.32 0.3 to 1.43 (for 1 GHz only)	V	
PLL supply voltage		AV_{DD}	−0.3 to 1.32 0.3 to 1.43 (for 1 GHz only)	V	
DDR DRAM I/O voltage		GV_{DD}	−0.3 to 3.63	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63 −0.3 to 2.75	V	
CPM, PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to ($LV_{DD} + 0.3$)	V	4, 5
	CPM, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$) ¹	V	5
	PCI	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (M,L,O) V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8555E requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- V_{DD} , AV_{DDn}
- GV_{DD} , LV_{DD} , OV_{DD} (I/O supplies)

Table 5. Typical I/O Power Dissipation

Interface	Parameters	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	—
	CCB = 266 MHz	0.59	—	—	—	W	—
	CCB = 300 MHz	0.66	—	—	—	W	—
	CCB = 333 MHz	0.73	—	—	—	W	—
PCI I/O	64b, 66 MHz	—	0.14	—	—	W	—
	64b, 33 MHz	—	0.08	—	—	W	—
	32b, 66 MHz	—	0.07	—	—	W	Multiply by 2 if using two 32b ports
	32b, 33 MHz	—	0.04	—	—	W	
Local Bus I/O	32b, 167 MHz	—	0.30	—	—	W	—
	32b, 133 MHz	—	0.24	—	—	W	—
	32b, 83 MHz	—	0.16	—	—	W	—
	32b, 66 MHz	—	0.13	—	—	W	—
	32b, 33 MHz	—	0.07	—	—	W	—
TSEC I/O	MII	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	0.07	—	W	
	RGMI or RTBI	—	—	—	0.04	W	
CPM - FCC	MII	—	0.015	—	—	W	—
	RMII	—	0.013	—	—	W	—
	HDLC 16 Mbps	—	0.009	—	—	W	—
	UTOPIA-8 SPHY	—	0.06	—	—	W	—
	UTOPIA-8 MPHY	—	0.1	—	—	W	—
	UTOPIA-16 SPHY	—	0.094	—	—	W	—
	UTOPIA-16 MPHY	—	0.135	—	—	W	—
CPM - SCC	HDLC 16 Mbps	—	0.004	—	—	W	—
TDMA or TDMB	Nibble Mode	—	0.01	—	—	W	—
TDMA or TDMB	Per Channel	—	0.005	—	—	W	Up to 4 TDM channels, multiply by number of TDM channels.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8555E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8555E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	-10	10	μA	4
Output high current ($V_{OUT} = 1.95$ V)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35$ V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	5	μA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

8.2.3.2 MII Receive AC Timing Specifications

Table 23 provides the MII receive AC timing specifications.

Table 23. MII Receive AC Timing Specifications

At recommended operating conditions with V_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}^{2}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	$t_{MRXR}, t_{MRXF}^{2,3}$	1.0	—	4.0	ns

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

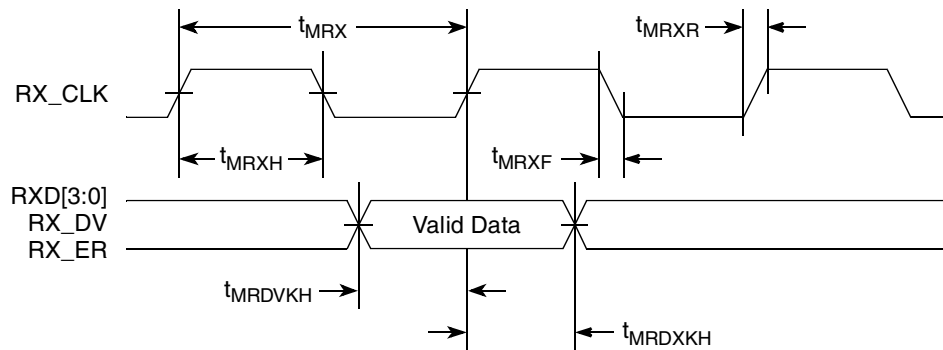


Figure 11. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	$t_{TTKHDTV}$	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR} , $t_{TTXF}^{2,3}$	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{TTKHDTV}$ symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

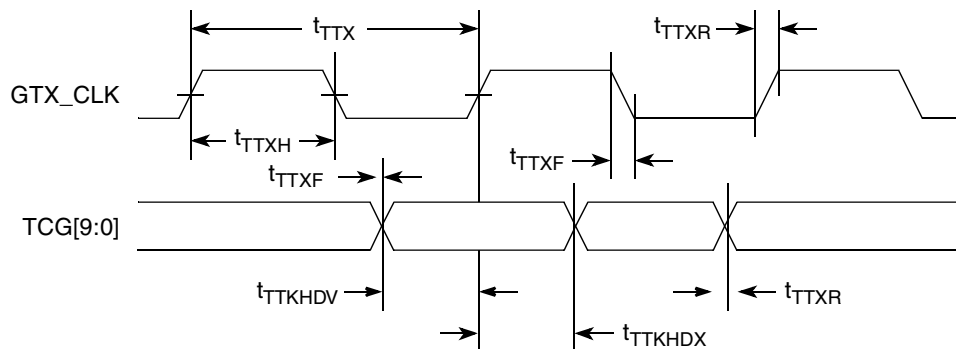


Figure 12. TBI Transmit AC Timing Diagram

Table 27. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input high current	I_{IH}	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	−600	—	μA

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is $3.3 \text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHVD}			$2 \cdot [1/(f_{ccb_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2 \cdot [1/(f_{ccb_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

Figure 17 to Figure 22 show the local bus signals.

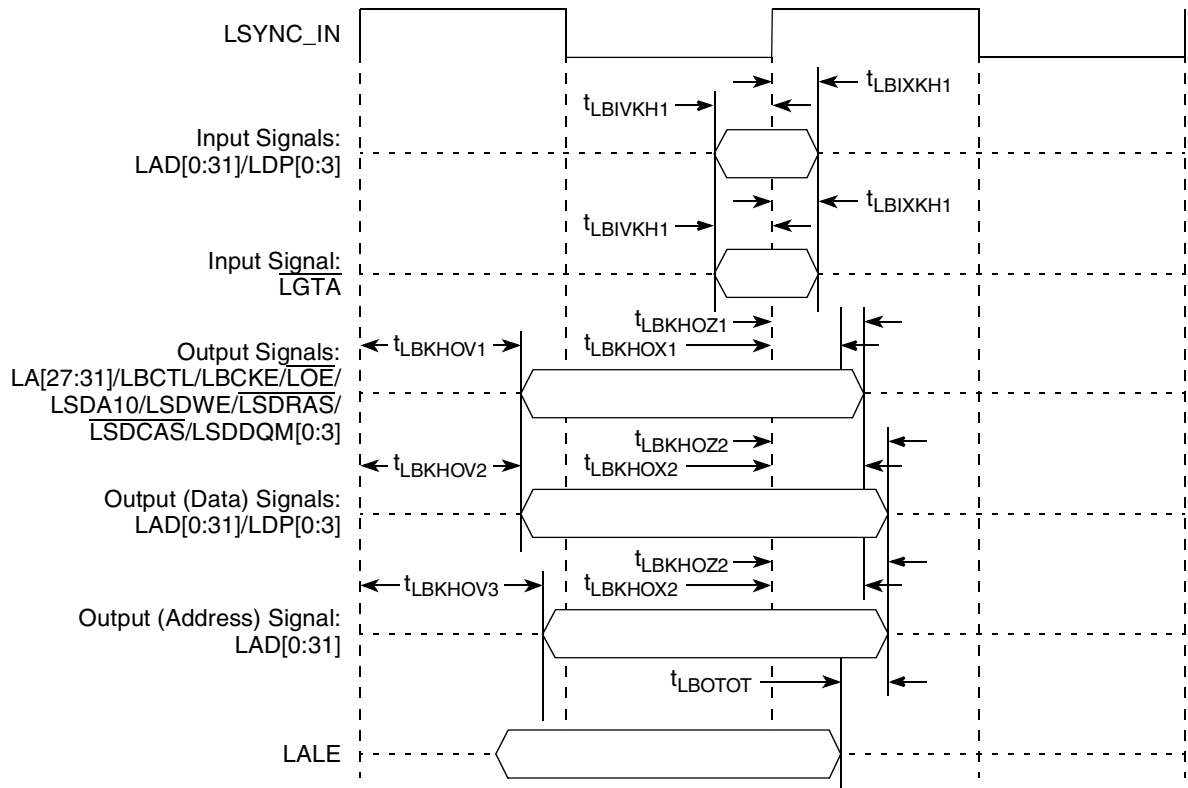


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

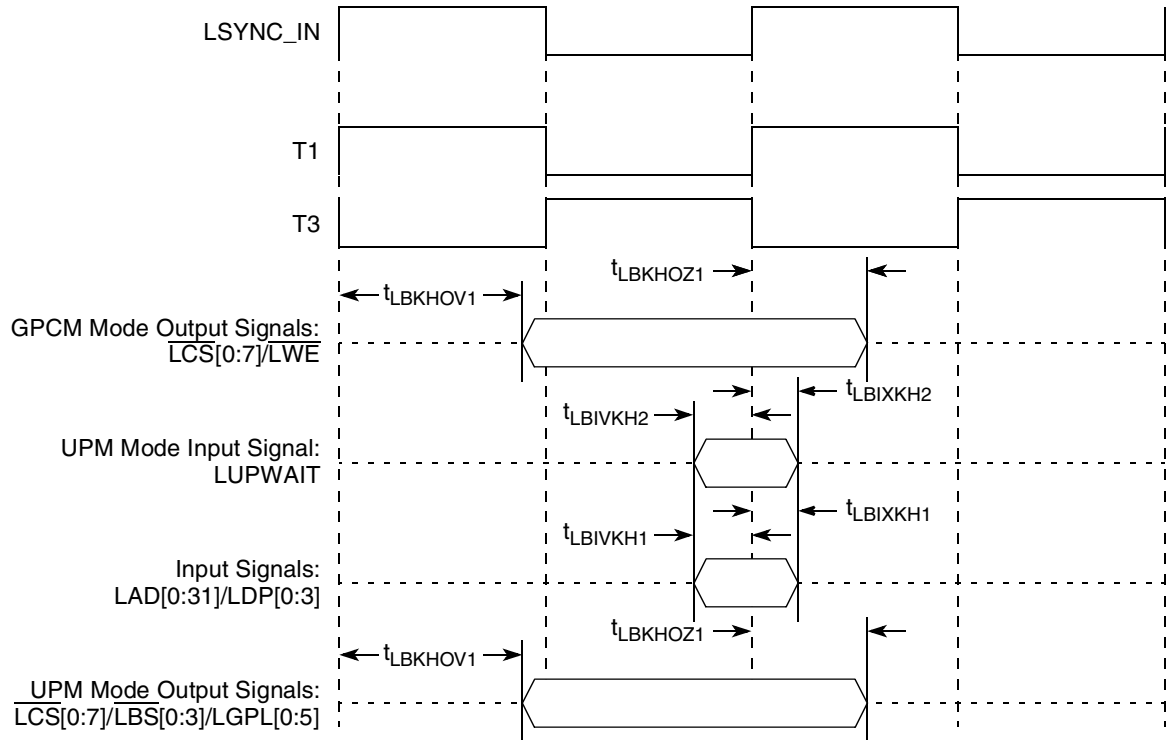


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8555E.

10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

Table 32. CPM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	3.465	V	1
Input low voltage	V_{IL}		GND	0.8	V	1, 2
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V	1
Output high voltage	V_{OH}	$I_{OH} = -2.0$ mA	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V	1

Note:

1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. $V_{IL}(\text{max})$ for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 33. CPM Input AC Timing Specifications ¹

Characteristic	Symbol ²	Min ³	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	6	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	t_{FEIXKH}^b	2	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	6	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SMC/SPI inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SMC/SPI inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	4	ns

Table 33. CPM Input AC Timing Specifications ¹ (continued)

Characteristic	Symbol ²	Min ³	Unit
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns
PIO inputs—input setup time	t_{PIIVKH}	8	ns
PIO inputs—input hold time	t_{PIIXKH}	1	ns
COL width high (FCC)	t_{FCCH}	1.5	CLK

Notes:

- Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time. And t_{TDIXKH} symbolizes the TDM timing (TD) with respect to the time the input signals (I) reach the invalid state (X) relative to the reference clock t_{FCC} (K) going to the high (H) state or hold time.
- PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Table 34. CPM Output AC Timing Specifications ¹

Characteristic	Symbol ²	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t_{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t_{FEKHOX}	2	8	ns
SCC/SMC/SPI outputs—internal clock (NMSI) delay	t_{NIKHOX}	0.5	10	ns
SCC/SMC/SPI outputs—external clock (NMSI) delay	t_{NEKHOX}	2	8	ns
TDM outputs/SI delay	t_{TDKHOX}	2.5	11	ns
PIO outputs delay	t_{PIKHOX}	1	11	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the CPM.

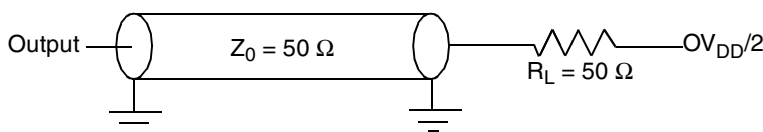

Figure 23. CPM AC Test Load

Table 35. I2C Timing (continued)

Characteristic	Expression	All Frequencies		Unit
		Min	Max	
SDA/SCL fall time	t_{SFALL}	-	$1/(33 * f_{SCL})$	s
Stop condition setup time	t_{SCHDH}	$2/(divider * f_{SCL})$	-	s

- Notes:**
- $F_{MAX} = BRGCLK / (min_divider * prescaler)$. Where $prescaler = 25 - I2MODE[PDIV]$; and $min_divider = 12$ if digital filter disabled and 18 if enabled.
 Example #1: if $I2MODE[PDIV] = 11$ ($prescaler = 4$) and $I2MODE[FLT] = 0$ (digital filter disabled) then $F_{MAX} = BRGCLK / 48$
 Example #2: if $I2MODE[PDIV] = 00$ ($prescaler = 32$) and $I2MODE[FLT] = 1$ (digital filter enabled) then $F_{MAX} = BRGCLK / 576$
 - $divider = f_{SCL} / prescaler$.
 In master mode: $divider = BRGCLK / (f_{SCL} * prescaler) = 2 * (I2BRG[DIV] + 3)$
 In slave mode: $divider = BRGCLK / (f_{SCL} * prescaler)$

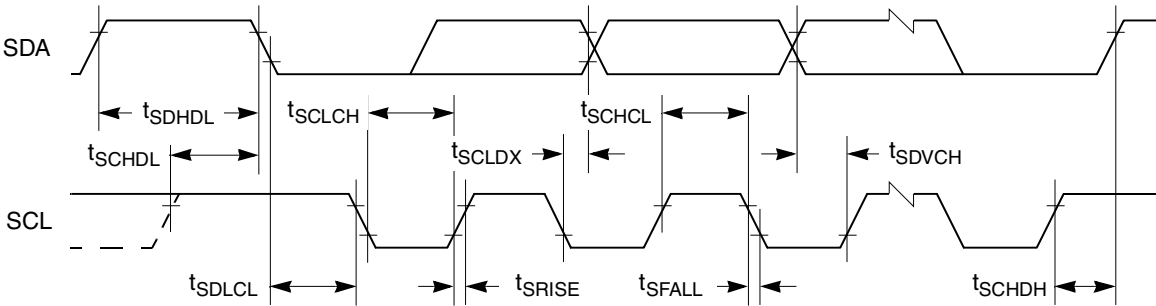


Figure 31. CPM I2C Bus Timing Diagram

Figure 32 provides the AC test load for TDO and the boundary-scan outputs of the MPC8555E.

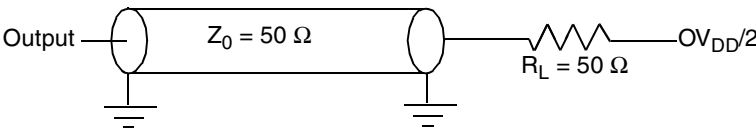


Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

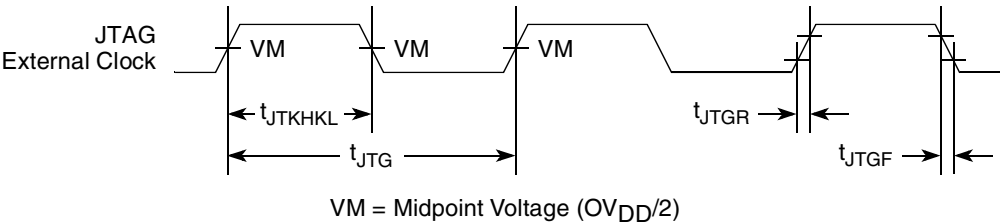


Figure 33. JTAG Clock Input Timing Diagram

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

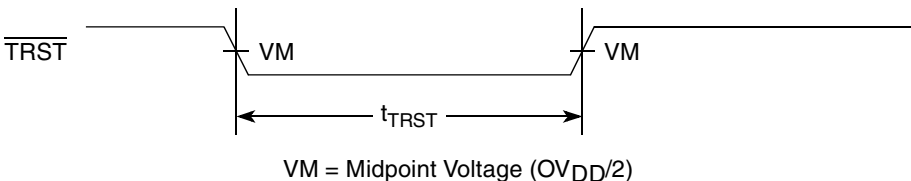


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

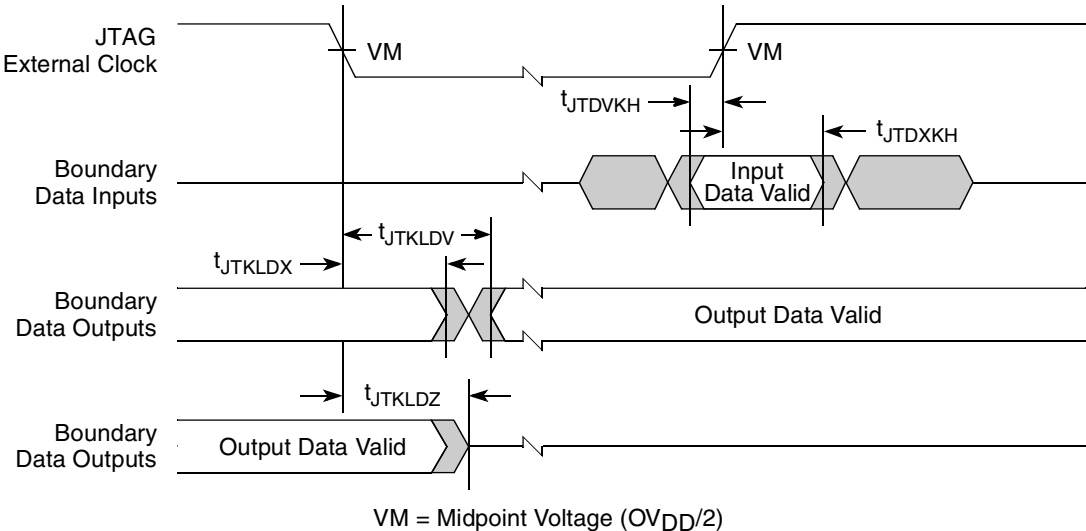


Figure 35. Boundary-Scan Timing Diagram

12.2 I²C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I²C interface of the MPC8555E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} ⁶	1.3	—	μs
High period of the SCL clock	t_{I2CH} ⁶	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} ⁶	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} ⁶	0.6	—	μs
Data setup time	t_{I2DVKH} ⁶	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1 C_b$ ⁴	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1 C_b$ ⁴	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8555E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_b = capacitance of one bus line in pF.
- Guaranteed by design.

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_GNT[1:4]	AD18, AE18, AE19, AD19	O	OV _{DD}	5, 9
PCI2_IDSEL	AC22	I	OV _{DD}	—
PCI2_IRDY	AD20	I/O	OV _{DD}	2
PCI2_PERR	AC20	I/O	OV _{DD}	2
PCI2_REQ[0]	AD21	I/O	OV _{DD}	—
PCI2_REQ[1:4]	AE21, AD22, AE22, AC23	I	OV _{DD}	—
PCI2_SERR	AE20	I/O	OV _{DD}	2,4
PCI2_STOP	AC21	I/O	OV _{DD}	2
PCI2_TRDY	AC19	I/O	OV _{DD}	2
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV _{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV _{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV _{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV _{DD}	—
MBA[0:1]	B18, B19	O	GV _{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV _{DD}	—
MWE	D17	O	GV _{DD}	—
MRAS	F17	O	GV _{DD}	—
MCAS	J16	O	GV _{DD}	—
MCS[0:3]	H16, G16, J15, H15	O	GV _{DD}	—
MCKE[0:1]	E26, E28	O	GV _{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV _{DD}	—
MCK[0:5]	F20, G27, B15, E20, F27, L14	O	GV _{DD}	—
MSYNC_IN	M28	I	GV _{DD}	22
MSYNC_OUT	N28	O	GV _{DD}	22
Local Bus Controller Interface				
LA[27]	U18	O	OV _{DD}	5, 9

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/O	OV _{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/O	OV _{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/O	OV _{DD}	—

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
3. TEST_SEL0 must be pulled-high, TEST_SEL1 must be tied to ground.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8555E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCCLK PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See [Section 15.2, “Platform/System PLL Ratio.”](#)
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See the [Section 15.3, “e500 Core PLL Ratio.”](#)
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 k Ω) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2_C_BE}}$ [7:4]).
18. If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
19. Recommend a pull-up resistor (~1 k Ω) be placed on this pin to OV_{DD}.
20. These are test signals for factory use only and must be pulled up (100 Ω to 1k Ω) to OV_{DD} for normal machine operation.
21. If this signal is used as both an input and an output, a weak pull-up (~10k Ω) is required on this pin.
22. MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

15 Clocking

This section describes the PLL configuration of the MPC8555E. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

[Table 44](#) provides the clocking specifications for the processor core and [Table 44](#) provides the clocking specifications for the memory bus.

Table 44. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency										Unit	Notes
	533 MHz		600 MHz		667 MHz		833 MHz		1000 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	533	400	600	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

Table 45. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	533, 600, 667, 883, 1000 MHz			
	Min	Max		
Memory bus frequency	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

16 Thermal

This section describes the thermal specifications of the MPC8555E.

16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8555E.

Table 49. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	$R_{\theta JC}$	0.96	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51–6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 43. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

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16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device. See [Table 4](#) and [Table 5](#).

During operation the die-junction temperatures (T_J) should be maintained within the range specified in [Table 2](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. For the purposes of this example, the θ_{JC} value given in [Table 49](#) that includes the thermal grease interface and is documented in note 4 is used. If a thermal pad is used, θ_{INT} must be added.

Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package $\theta_{JC} = 0.96$, and a power consumption (P_D) of 8.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + \theta_{SA}) \times 8.0 \text{ W}$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in [Figure 47](#).

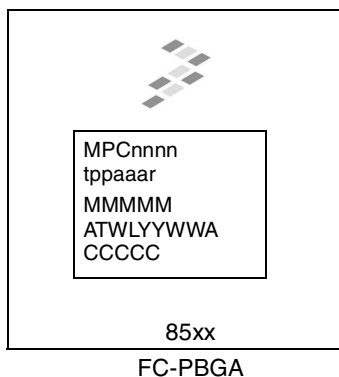
Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

$$T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + 3.3^\circ\text{C/W}) \times 8.0 \text{ W},$$

resulting in a die-junction temperature of approximately 69°C which is well within the maximum operating temperature of the component.

19.2 Part Marking

Parts are marked as the example shown in [Figure 54](#).



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device