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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8555ecpxajd

Figure 6 provides the AC test load for the DDR bus.

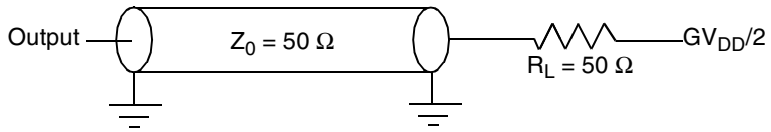


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8555E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8555E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

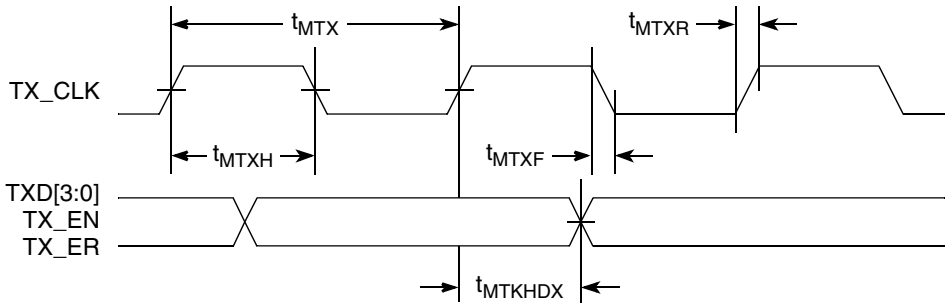


Figure 10. MII Transmit AC Timing Diagram

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKHOZ2}$	—	2.8	ns	5, 9
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			4.2		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHKT}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	–1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	–0.8	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV1}$	—	0.5	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV2}$	—	0.7	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.2		

Figure 17 to Figure 22 show the local bus signals.

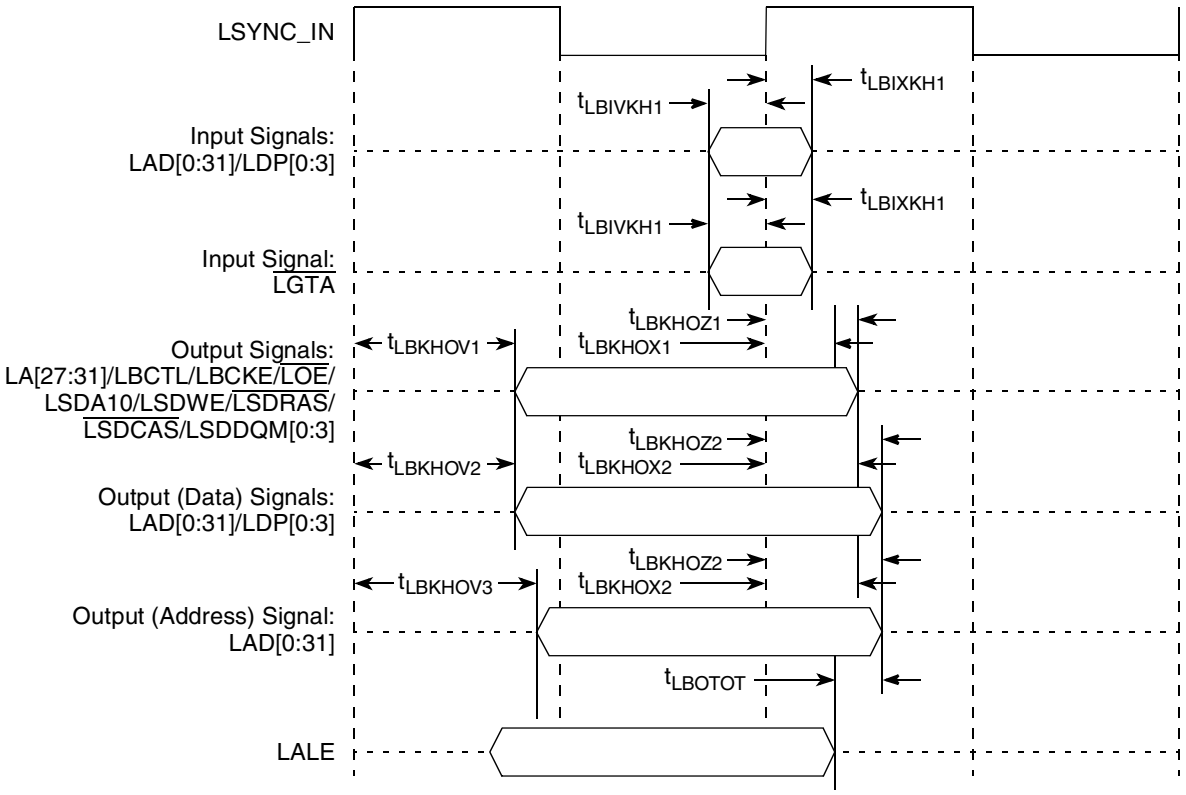


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

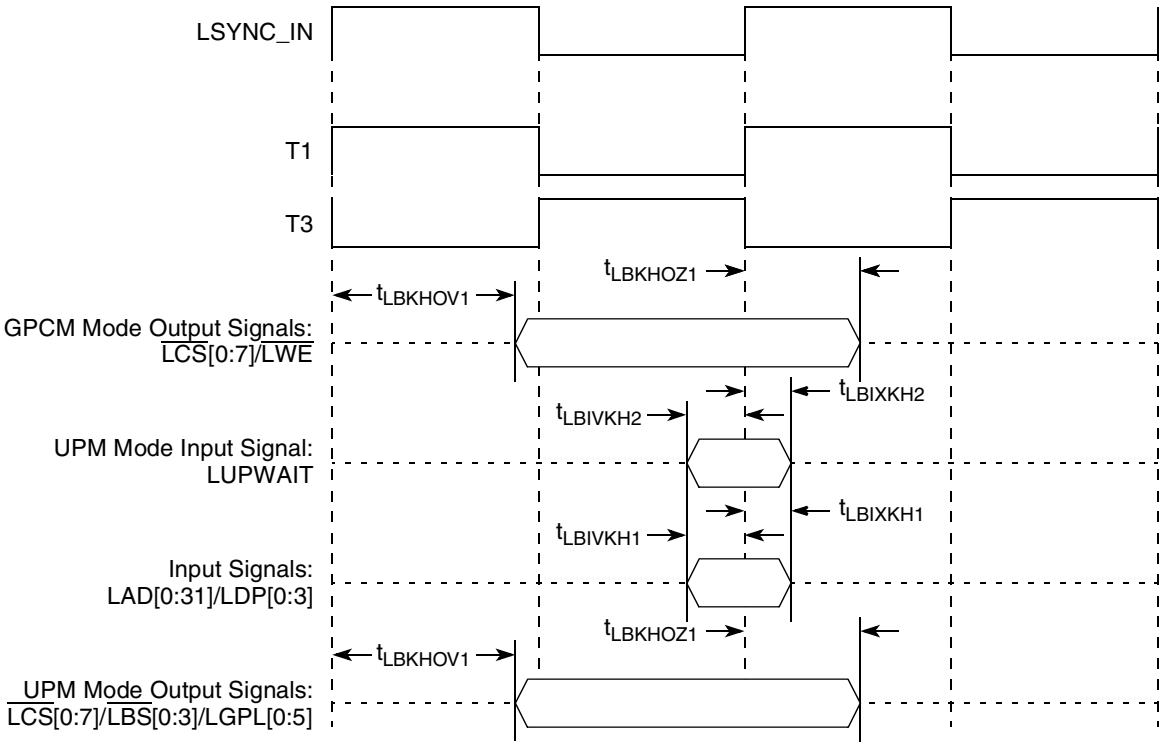


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

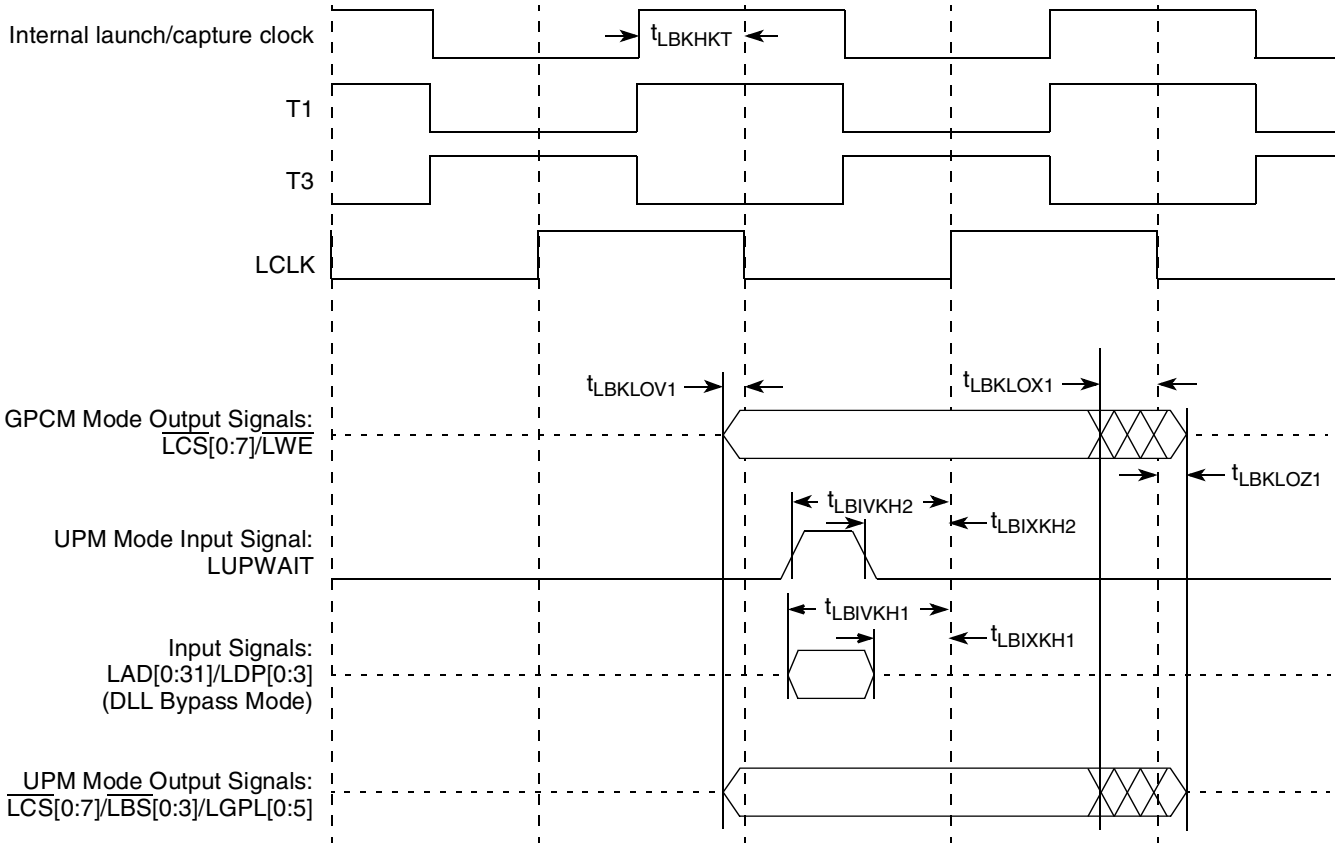
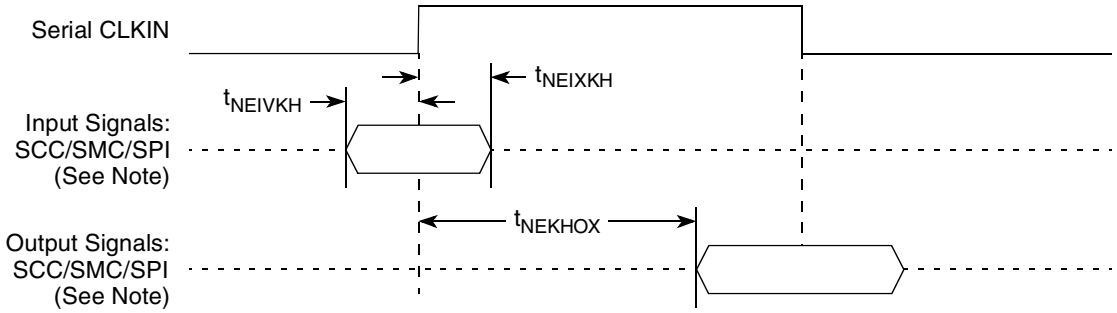


Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

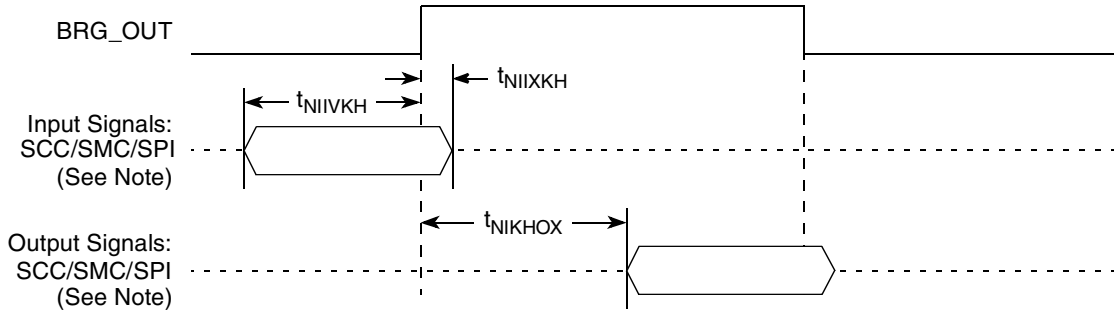
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

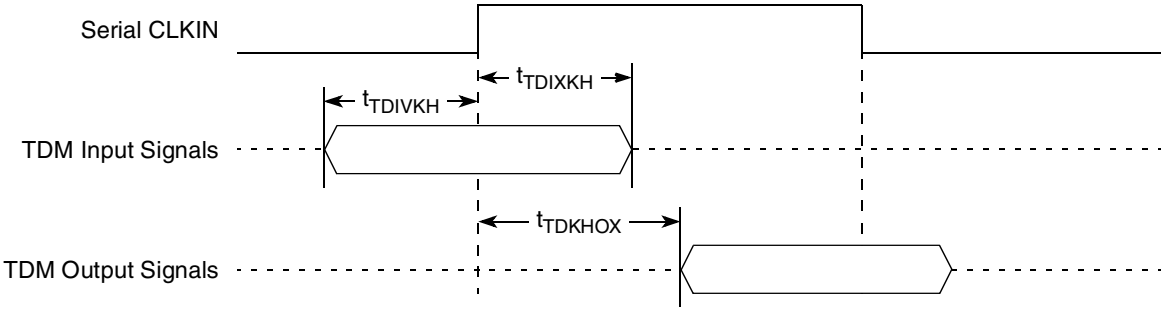
Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

[1] SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

[2] SPI AC timings refer always to SPICLK.

Figure 29 shows TDM input and output signals.



Note: There are 4 possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 29. TDM Signal AC Timing Diagram

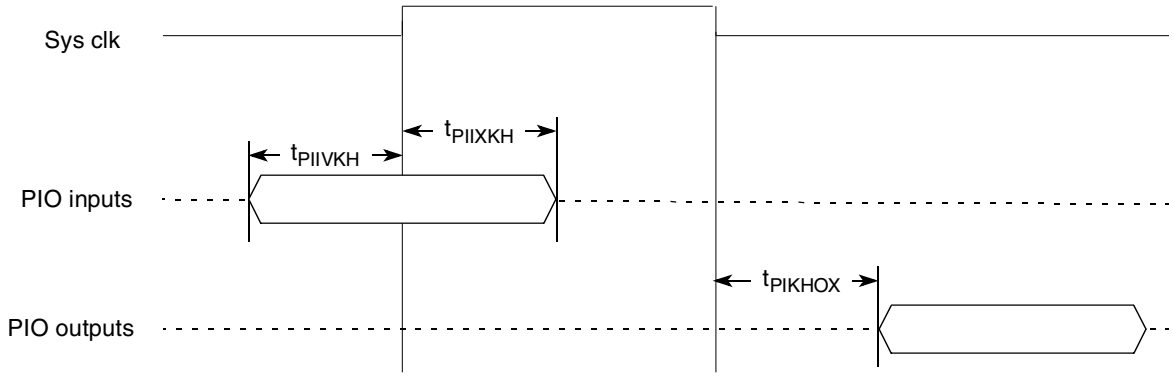


Figure 30. PIO Signal Diagram

10.3 CPM I2C AC Specification

Table 35. I2C Timing

Characteristic	Expression	All Frequencies		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX} (1)	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	-	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	-	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	-	s
Start condition setup time[2]	t_{SCHDL}	2/(divider * f_{SCL})	- (2)	s
Start condition hold time[2]	t_{SDLCL}	3/(divider * f_{SCL})	-	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	-	s
Data setup time[2]	t_{SDVCH}	3/(divider * f_{SCL})	-	s
SDA/SCL rise time	t_{SRISE}	-	1/(10 * f_{SCL})	s

Figure 32 provides the AC test load for TDO and the boundary-scan outputs of the MPC8555E.

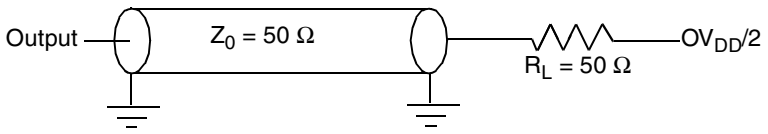


Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

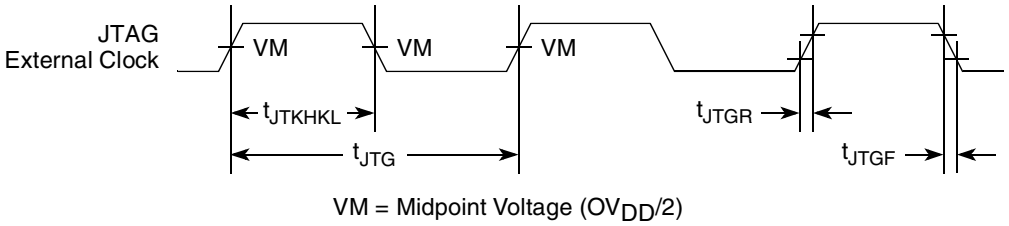


Figure 33. JTAG Clock Input Timing Diagram

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

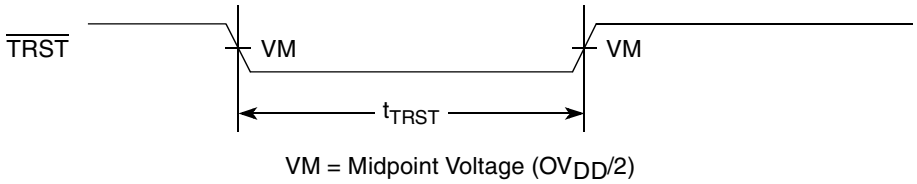


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

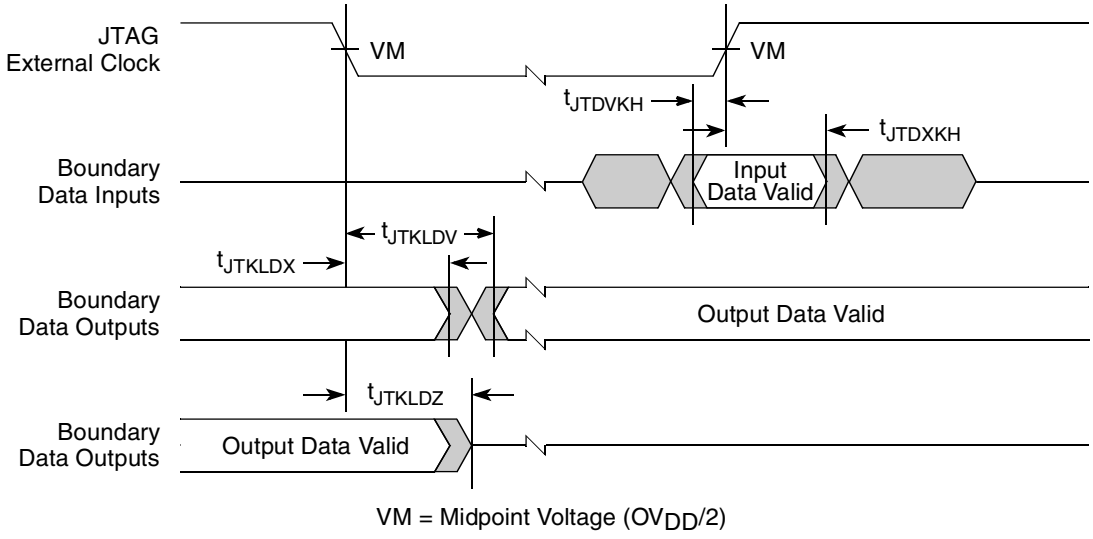


Figure 35. Boundary-Scan Timing Diagram

12.2 I^2C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I^2C interface of the MPC8555E.

Table 40. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [6]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [6]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [6]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [6]	0.6	—	μs
Data setup time	t_{I2DVKH} [6]	100	—	ns
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8555E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design.

Figure 16 provides the AC test load for the I^2C.

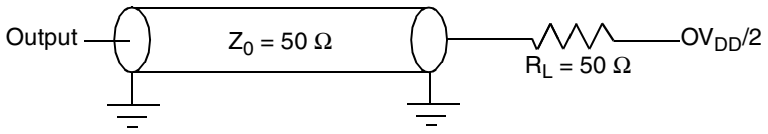


Figure 37. I^2C AC Test Load

Figure 38 shows the AC timing diagram for the I^2C bus.

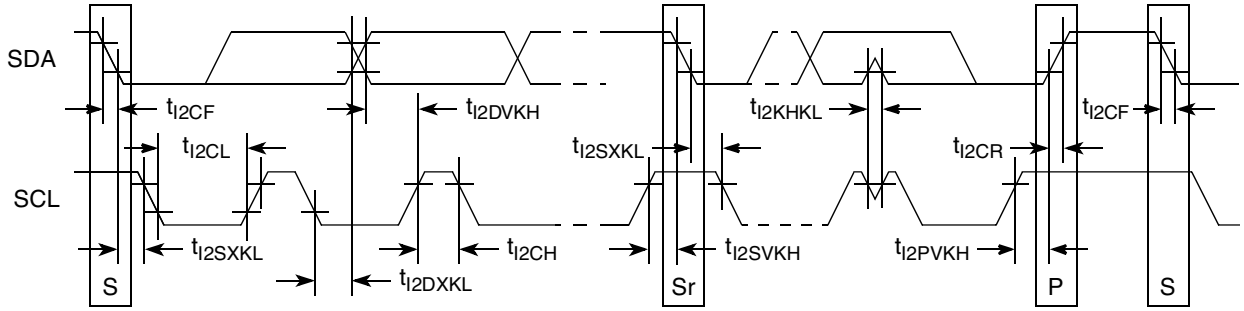


Figure 38. I^2C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8555E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8555E.

Table 41. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$	—	±5	µA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8555E, 783 FC-PBGA package.

Table 43. MPC8555E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32], PCI2_AD[31:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
$\overline{\text{PCI_C_BE64}}$[7:4] $\overline{\text{PCI2_C_BE}}$[3:0]	AG13, AH13, V14, W14	I/O	OV_{DD}	17
$\overline{\text{PCI_C_BE64}}$[3:0] $\overline{\text{PCI1_C_BE}}$[3:0]	AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI1_PAR	AA11	I/O	OV_{DD}	—
PCI1_PAR64/PCI2_PAR	Y14	I/O	OV_{DD}	—
$\overline{\text{PCI1_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI1_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI1_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI1_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI1_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI1_IDSEL	AA9	I	OV_{DD}	—
$\overline{\text{PCI1_REQ64}}$/$\overline{\text{PCI2_FRAME}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI1_ACK64}}$/$\overline{\text{PCI2_DEVSEL}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI1_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI1_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1_REQ}}$[0]	AF5	I/O	OV_{DD}	—
$\overline{\text{PCI1_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
$\overline{\text{PCI1_GNT}}$[0]	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI1_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9
PCI1_CLK	AH25	I	OV_{DD}	—
PCI2_CLK	AH27	I	OV_{DD}	—
$\overline{\text{PCI2_GNT}}$[0]	AC18	I/O	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_CRS	D9	I	LV_{DD}	—
TSEC2_COL	F8	I	LV_{DD}	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	—
TSEC2_RX_DV	H8	I	LV_{DD}	—
TSEC2_RX_ER	A8	I	LV_{DD}	—
TSEC2_RX_CLK	E10	I	LV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0,1]	Y2, Y3	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0,1]	Y1, AD1	O	OV_{DD}	—
UART_SIN[0,1]	P11, AD5	I	OV_{DD}	—
UART_SOUT[0,1]	N6, AD2	O	OV_{DD}	—
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 19
IIC_SCL	AH23	I/O	OV_{DD}	4, 19
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	18
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	—
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 18
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:3]	F3, F5	O	OV_{DD}	6
MSRCID4	F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	—
RTC	AB23	I	OV_{DD}	—
CLK_OUT	AF22	O	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	—
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—

15 Clocking

This section describes the PLL configuration of the MPC8555E. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 44 provides the clocking specifications for the processor core and Table 44 provides the clocking specifications for the memory bus.

Table 44. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency										Unit	Notes
	533 MHz		600 MHz		667 MHz		833 MHz		1000 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	533	400	600	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

Table 45. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	533, 600, 667, 883, 1000 MHz			
	Min	Max		
Memory bus frequency	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

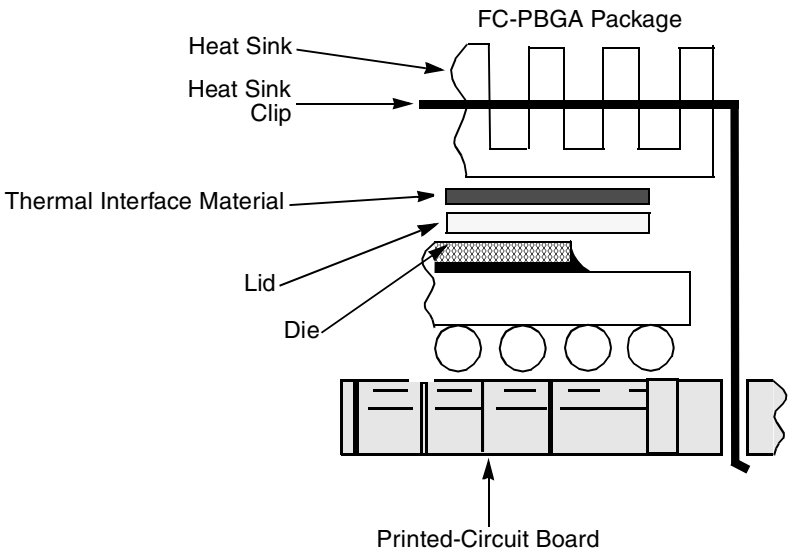


Figure 43. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8555E. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device. See Table 4 and Table 5.

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. For the purposes of this example, the θ_{JC} value given in Table 49 that includes the thermal grease interface and is documented in note 4 is used. If a thermal pad is used, θ_{INT} must be added.

Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package θ_{JC} = 0.96, and a power consumption (P_D) of 8.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.96°C/W + \theta_{SA}) \times 8.0\ W$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 47.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

$$T_J = 30°C + 5°C + (0.96°C/W + 3.3°C/W) \times 8.0\ W,$$

resulting in a die-junction temperature of approximately 69°C which is well within the maximum operating temperature of the component.

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 48 and provide exploded views of the plastic fence, heat sink, and spring clip.

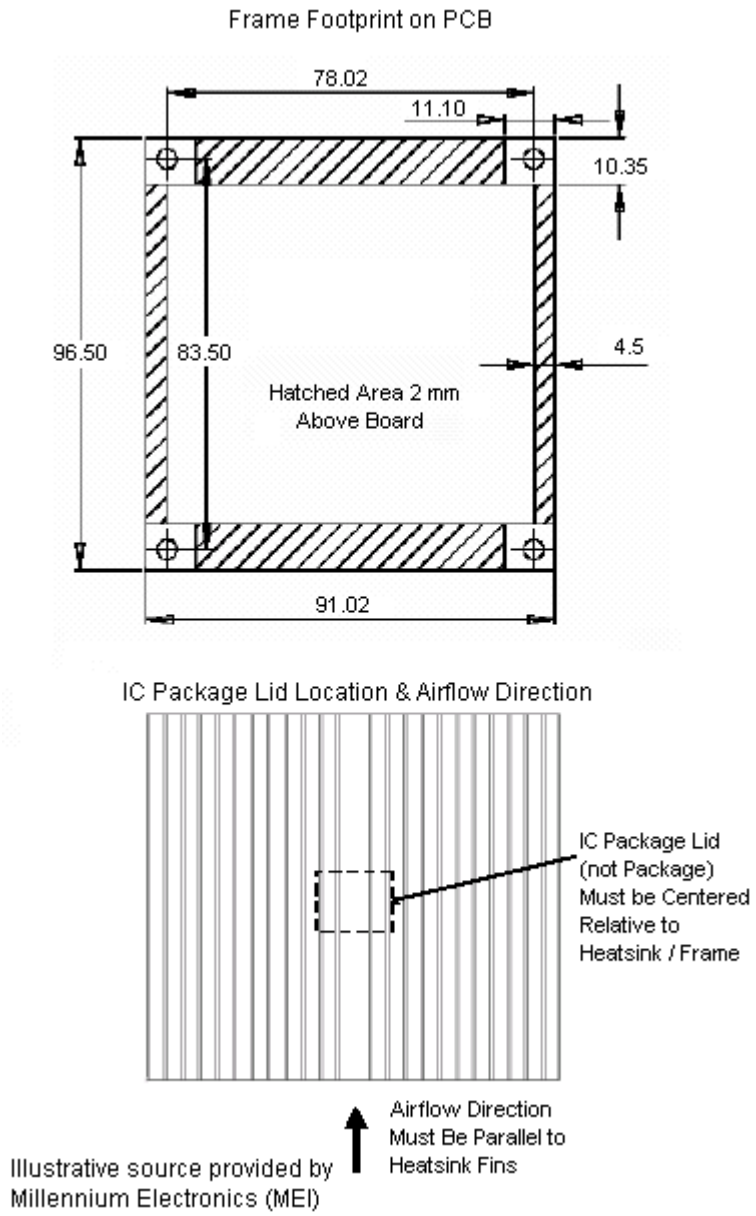
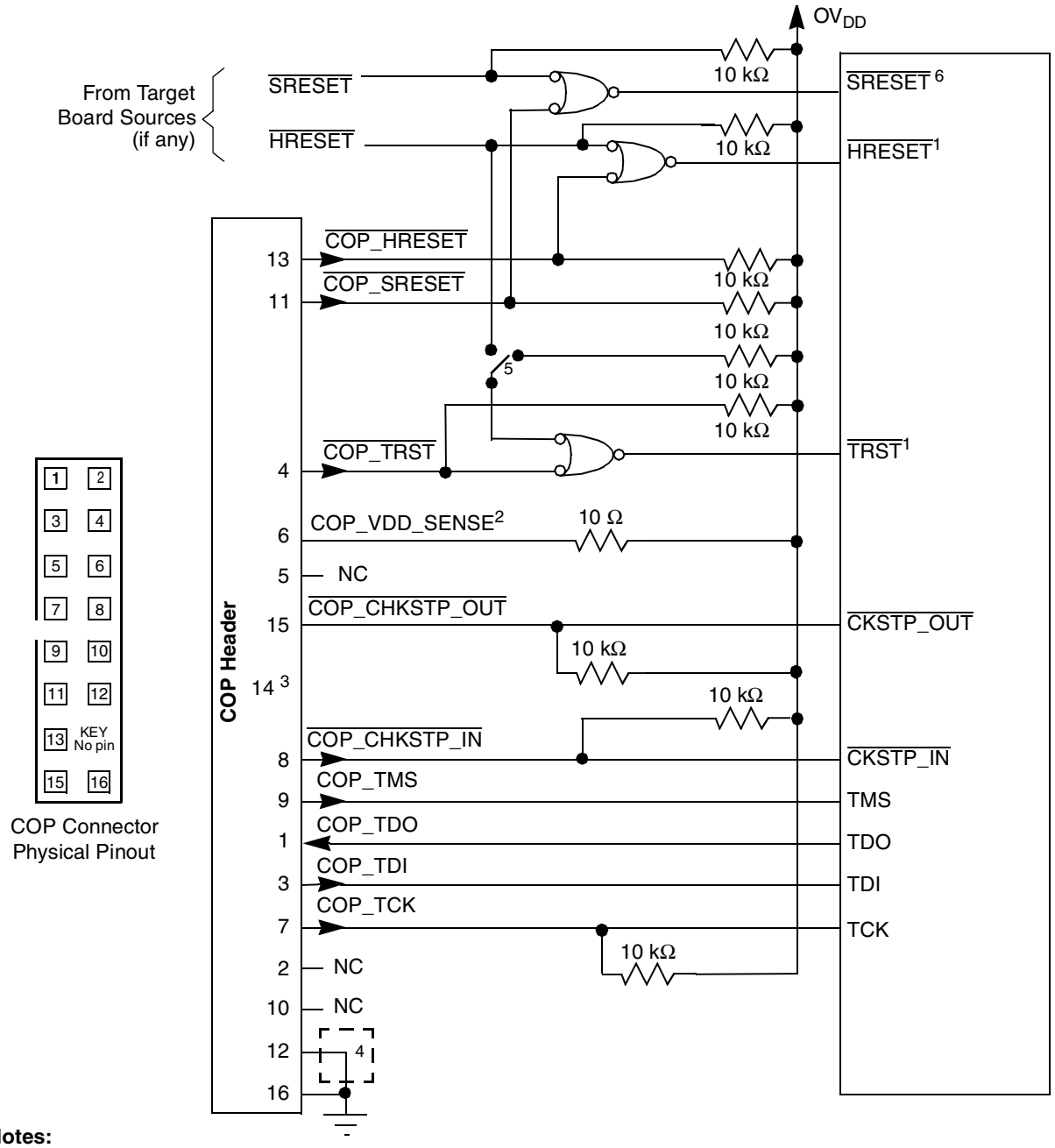


Figure 48. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	7/2007	Inserted Figure 3, ““Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Added footnote 2 about junction temperature in Table 4. Added max. power values for 1000 MHz core frequency in Table 4. Removed Figure 3, “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30. Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values inTable 30. Added note 3 to $t_{LBKHOV1}$ in Table 30. Modified note 3 in Table 30 and Table 31. Added note 3 to $t_{LBKLOV1}$ in Table 31. Modified values for t_{LBKHKT}, $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31. Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21. Modified note for signal CLK_OUT in Table 43. PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43. Added column for Encryption Acceleration in Table 52.
3	8/2005	Modified max. power values in Table 4. Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43.
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31. Added note 2 in Table 7. Modified min and max values for t_{DDKHMP} in Table 14.
1	6/2005	Changed LV_{dd} to OV_{dd} for the supply voltage Ethernet management interface in Table 27. Modified footnote 4 and changed typical power for the 1000 MHz core frequency inTable 4. Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31.
0	6/2005	Initial release.