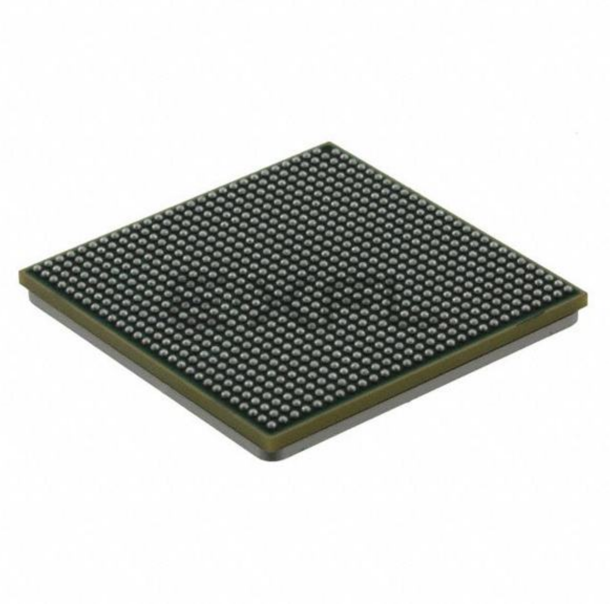

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555ecpxalf

  - 10 Mbps IEEE 802.3 MII
  - 1000 Mbps IEEE 802.3z TBI
  - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking

- OCeaN switch fabric
  - Three-port crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no-snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI Controllers
  - PCI 2.2 compatible
  - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
  - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8555E.

Table 6. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ±1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8555E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise time	t_{G125R}	—	—	1.0	ns	1
EC_GTX_CLK125 fall time	t_{G125F}	—	—	1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

Table 8. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	2 x t_{CCB_CLK}	—	—	ns	—
RTC clock low time	t_{RTCL}	2 x t_{CCB_CLK}	—	—	ns	—

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8555E. Table 9 provides the RESET initialization AC timing specifications.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before HRESET negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8555E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the SYSCLK × platform PLL ratio.

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration [3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall times	t_{RGTR} [6,7], t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 and 2.0 V voltage levels.

Figure 15 shows the MII management AC timing diagram.

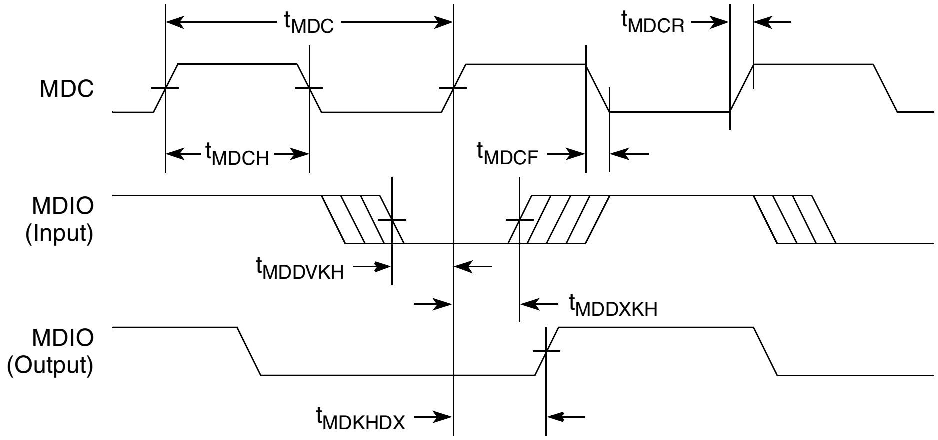

Figure 15. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8555E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –2mA	OV_{DD} –0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 2mA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to address valid for LAD	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOV3}$	—	0.8	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.3		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOX1}$	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		–1.8			
Output hold from local bus clock for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOX2}$	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1]$ = 11 (default)		–1.8			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOZ1}$	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.4		
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1]$ = 00	$t_{LBKLOZ2}$	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1]$ = 11 (default)			2.4		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.

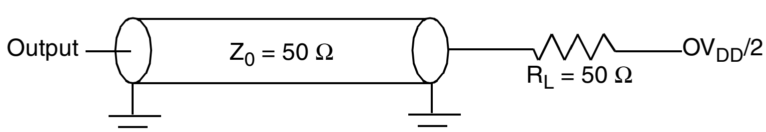

Figure 16. Local Bus C Test Load

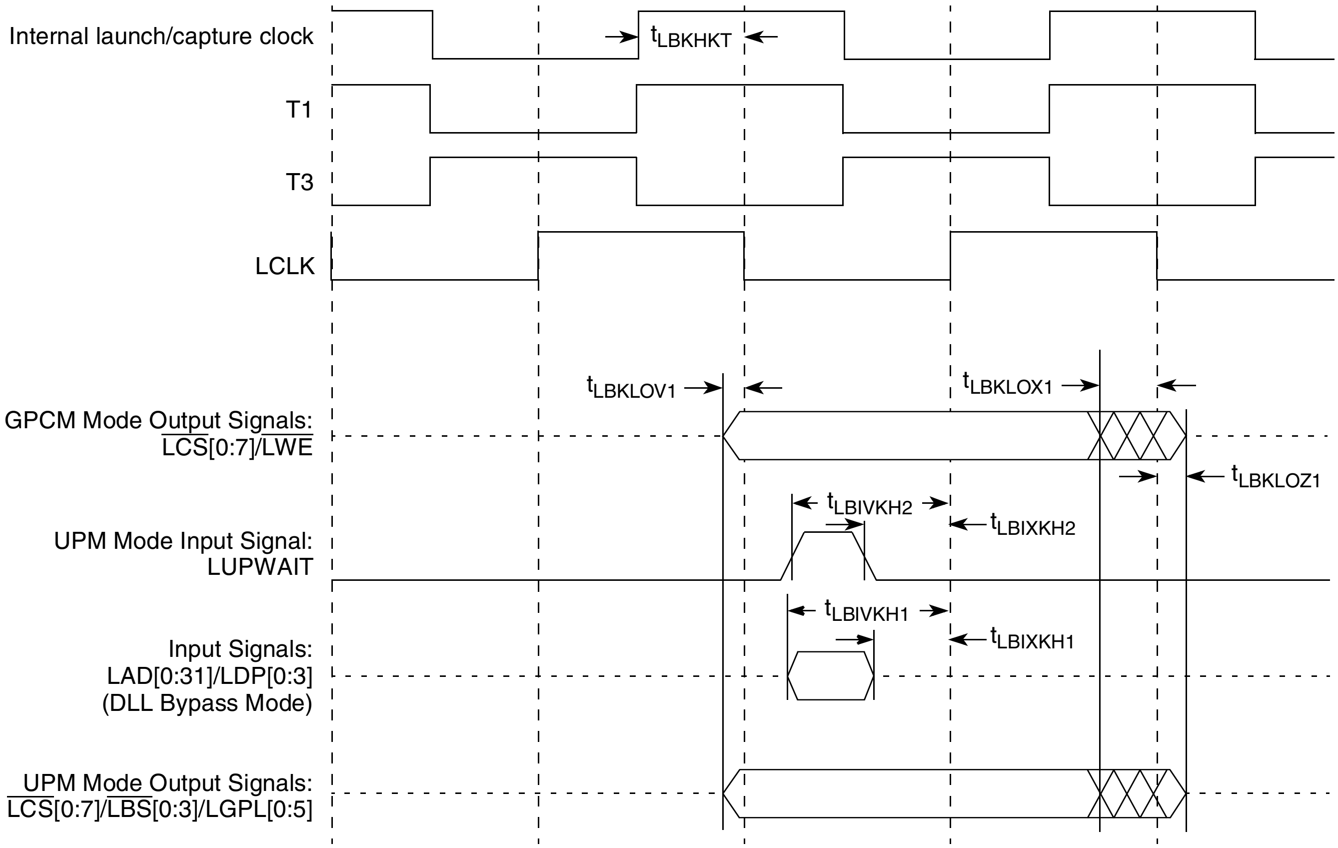

Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8555E.

10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

Table 32. CPM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	3.465	V	1
Input low voltage	V_{IL}		GND	0.8	V	1, 2
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	1
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1

Note:
1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. V_{IL}(max) for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 33. CPM Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min[3]	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	6	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	$t_{FEIXKH}b$	2	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	6	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SMC/SPI inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SMC/SPI inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	4	ns

Table 33. CPM Input AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min[3]	Unit
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns
PIO inputs—input setup time	t_{PIIVKH}	8	ns
PIO inputs—input hold time	t_{PIIXKH}	1	ns
COL width high (FCC)	t_{FCCH}	1.5	CLK

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time. And t_{TDIXKH} symbolizes the TDM timing (TD) with respect to the time the input signals (I) reach the invalid state (X) relative to the reference clock t_{FCC} (K) going to the high (H) state or hold time.
3. PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Table 34. CPM Output AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t_{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t_{FEKHOX}	2	8	ns
SCC/SMC/SPI outputs—internal clock (NMSI) delay	t_{NIKHOX}	0.5	10	ns
SCC/SMC/SPI outputs—external clock (NMSI) delay	t_{NEKHOX}	2	8	ns
TDM outputs/SI delay	t_{TDKHOX}	2.5	11	ns
PIO outputs delay	t_{PIKHOX}	1	11	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the CPM.

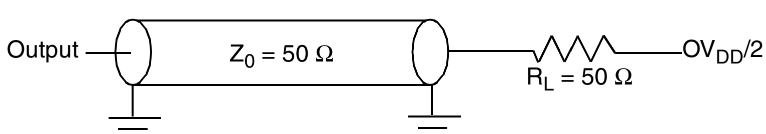

Figure 23. CPM AC Test Load

12.2 I²C AC Electrical Specifications

Table 40 provides the AC timing parameters for the I^2C interface of the MPC8555E.

Table 40. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 39).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [6]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [6]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [6]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [6]	0.6	—	μs
Data setup time	t_{I2DVKH} [6]	100	—	ns
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$ [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8555E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design.

Figure 40 shows the PCI input AC timing conditions.

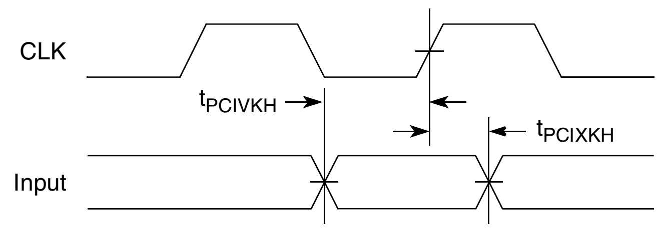

Figure 40. PCI Input AC Timing Measurement Conditions

Figure 41 shows the PCI output AC timing conditions.

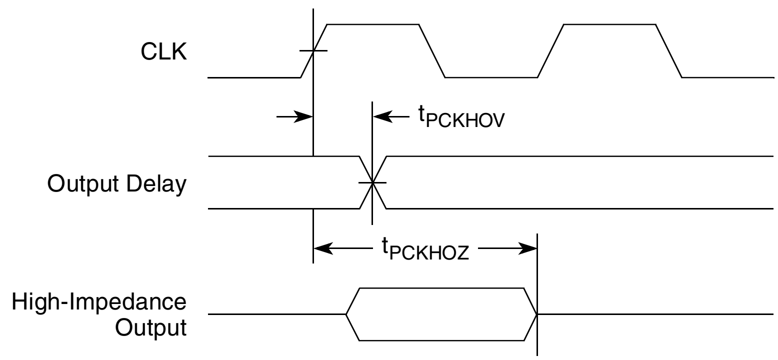

Figure 41. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8555E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8555E, 783 FC-PBGA package.

Table 43. MPC8555E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32], PCI2_AD[31:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	I/O	OV_{DD}	17
PCI1_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_BE64[7:4] PCI2_C_BE[3:0]	AG13, AH13, V14, W14	I/O	OV_{DD}	17
PCI_C_BE64[3:0] PCI1_C_BE[3:0]	AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI1_PAR	AA11	I/O	OV_{DD}	—
PCI1_PAR64/PCI2_PAR	Y14	I/O	OV_{DD}	—
PCI1_FRAME	AC10	I/O	OV_{DD}	2
PCI1_TRDY	AG10	I/O	OV_{DD}	2
PCI1_IRDY	AD10	I/O	OV_{DD}	2
PCI1_STOP	V11	I/O	OV_{DD}	2
PCI1_DEVSEL	AH10	I/O	OV_{DD}	2
PCI1_IDSEL	AA9	I	OV_{DD}	—
PCI1_REQ64/PCI2_FRAME	AE13	I/O	OV_{DD}	5, 10
PCI1_ACK64/PCI2_DEVSEL	AD13	I/O	OV_{DD}	2
PCI1_PERR	W11	I/O	OV_{DD}	2
PCI1_SERR	Y11	I/O	OV_{DD}	2, 4
PCI1_REQ[0]	AF5	I/O	OV_{DD}	—
PCI1_REQ[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
PCI1_GNT[0]	AE6	I/O	OV_{DD}	—
PCI1_GNT[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9
PCI1_CLK	AH25	I	OV_{DD}	—
PCI2_CLK	AH27	I	OV_{DD}	—
PCI2_GNT[0]	AC18	I/O	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	—
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/O	OV_{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/O	OV_{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/O	OV_{DD}	—

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA\_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
3. TEST_SEL0 must be pulled-high, TEST_SEL1 must be tied to ground.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8555E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 15.2, "Platform/System PLL Ratio."
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 15.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2\_C\_BE}}$[7:4]).
18. If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
19. Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OV_{DD}.
20. These are test signals for factory use only and must be pulled up (100Ω to 1kΩ) to OV_{DD} for normal machine operation.
21. If this signal is used as both an input and an output, a weak pull-up (~10kΩ) is required on this pin.
22. MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 46.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 46. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8555E to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8555E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid (11 × 11 × 1 mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance (8.7 × 9.3 × 0.05 mm)		
k_z	1.07	
Die (8.7 × 9.3 × 0.75 mm)		
Bump/Underfill—Collapsed resistance (8.7 × 9.3 × 0.07 mm)		
k_z	4.4	
Substrate and Solder Balls (25 × 25 × 1.6 mm)		
k_x	14.2	
k_y	14.2	
k_z	1.2	

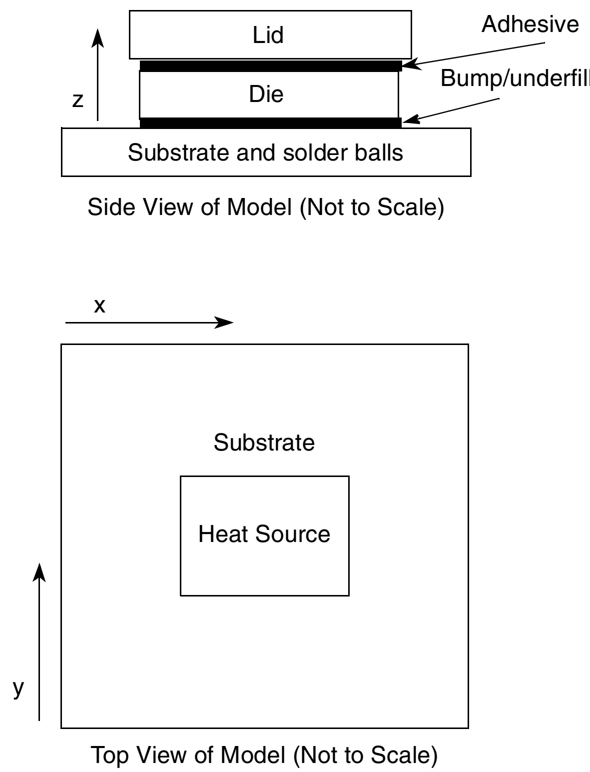

Figure 44. MPC8555E Thermal Model

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 45 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

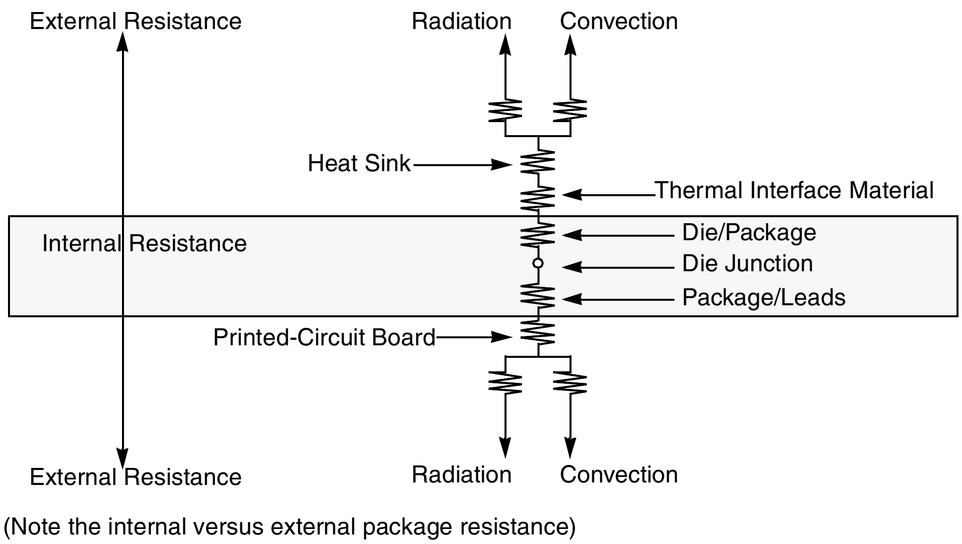

Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 46 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 42). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

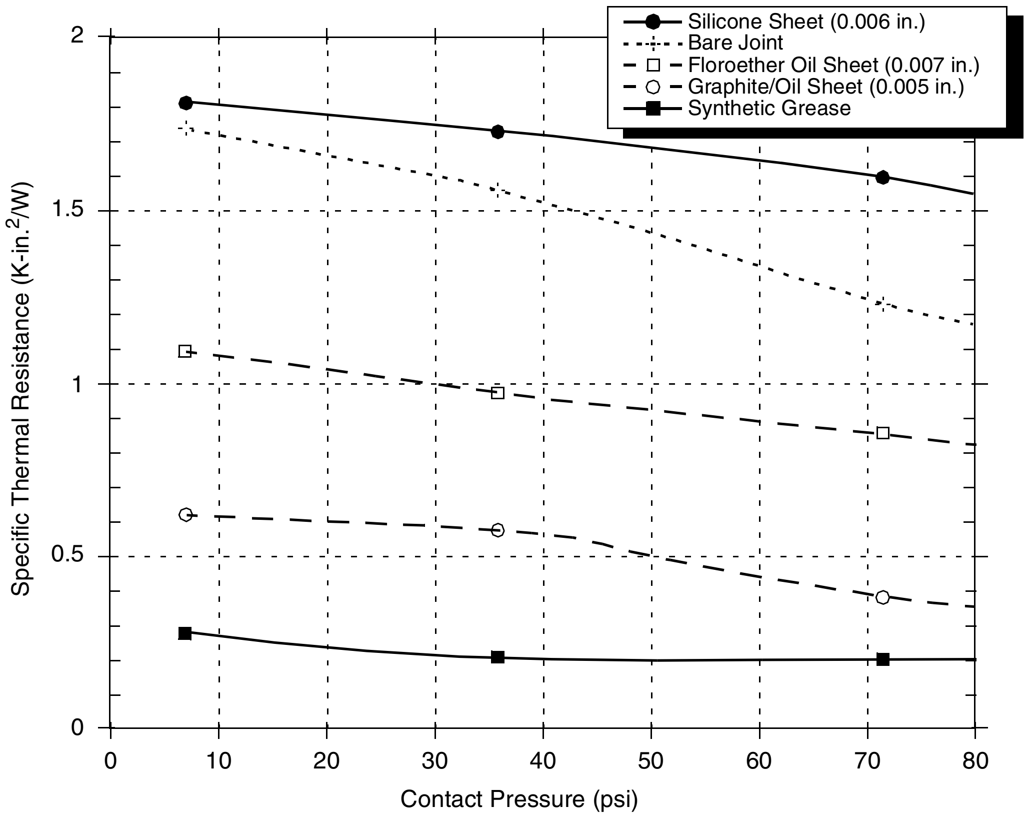

Figure 46. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St.	800-347-4572

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, "Platform/System PLL Ratio."
2. The e500 Core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, "e500 Core PLL Ratio."
3. The CPM PLL ($AV_{DD}3$) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL ($AV_{DD}4$) generates the clocking for the first PCI bus.
5. The PCI2 PLL ($AV_{DD}5$) generates the clock for the second PCI bus.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, and $AV_{DD}5$ respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 50, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

17.6 Configuration Pin Multiplexing

The MPC8555E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8555E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.