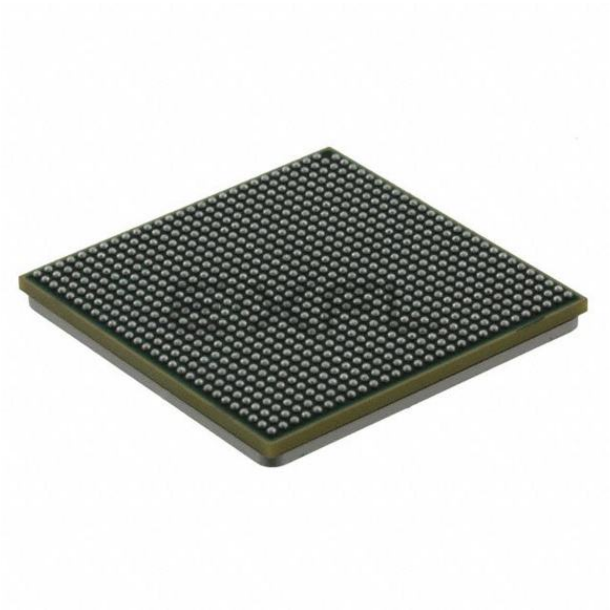


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555ecvtajd

1 Overview

The following section provides a high-level overview of the MPC8555E features. Figure 1 shows the major functional units within the MPC8555E.

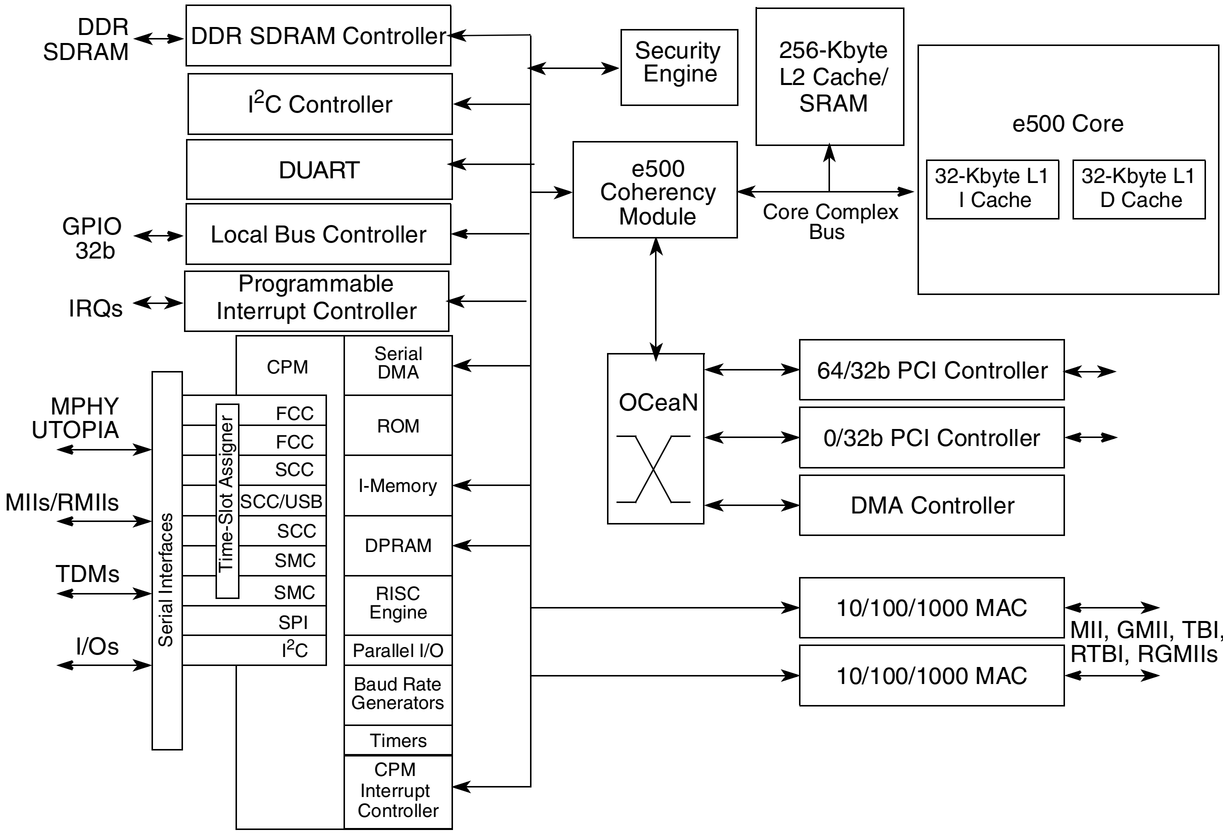


Figure 1. MPC8555E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8555E feature set.

- Embedded e500 Book E-compatible core
  - — High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
  - — Dual-issue superscalar, 7-stage pipeline design
  - — 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
  - — Lockable L1 caches—entire cache or on a per-line basis
  - — Separate locking for instructions and data
  - — Single-precision floating-point operations
  - — Memory management unit especially designed for embedded applications
  - — Enhanced hardware and software debug support
  - — Dynamic power management
  - — Performance monitor facility

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
  - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses

• Address translation and mapping unit (ATMU)
- Eight local access windows define mapping within local 32-bit address space
- Inbound and outbound ATMUs map to larger external address spaces
  - Three inbound windows plus a configuration window on PCI
  - Four inbound windows
  - Four outbound windows plus default translation for PCI

• DDR memory controller
- Programmable timing supporting first generation DDR SDRAM
- 64-bit data interface, up to MHz data rate
- Four banks of memory supported, each up to 1 Gbyte
- DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
- Full ECC support
- Page mode support (up to 16 simultaneous open pages)
- Contiguous or discontiguous memory mapping
- Sleep mode support for self refresh DDR SDRAM
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL2 compatible I/O

• Programmable interrupt controller (PIC)
- Programming model is compliant with the OpenPIC architecture
- Supports 16 programmable interrupt and processor task priority levels
- Supports 12 discrete external interrupts
- Supports 4 message interrupts with 32-bit messages

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8555E may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8555E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V ± 60 mV 1.3 V± 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V ± 60 mV 1.3 V ± 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

3 Power Characteristics

The estimated typical power dissipation for this family of PowerQUICC III devices is shown in Table 4.

Table 4. Power Dissipation(1) (2)

CCB Frequency (MHz)	Core Frequency (MHz)	V_{DD}	Typical Power(3)(4) (W)	Maximum Power(5) (W)
200	400	1.2	4.9	6.6
	500	1.2	5.2	7.0
	600	1.2	5.5	7.3
267	533	1.2	5.4	7.2
	667	1.2	5.9	7.7
	800	1.2	6.3	9.1
333	667	1.2	6.0	7.9
	833	1.2	6.5	9.3
	1000(6)	1.3	9.6	12.8

Notes:

1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 degrees junction temperature is not exceeded on this device.
3. Typical power is based on a nominal voltage of V_{DD} = 1.2V, a nominal process, a junction temperature of T_j = 105° C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions likely need to design to a value higher than Typical Power based on the end application, T_A target, and I/O power
5. Maximum power is based on a nominal voltage of V_{DD} = 1.2V, worst case process, a junction temperature of T_j = 105° C, and an artificial smoke test.
6. The nominal recommended V_{DD} = 1.3V for this speed grade.

Notes:

1.

2.

3.

4.

5.

6.

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8555E.

Table 6. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ±1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8555E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise time	t_{G125R}	—	—	1.0	ns	1
EC_GTX_CLK125 fall time	t_{G125F}	—	—	1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

Figure 4 shows the DDR SDRAM output timing for address skew with respect to any MCK.

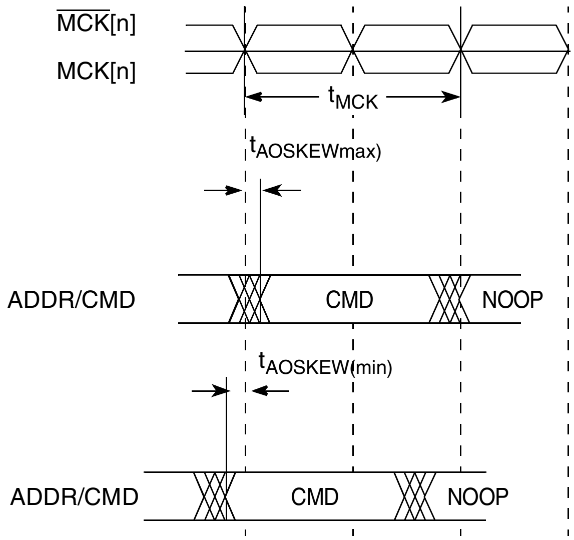


Figure 4. Timing Diagram for t_{AOSKEW} Measurement

Figure 5 shows the DDR SDRAM output timing diagram for the source synchronous mode.

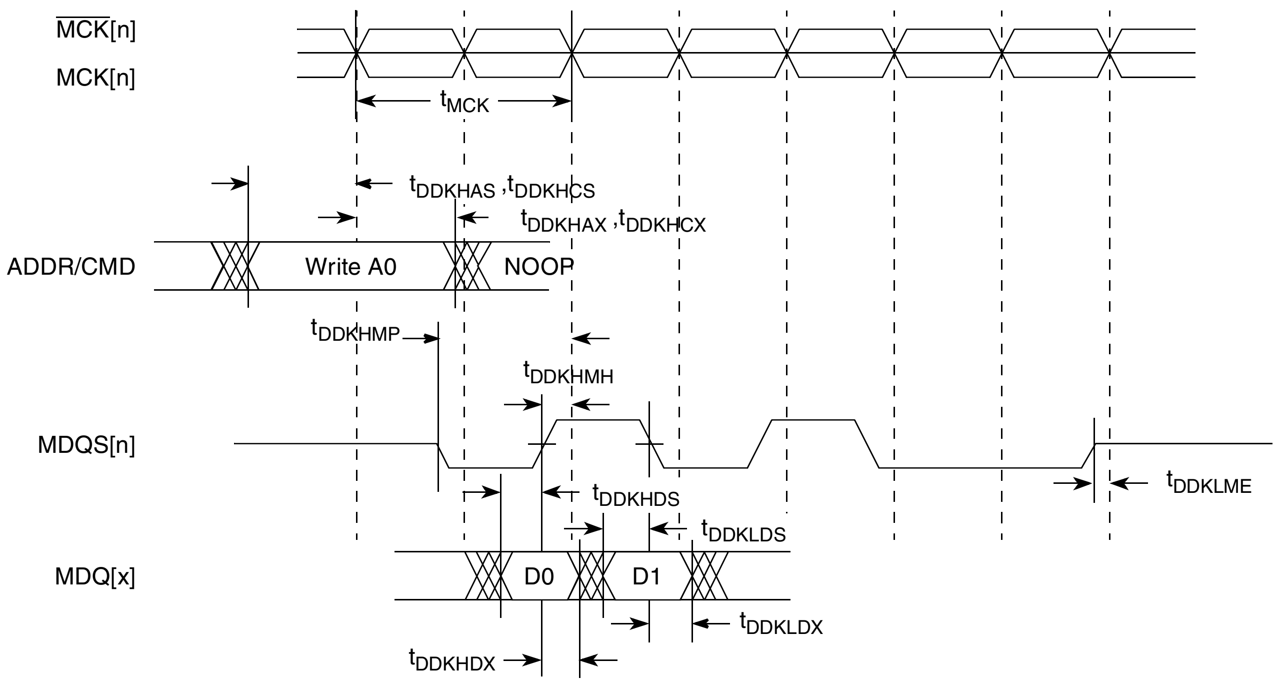


Figure 5. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GMII data TCG[9:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
GMII data TCG[9:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF} [2,3]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

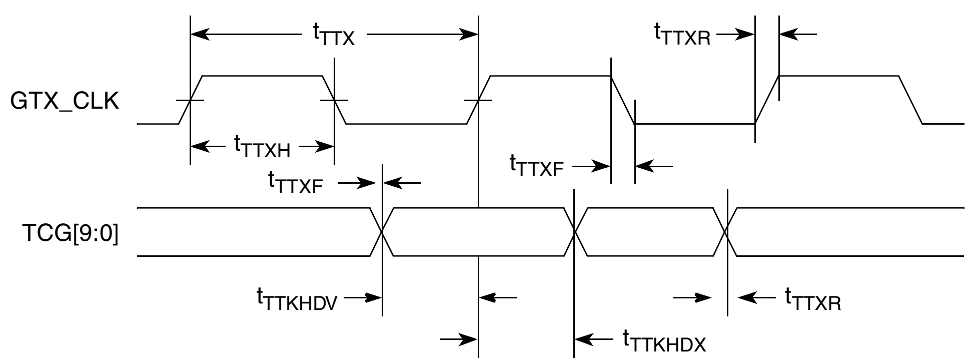


Figure 12. TBI Transmit AC Timing Diagram

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.

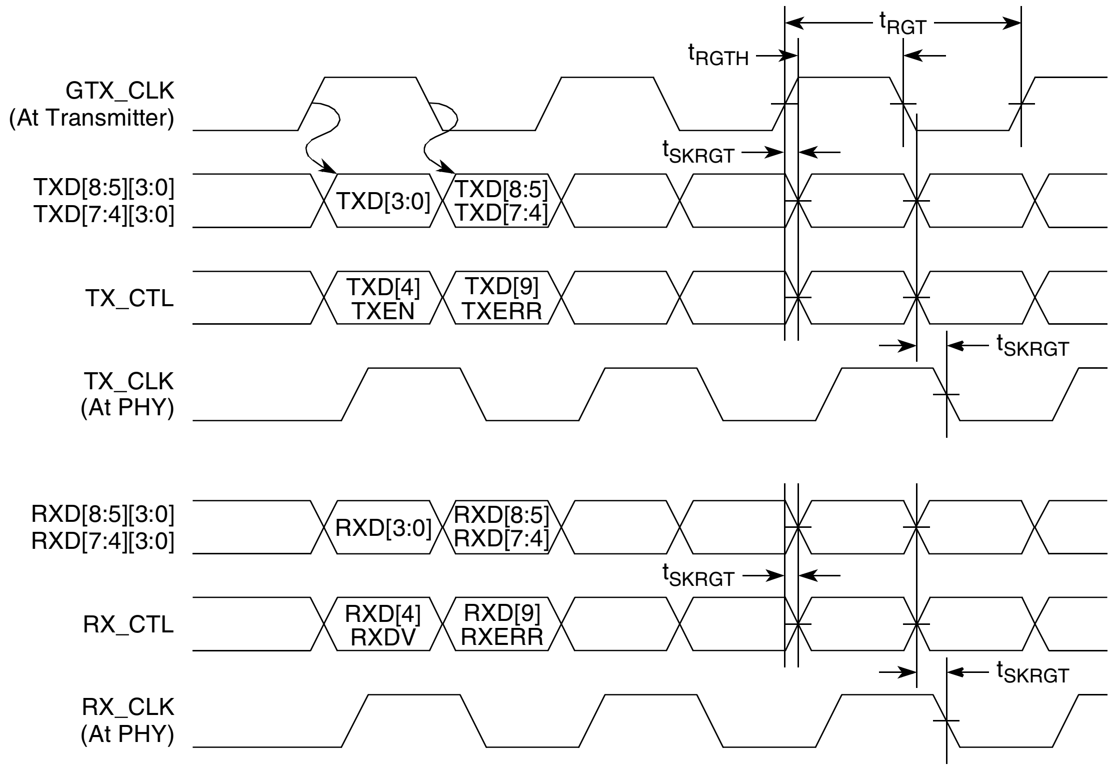


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		1.70	—	V
Input low voltage	V_{IL}	—		—	0.90	V

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKHOZ2}$	—	2.8	ns	5, 9
	$\overline{LWE[0:1]}$ = 11 (default)			4.2		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{LWE[0:1]}$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration [7]	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHKT}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	–1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	–0.8	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE[0:1]}$ = 00	$t_{LBKLOV1}$	—	0.5	ns	3
	$\overline{LWE[0:1]}$ = 11 (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{LWE[0:1]}$ = 00	$t_{LBKLOV2}$	—	0.7	ns	3
	$\overline{LWE[0:1]}$ = 11 (default)			2.2		

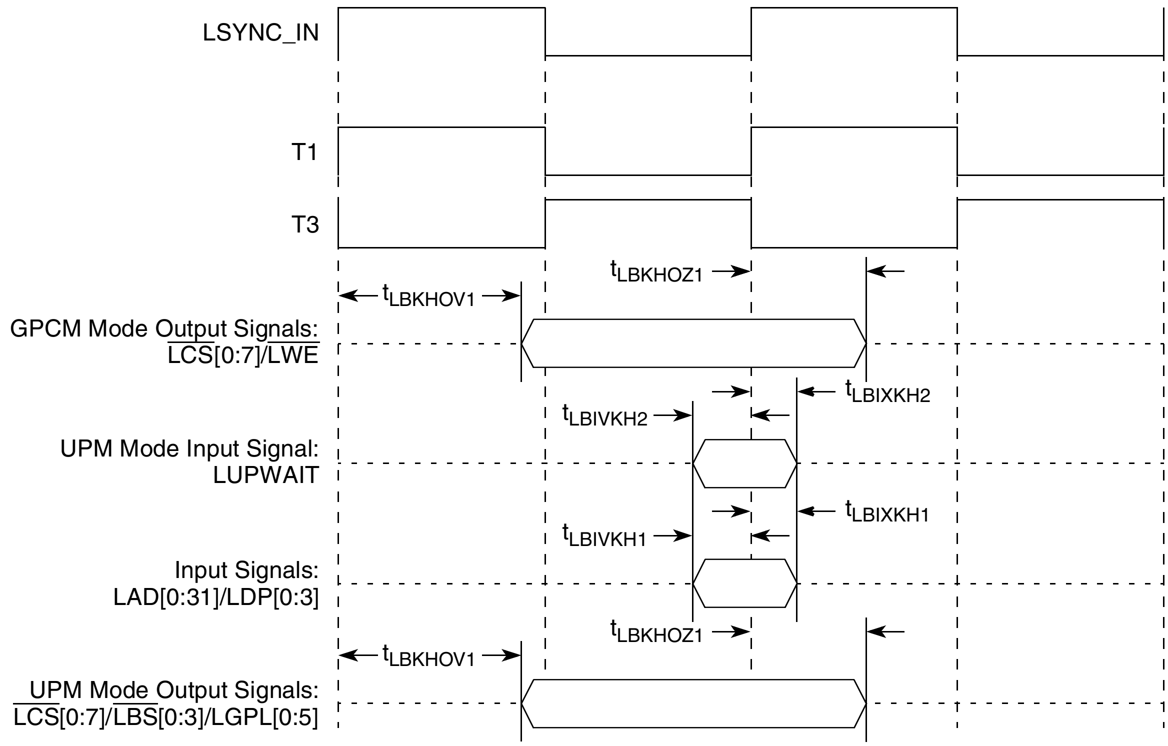


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8555E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data	t_{JTDVKH}	4	—		4
TMS, TDI	t_{JTIVKH}	0	—		
Input hold times:				ns	
Boundary-scan data	t_{JTDXKH}	20	—		4
TMS, TDI	t_{JTIXKH}	25	—		
Valid times:				ns	
Boundary-scan data	t_{JTKLDV}	4	20		5
TDO	t_{JTKLOV}	4	25		
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	—	—		5
TDO	t_{JTKLOX}	—	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	3	19		5, 6
TDO	t_{JTKLOZ}	3	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs of the MPC8555E.

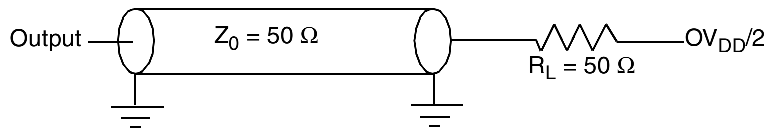


Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

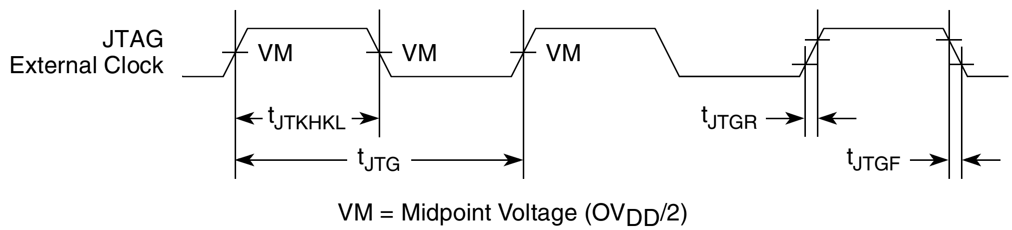


Figure 33. JTAG Clock Input Timing Diagram

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

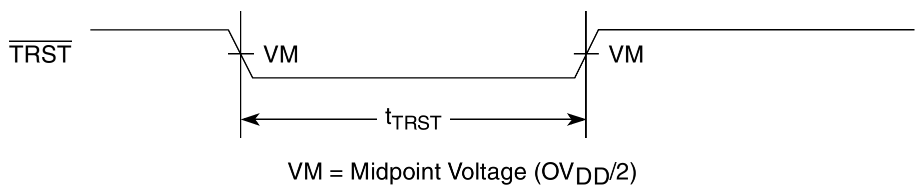


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

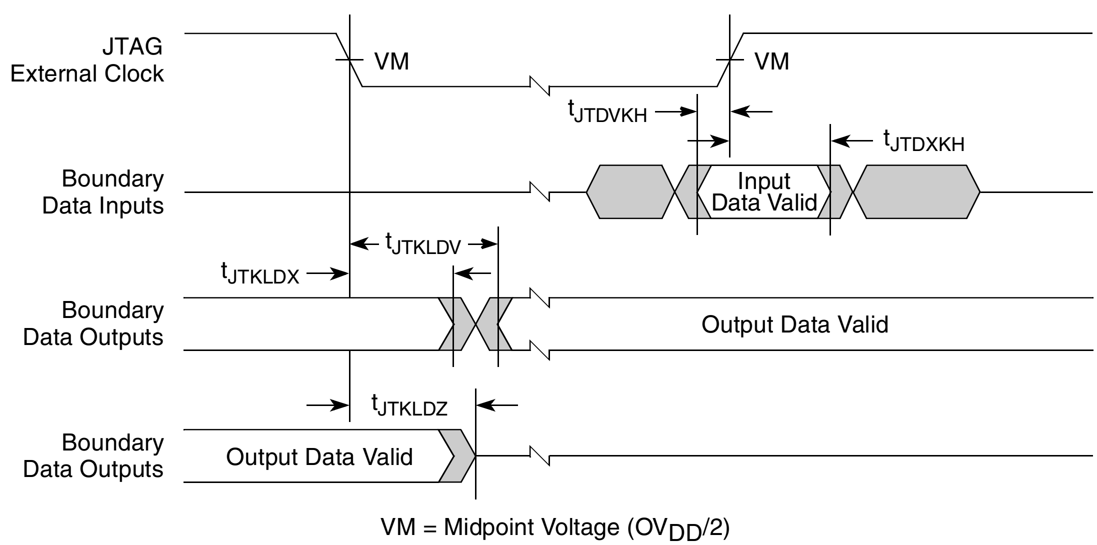


Figure 35. Boundary-Scan Timing Diagram

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:
1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
9. Guaranteed by characterization.
10. Guaranteed by design.

Figure 16 provides the AC test load for PCI.

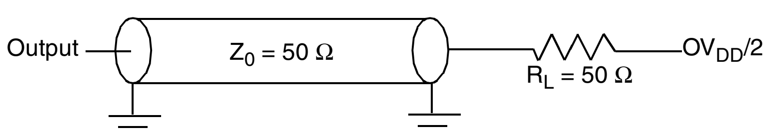


Figure 39. PCI AC Test Load

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	—
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7 AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—

16 Thermal

This section describes the thermal specifications of the MPC8555E.

16.1 Thermal Characteristics

Table 49 provides the package thermal characteristics for the MPC8555E.

Table 49. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@400 ft/min or 2.0 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	$R_{\theta JC}$	0.96	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51–6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 43. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

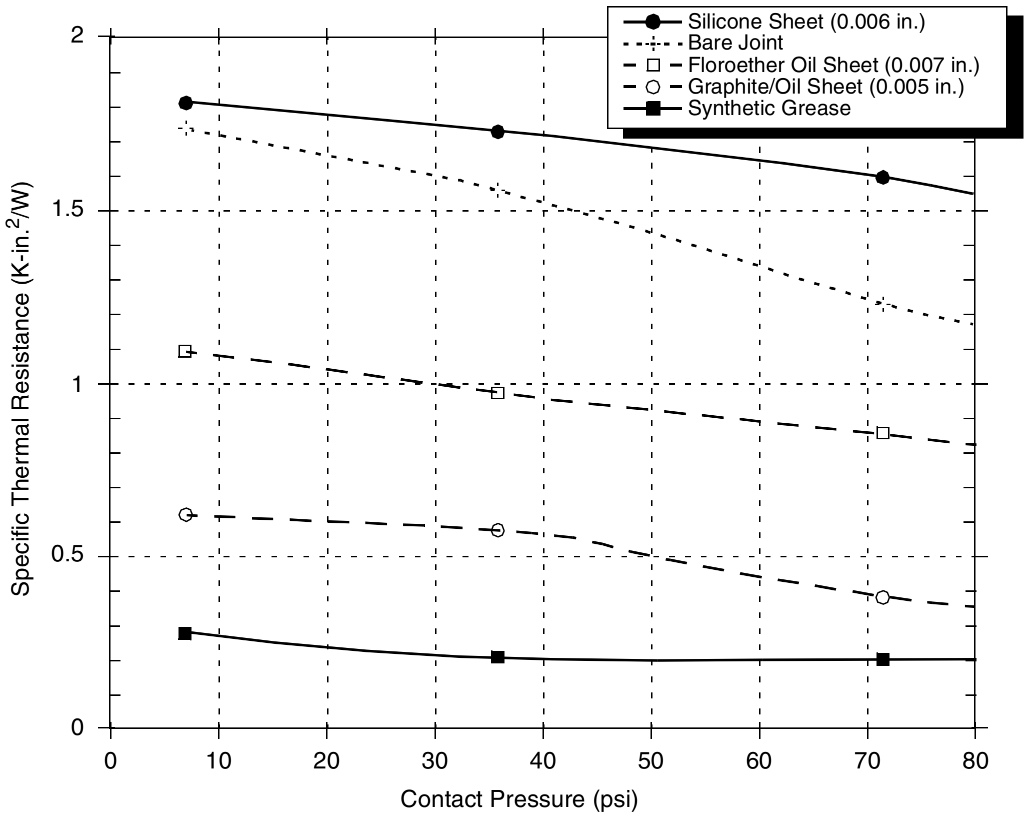


Figure 46. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St.	800-347-4572

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 52 is common to all known emulators.

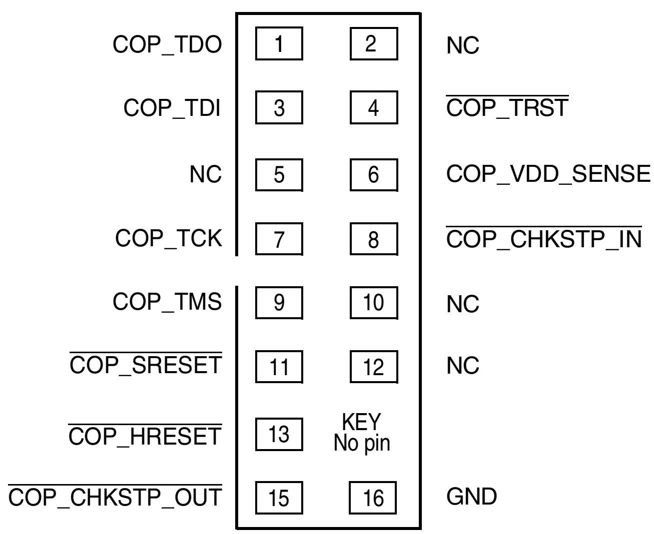
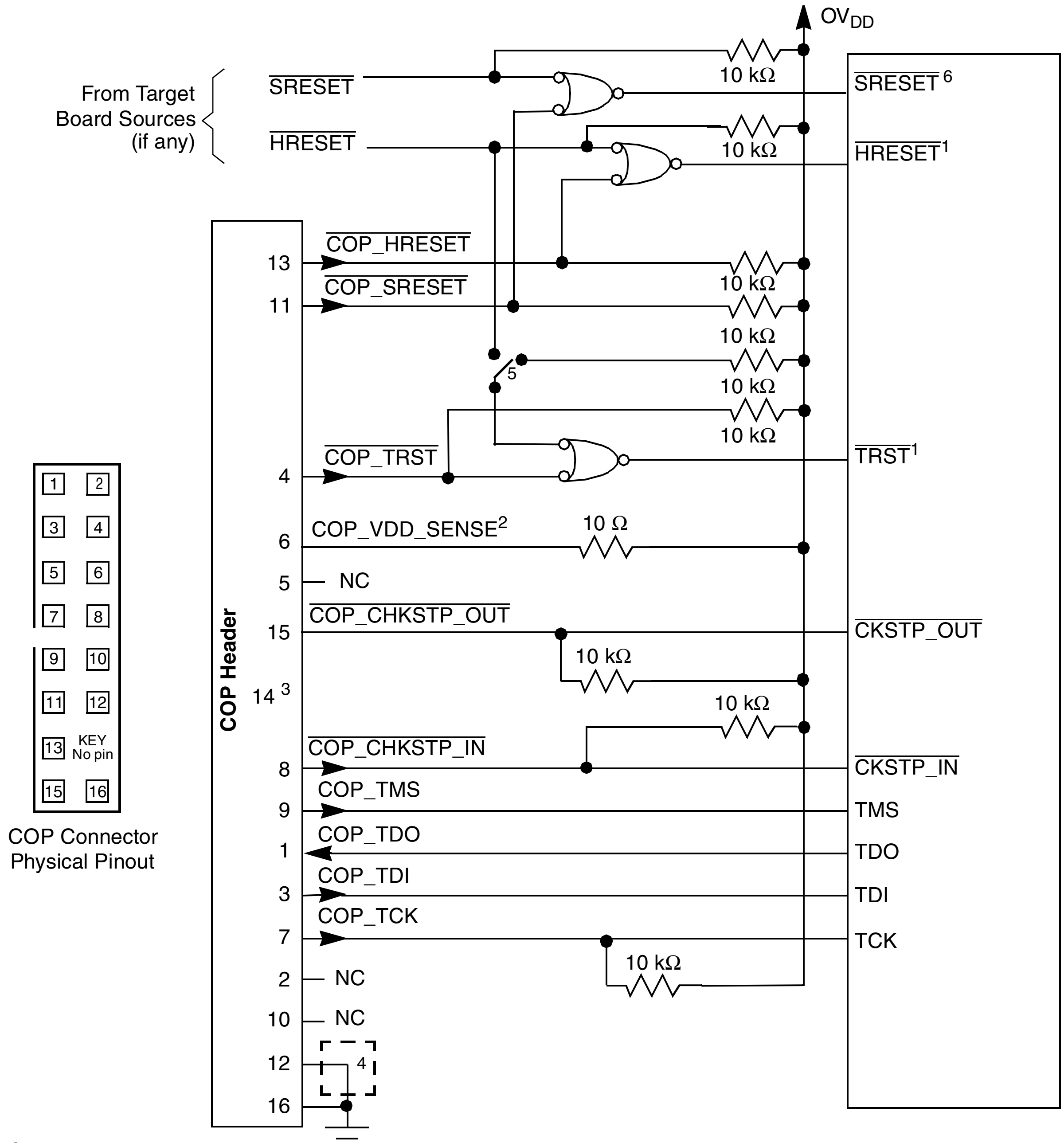


Figure 52. COP Connector Physical Pinout



Notes:
1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Nomenclature of Parts Fully Addressed by this Document."

19.1 Nomenclature of Parts Fully Addressed by this Document

Table 52 provides the Freescale part numbering nomenclature for the MPC8555E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 52. Part Numbering Nomenclature

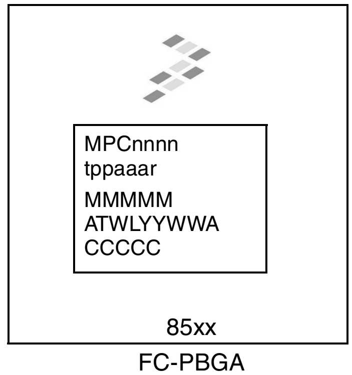
MPC	*nnnn*		*t*	*pp*	*aa*	*a*	*r*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**[1]	**Package**[2]	**Processor Frequency**[3]	**Platform Frequency**	**Revision Level**[4]
MPC	8555	Blank = not included E = included	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (lead free)	AJ = 533 MHz AK = 600 MHz AL = 667 MHz AP = 833 MHz AQ = 1000 MHZ	D = 266 MHz E = 300 MHz F = 333 MHz	

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz with a Platform Frequency selector of 333 MHz, Processor Frequency is limited to 533 MHz with a Platform Frequency selector of 266 MHz.
2. See Section 14, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. Contact you local Freescale field applications engineer (FAE).

19.2 Part Marking

Parts are marked as the example shown in Figure 54.



Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device