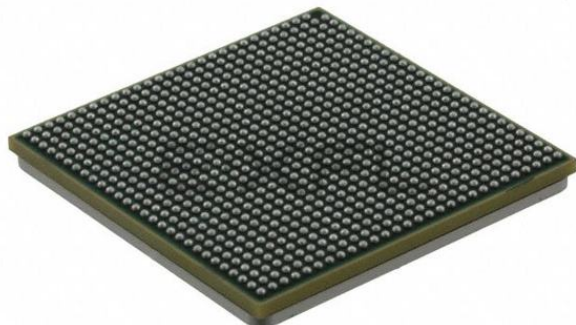




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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555epxake

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8555E may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8555E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V $\pm$ 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV	V
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V $\pm$ 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

Table 8. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	2 x t_{CCB_CLK}	—	—	ns	—
RTC clock low time	t_{RTCL}	2 x t_{CCB_CLK}	—	—	ns	—

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8555E. Table 9 provides the RESET initialization AC timing specifications.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$	100	—	μs	—
Minimum assertion time for $\overline{SRESET}$	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{HRESET}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{HRESET}$	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{HRESET}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{HRESET}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8555E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the $SYSCLK \times \text{platform PLL ratio}$.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8555E.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8555E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	-10	10	μA	4
Output high current ($V_{OUT} = 1.95$ V)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35$ V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	5	μA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 V \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, $f = 1$ MHz, $T_A = 25^\circ C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

Figure 6 provides the AC test load for the DDR bus.

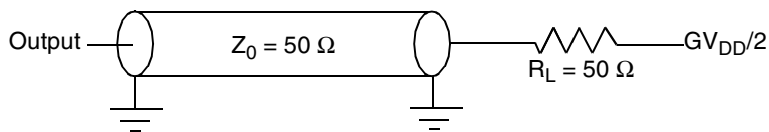


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31 \text{ V}$	V	1
V_{OUT}	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8555E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8555E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8555E.

Table 17. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB_CLK} / 1048576$	baud	3
Maximum baud rate	$f_{CCB_CLK} / 16$	baud	1, 3
Oversample rate	16	—	2, 3

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
3. Guaranteed by design.

8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 18](#) and [Table 19](#). The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (for example, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}^2	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR} , $t_{MTXF}^{2,3}$	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

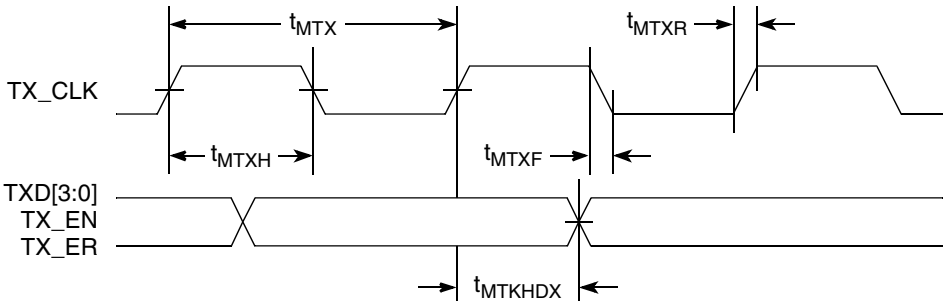


Figure 10. MII Transmit AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}^{5}	–500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}^{6}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ⁴	t_{RGTH}/t_{RGT}^{6}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ³	t_{RGTH}/t_{RGT}^{6}	40	50	60	%
Rise and fall times	$t_{RGTR}^{6,7}, t_{RGTF}^{6,7}$	—	—	0.75	ns

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Guaranteed by characterization.
- Guaranteed by design.
- Signal timings are measured at 0.5 and 2.0 V voltage levels.

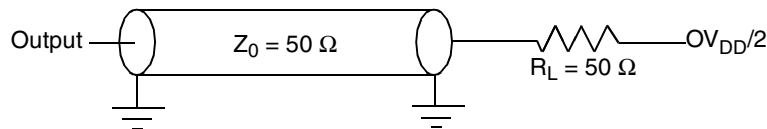
Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to address valid for LAD	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV3}	—	0.8	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.3		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOX1}	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)		–1.8			
Output hold from local bus clock for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOX2}	–2.7	—	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)		–1.8			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOZ1}	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.4		
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOZ2}	—	1.0	ns	5
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.4		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $\text{OV}_{\text{DD}}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times \text{OV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{OV}_{\text{DD}}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.


Figure 16. Local Bus C Test Load

Local Bus

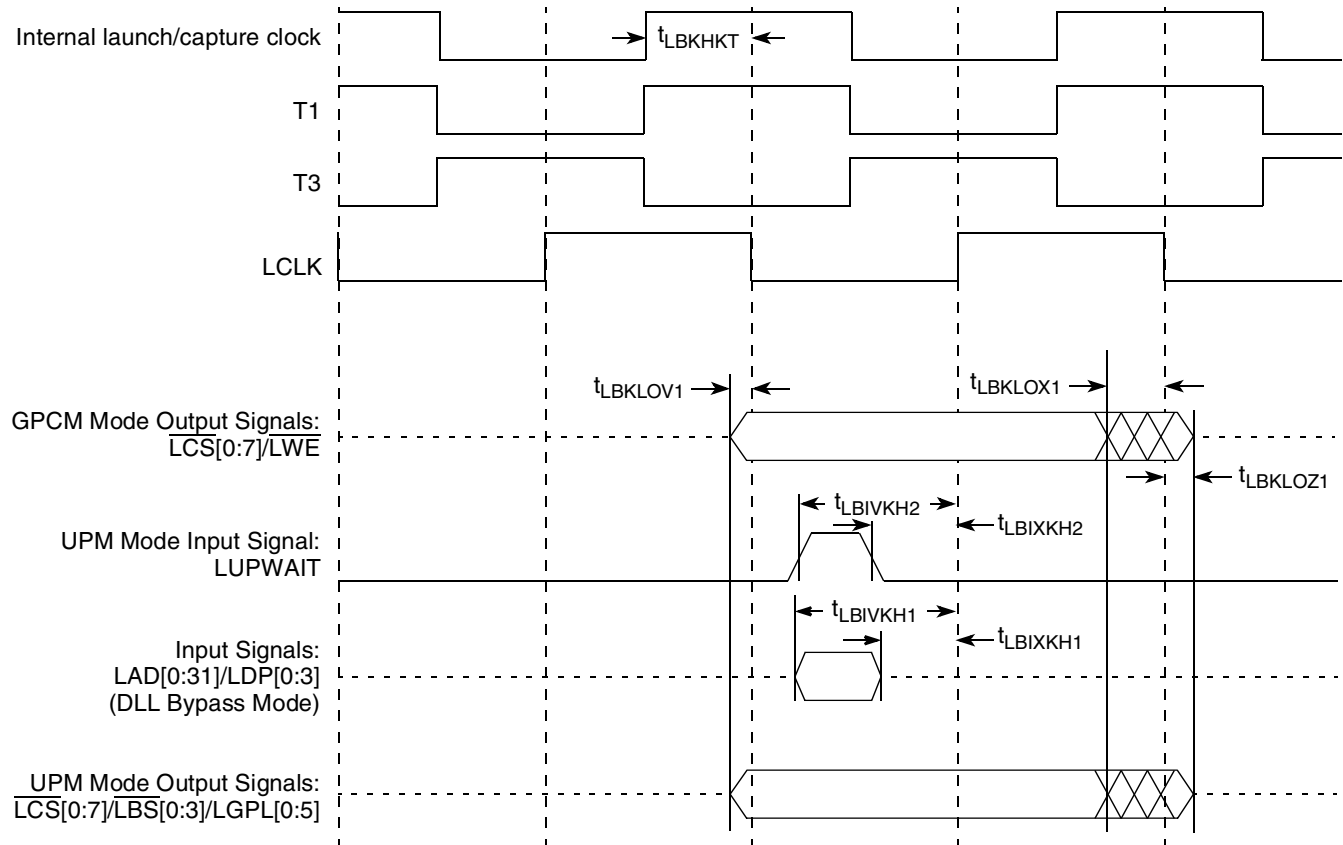


Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

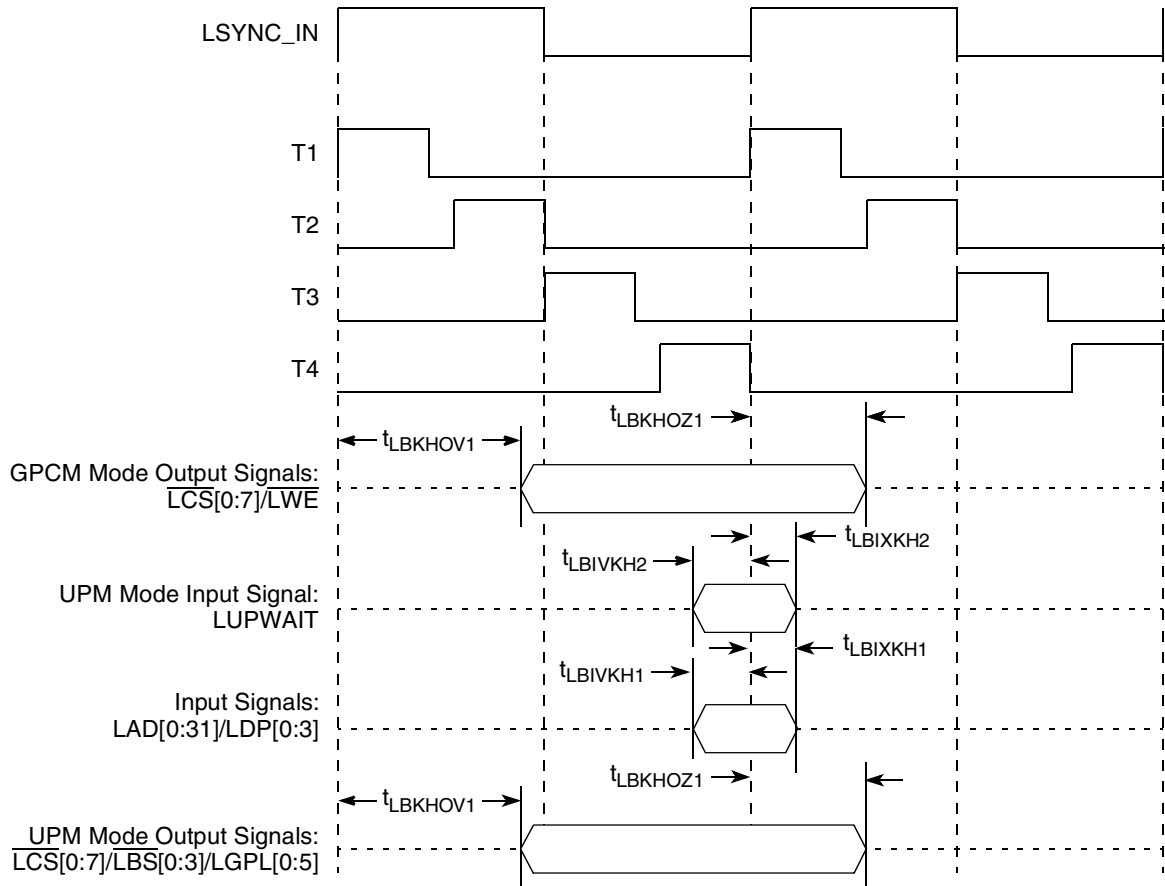


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 24 through Figure 30 represent the AC timing from Table 33 and Table 34. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 24 shows the FCC internal clock.

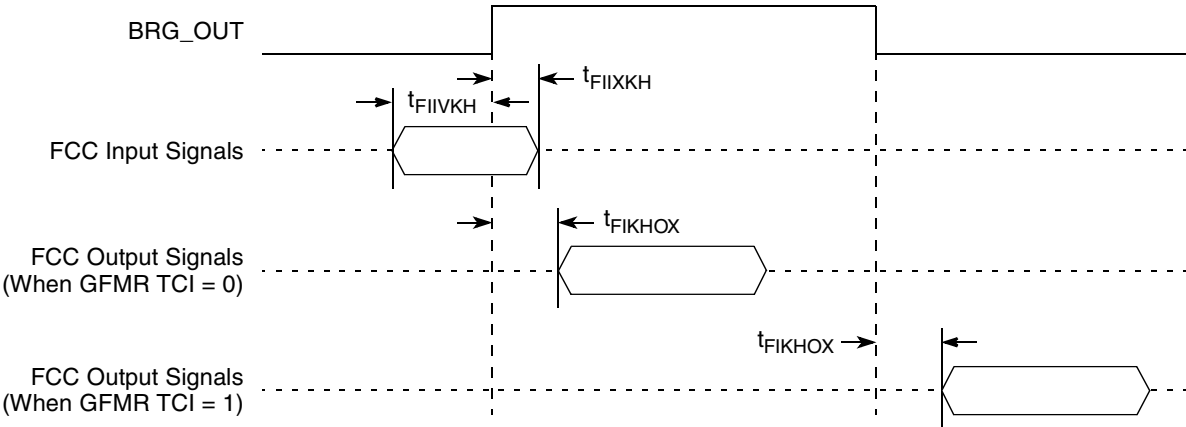


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

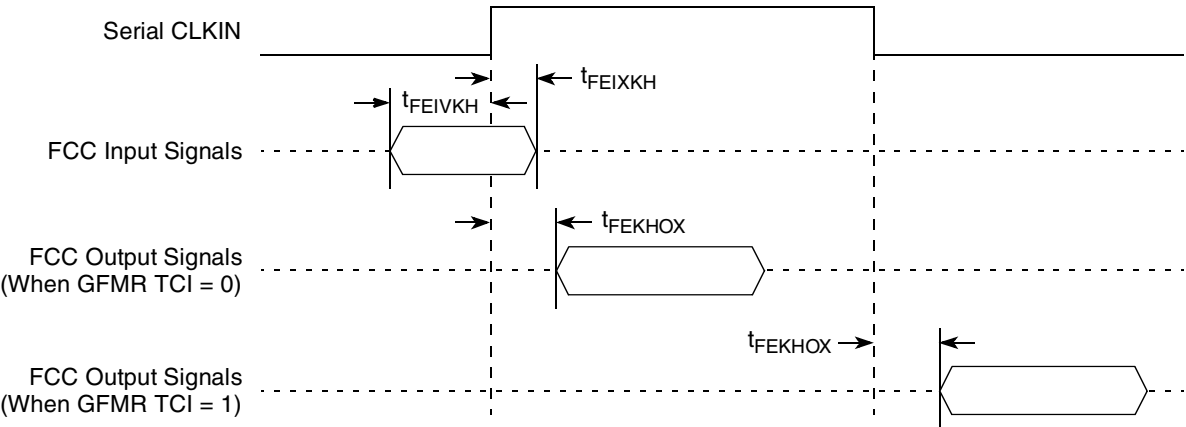


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

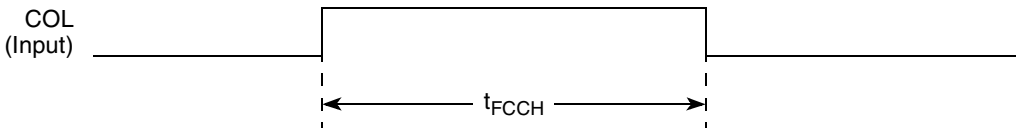
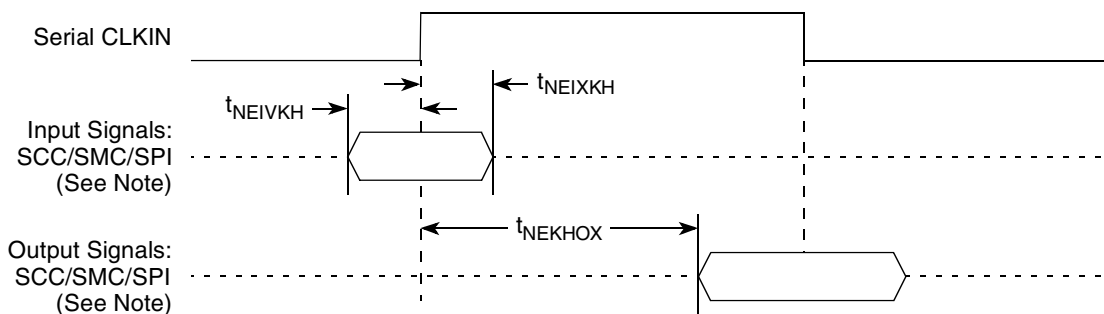


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

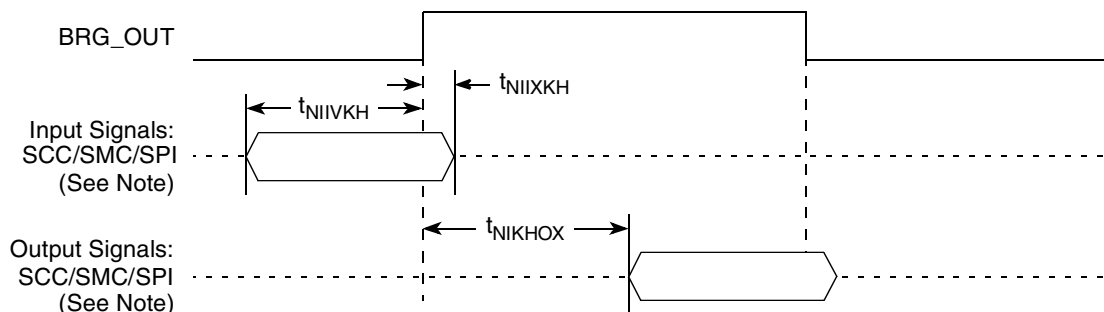
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

¹ SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

² SPI AC timings refer always to SPICLK.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs of the MPC8555E.

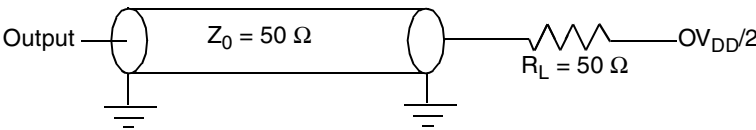


Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

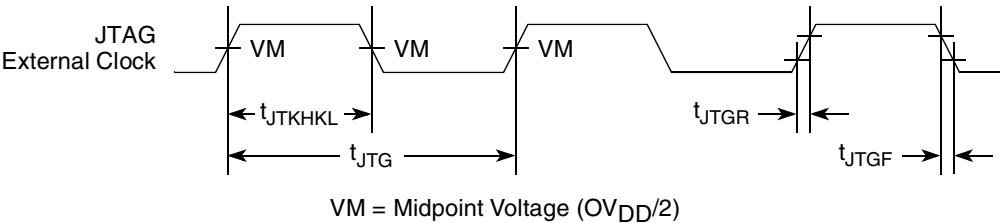


Figure 33. JTAG Clock Input Timing Diagram

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

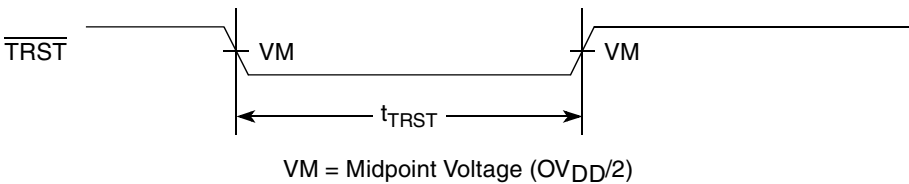


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

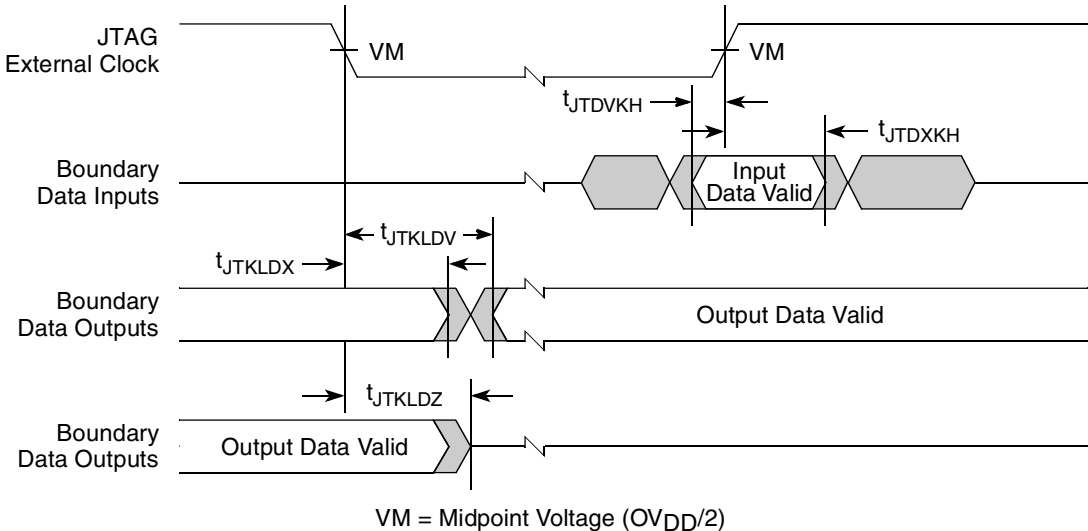


Figure 35. Boundary-Scan Timing Diagram

Figure 40 shows the PCI input AC timing conditions.

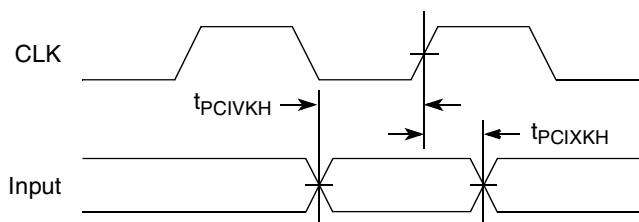


Figure 40. PCI Input AC Timing Measurement Conditions

Figure 41 shows the PCI output AC timing conditions.

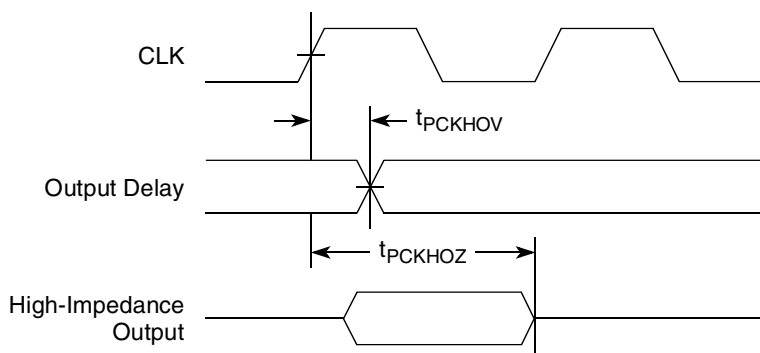


Figure 41. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8555E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

14.3 Pinout Listings

Table 43 provides the pin-out listing for the MPC8555E, 783 FC-PBGA package.

Table 43. MPC8555E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32], PCI2_AD[31:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV _{DD}	17
PCI_C_BE64[7:4] PCI2_C_BE[3:0]	AG13, AH13, V14, W14	I/O	OV _{DD}	17
PCI_C_BE64[3:0] PCI1_C_BE[3:0]	AH8, AB10, AD11, AC12	I/O	OV _{DD}	17
PCI1_PAR	AA11	I/O	OV _{DD}	—
PCI1_PAR64/PCI2_PAR	Y14	I/O	OV _{DD}	—
PCI1_FRAME	AC10	I/O	OV _{DD}	2
PCI1_TRDY	AG10	I/O	OV _{DD}	2
PCI1_IRDY	AD10	I/O	OV _{DD}	2
PCI1_STOP	V11	I/O	OV _{DD}	2
PCI1_DEVSEL	AH10	I/O	OV _{DD}	2
PCI1_IDSEL	AA9	I	OV _{DD}	—
PCI1_REQ64/PCI2_FRAME	AE13	I/O	OV _{DD}	5, 10
PCI1_ACK64/PCI2_DEVSEL	AD13	I/O	OV _{DD}	2
PCI1_PERR	W11	I/O	OV _{DD}	2
PCI1_SERR	Y11	I/O	OV _{DD}	2, 4
PCI1_REQ[0]	AF5	I/O	OV _{DD}	—
PCI1_REQ[1:4]	AF3, AE4, AG4, AE5	I	OV _{DD}	—
PCI1_GNT[0]	AE6	I/O	OV _{DD}	—
PCI1_GNT[1:4]	AG5, AH5, AF6, AG6	O	OV _{DD}	5, 9
PCI1_CLK	AH25	I	OV _{DD}	—
PCI2_CLK	AH27	I	OV _{DD}	—
PCI2_GNT[0]	AC18	I/O	OV _{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV _{DD}	—
TDI	AG21	I	OV _{DD}	12
TDO	AF19	O	OV _{DD}	11
TMS	AF23	I	OV _{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV _{DD}	12
DFT				
LSSD_MODE	AG19	I	OV _{DD}	20
L1_TSTCLK	AB22	I	OV _{DD}	20
L2_TSTCLK	AG22	I	OV _{DD}	20
$\overline{\text{TEST_SEL0}}$	AH20	I	OV _{DD}	3
TEST_SEL1	AG26	I	OV _{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
AV _{DD1}	AH19	Power for e500 PLL (1.2 V)	AV _{DD1}	—
AV _{DD2}	AH18	Power for CCB PLL (1.2 V)	AV _{DD2}	—
AV _{DD3}	AH17	Power for CPM PLL (1.2 V)	AV _{DD3}	—
AV _{DD4}	AF28	Power for PCI1 PLL (1.2 V)	AV _{DD4}	—
AV _{DD5}	AE28	Power for PCI2 PLL (1.2 V)	AV _{DD5}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/O	OV _{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/O	OV _{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/O	OV _{DD}	—

Notes:

- All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
- Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
- TEST_SEL0 must be pulled-high, TEST_SEL1 must be tied to ground.
- This pin is an open drain signal.
- This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8555E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
- Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCCLK PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See [Section 15.2, “Platform/System PLL Ratio.”](#)
- The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See the [Section 15.3, “e500 Core PLL Ratio.”](#)
- Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
- This output is actively driven during reset rather than being three-stated during reset.
- These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- Internal thermally sensitive resistor.
- No connections should be made to these pins.
- These pins are not connected for any functional use.
- PCI specifications recommend that a weak pull-up resistor (2–10 k Ω) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2_C_BE}}$ [7:4]).
- If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
- Recommend a pull-up resistor (~1 k Ω) be placed on this pin to OV_{DD}.
- These are test signals for factory use only and must be pulled up (100 Ω to 1k Ω) to OV_{DD} for normal machine operation.
- If this signal is used as both an input and an output, a weak pull-up (~10k Ω) is required on this pin.
- MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

the heat sink should be slowly removed. Heating the heat sink to 40–50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

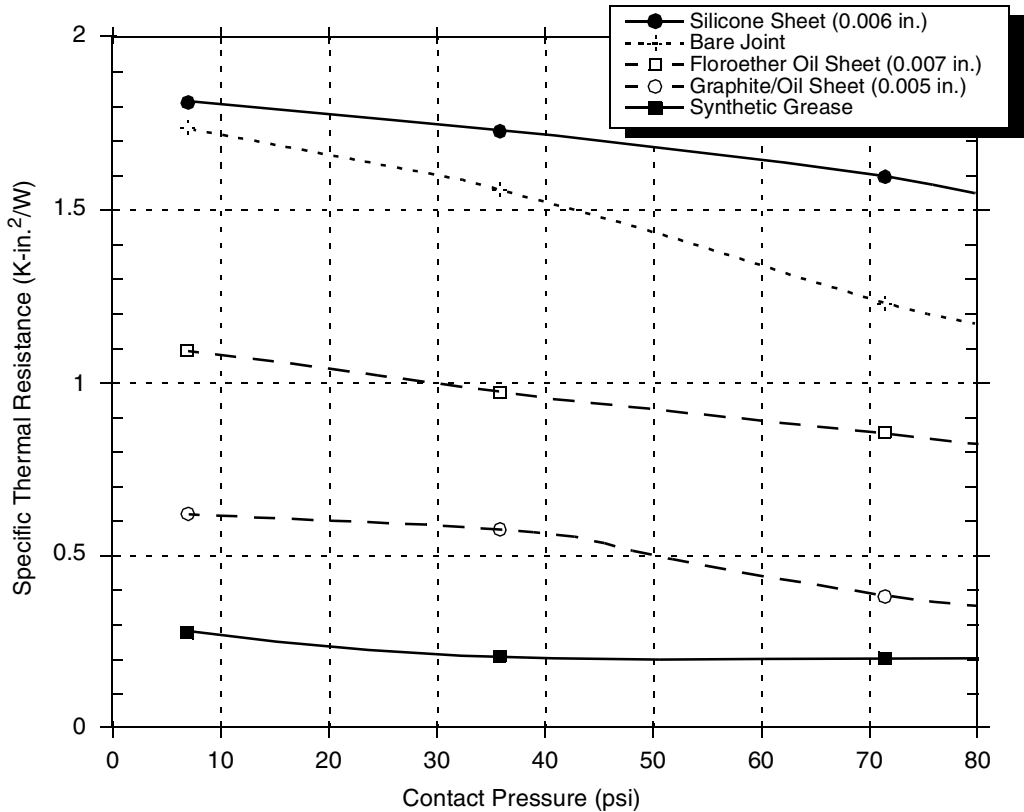


Figure 46. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78 th St.	800-347-4572

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 52 is common to all known emulators.

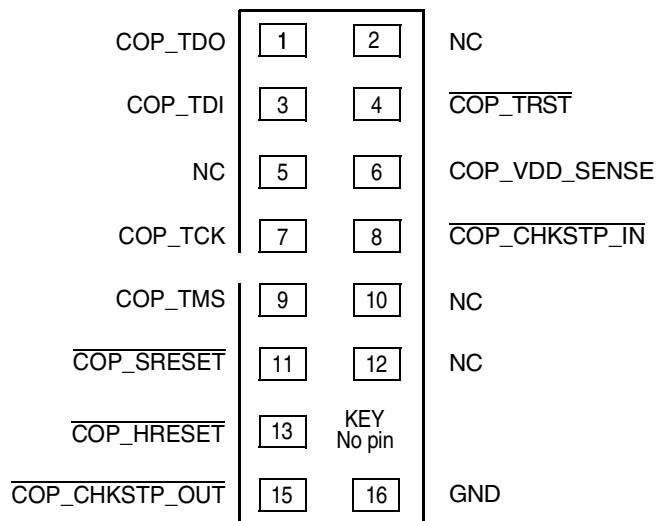


Figure 52. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.