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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8555epxaqf

1 Overview

The following section provides a high-level overview of the MPC8555E features. Figure 1 shows the major functional units within the MPC8555E.

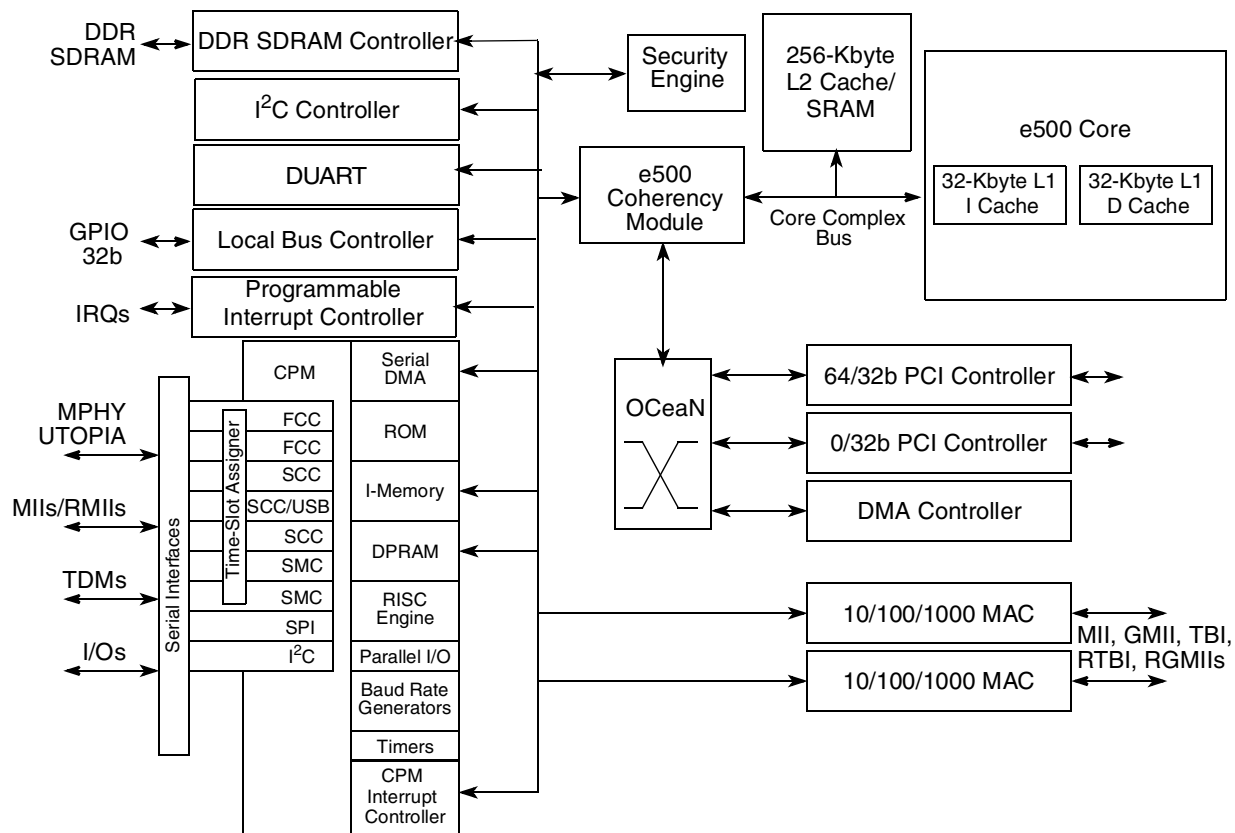


Figure 1. MPC8555E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8555E feature set.

- Embedded e500 Book E-compatible core
 - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
 - Dual-issue superscalar, 7-stage pipeline design
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
 - Lockable L1 caches—entire cache or on a per-line basis
 - Separate locking for instructions and data
 - Single-precision floating-point operations
 - Memory management unit especially designed for embedded applications
 - Enhanced hardware and software debug support
 - Dynamic power management
 - Performance monitor facility

- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
 - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
 - Supports power save modes: doze, nap, and sleep
 - Employs dynamic power management
 - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8555E. The MPC8555E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8555E for the 3.3-V signals, respectively.

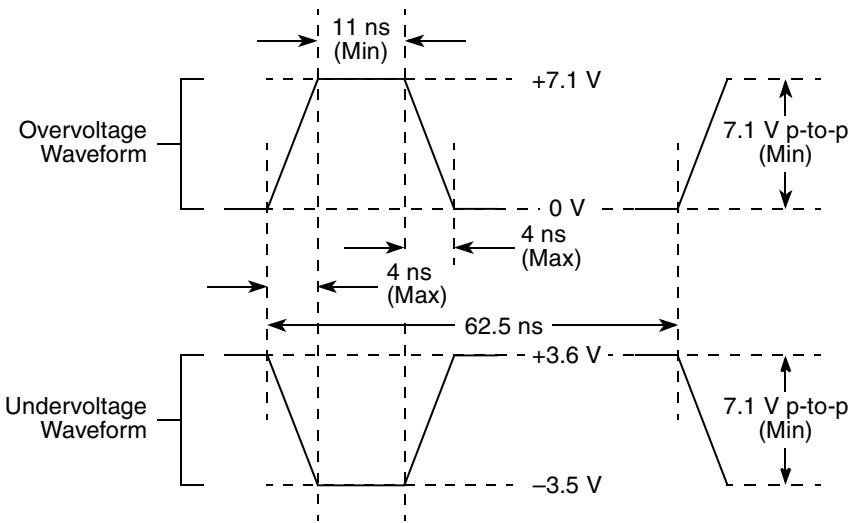


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	$OV_{DD} = 3.3\text{ V}$	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	$GV_{DD} = 2.5\text{ V}$	
TSEC/10/100 signals	42	$LV_{DD} = 2.5/3.3\text{ V}$	
DUART, system control, I2C, JTAG	42	$OV_{DD} = 3.3\text{ V}$	

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the PCI interface is determined by the setting of the `PCI_GNT1` signal at reset.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCX}	2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKMHM}	−0.9 −1.1 −1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.9$	$-0.5 \times t_{MCK} + 0.3$	ns	7
MDQS epilogue end	t_{DDKLME}	−0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{MCK}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
- In the source synchronous mode, MCK/ $\overline{MCK}$ can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns. t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this typically is set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8555E.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8555E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2 GMII Transmit AC Timing Specifications

Table 20 provides the GMII transmit AC timing specifications.

Table 20. GMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise and fall times	$t_{GTXR}^3, t_{GTXF}^{2,4}$	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

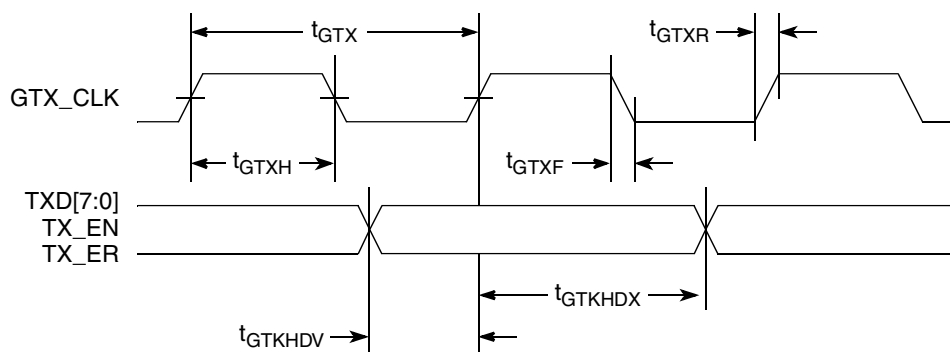


Figure 7. GMII Transmit AC Timing Diagram

8.2.2.1 GMII Receive AC Timing Specifications

Table 21 provides the GMII receive AC timing specifications.

Table 21. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} ^{2,3}	—	—	1.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

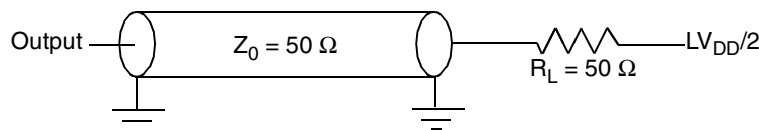


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

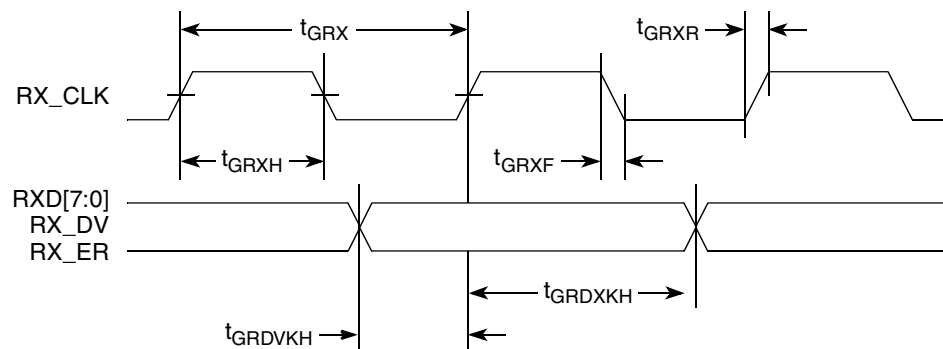


Figure 9. GMII Receive AC Timing Diagram

Table 30. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKHOZ2}	—	2.8	ns	5, 9
	$\overline{\text{LWE}}[0:1] = 11$ (default)			4.2		

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC_IN for DLL enabled mode.
- All signals are measured from $\text{OV}_{\text{DD}}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times \text{OV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{OV}_{\text{DD}}/2$.
- Guaranteed by characterization.
- Guaranteed by design.

Table 31 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL bypassed.

Table 31. Local Bus General Timing Parameters—DLL Bypassed

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHK1}	1.8	3.4	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		t_{LBKSKEW}	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		t_{LBIVKH1}	5.2	—	ns	3, 4
LUPWAIT input setup to local bus clock		t_{LBIVKH2}	5.1	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		t_{LBIXKH1}	−1.3	—	ns	3, 4
LUPWAIT input hold from local bus clock		t_{LBIXKH2}	−0.8	—	ns	3, 4
LAL output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LAL)	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV1}	—	0.5	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.0		
Local bus clock to data valid for LAD/LDP	$\overline{\text{LWE}}[0:1] = 00$	t_{LBKLOV2}	—	0.7	ns	3
	$\overline{\text{LWE}}[0:1] = 11$ (default)			2.2		

Table 33. CPM Input AC Timing Specifications ¹ (continued)

Characteristic	Symbol ²	Min ³	Unit
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns
PIO inputs—input setup time	t_{PIIVKH}	8	ns
PIO inputs—input hold time	t_{PIIXKH}	1	ns
COL width high (FCC)	t_{FCCH}	1.5	CLK

Notes:

- Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time. And t_{TDIXKH} symbolizes the TDM timing (TD) with respect to the time the input signals (I) reach the invalid state (X) relative to the reference clock t_{FCC} (K) going to the high (H) state or hold time.
- PIO and TIMER inputs and outputs are asynchronous to SYSCLK or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Table 34. CPM Output AC Timing Specifications ¹

Characteristic	Symbol ²	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t_{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t_{FEKHOX}	2	8	ns
SCC/SMC/SPI outputs—internal clock (NMSI) delay	t_{NIKHOX}	0.5	10	ns
SCC/SMC/SPI outputs—external clock (NMSI) delay	t_{NEKHOX}	2	8	ns
TDM outputs/SI delay	t_{TDKHOX}	2.5	11	ns
PIO outputs delay	t_{PIKHOX}	1	11	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the CPM.

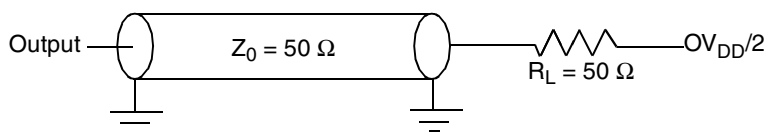

Figure 23. CPM AC Test Load

Figure 24 through Figure 30 represent the AC timing from Table 33 and Table 34. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 24 shows the FCC internal clock.

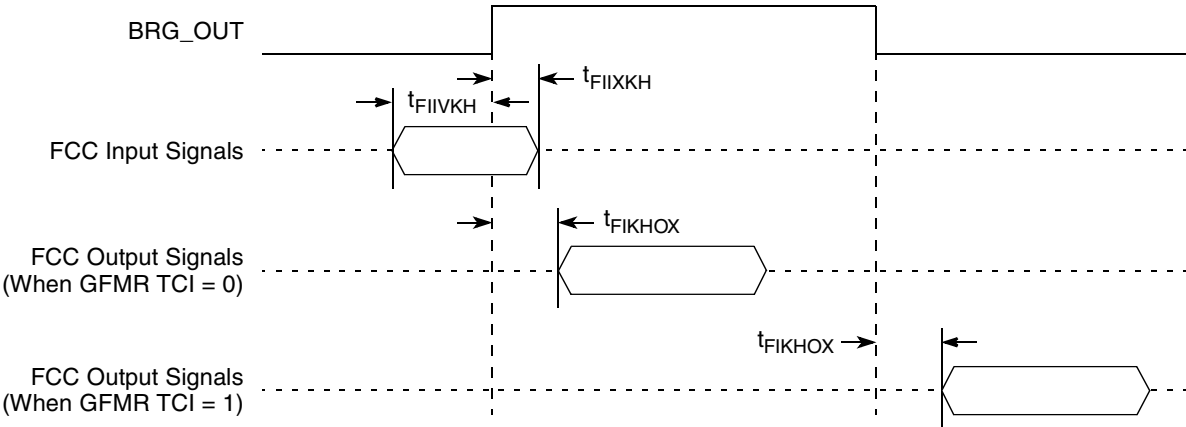


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

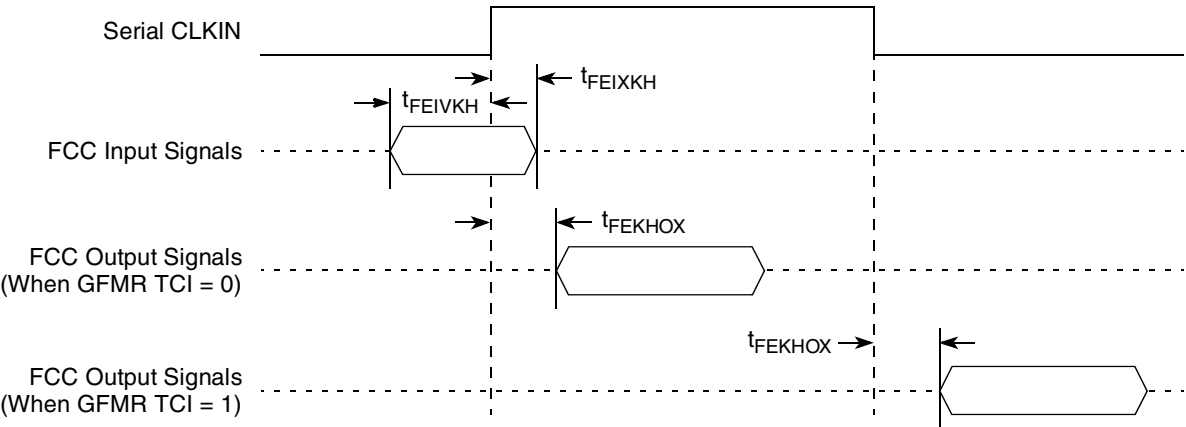


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

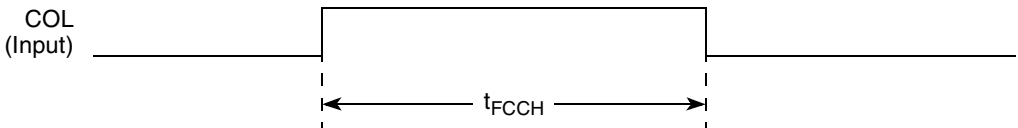


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{REQ64}$ to $\overline{HRESET}$ ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

- Note that the symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
- The setup and hold time is with respect to the rising edge of $\overline{HRESET}$.
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for $\overline{HRESET}$ is 100 μs .
- Guaranteed by characterization.
- Guaranteed by design.

Figure 16 provides the AC test load for PCI.

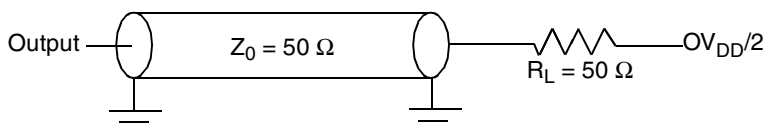


Figure 39. PCI AC Test Load

Figure 40 shows the PCI input AC timing conditions.

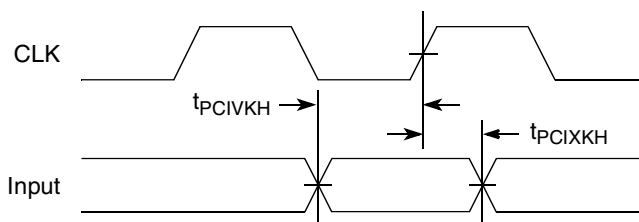


Figure 40. PCI Input AC Timing Measurement Conditions

Figure 41 shows the PCI output AC timing conditions.

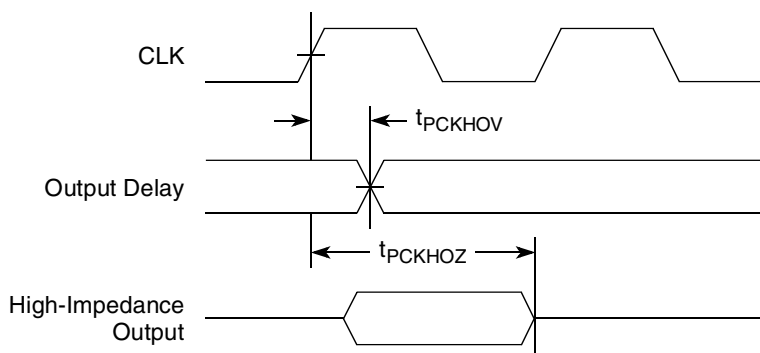


Figure 41. PCI Output AC Timing Measurement Condition

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8555E FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	8.7 mm × 9.3 mm × 0.75 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV _{DD}	—
IRQ8	AB20	I	OV _{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV _{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV _{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV _{DD}	1
IRQ_OUT	AB21	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV _{DD}	5, 9
EC_MDIO	E1	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV _{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV _{DD}	9, 18
TSEC1_TX_EN	C8	O	LV _{DD}	11
TSEC1_TX_ER	B8	O	LV _{DD}	—
TSEC1_TX_CLK	C6	I	LV _{DD}	—
TSEC1_GTX_CLK	B6	O	LV _{DD}	—
TSEC1_CRS	C3	I	LV _{DD}	—
TSEC1_COL	G7	I	LV _{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV _{DD}	—
TSEC1_RX_DV	D2	I	LV _{DD}	—
TSEC1_RX_ER	E5	I	LV _{DD}	—
TSEC1_RX_CLK	D6	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV _{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV _{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV _{DD}	11
TSEC2_TX_ER	D11	O	LV _{DD}	—
TSEC2_TX_CLK	D10	I	LV _{DD}	—
TSEC2_GTX_CLK	C10	O	LV _{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PB[18:31]	P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/O	OV _{DD}	—
PC[0, 1, 4–29]	R8, R9, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8	I/O	OV _{DD}	—
PD[7, 14–25, 29–31]	Y4, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD6, AE3, AE2	I/O	OV _{DD}	—

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
3. TEST_SEL0 must be pulled-high, TEST_SEL1 must be tied to ground.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8555E is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCCLK PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See [Section 15.2, “Platform/System PLL Ratio.”](#)
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See the [Section 15.3, “e500 Core PLL Ratio.”](#)
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 k Ω) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI2_C_BE}}$ [7:4]).
18. If this pin is connected to a device that pulls down during reset, an external pull-up is required to that is strong enough to pull this signal to a logic 1 during reset.
19. Recommend a pull-up resistor (~1 k Ω) be placed on this pin to OV_{DD}.
20. These are test signals for factory use only and must be pulled up (100 Ω to 1k Ω) to OV_{DD} for normal machine operation.
21. If this signal is used as both an input and an output, a weak pull-up (~10k Ω) is required on this pin.
22. MSYNC_IN and MSYNC_OUT should be connected together for proper operation.

15 Clocking

This section describes the PLL configuration of the MPC8555E. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

[Table 44](#) provides the clocking specifications for the processor core and [Table 44](#) provides the clocking specifications for the memory bus.

Table 44. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency										Unit	Notes
	533 MHz		600 MHz		667 MHz		833 MHz		1000 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	533	400	600	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
- 2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. 1000 MHz frequency supports only a 1.3 V core.

Table 45. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	533, 600, 667, 883, 1000 MHz			
	Min	Max		
Memory bus frequency	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 15.2, “Platform/System PLL Ratio,”](#) and [Section 15.3, “e500 Core PLL Ratio,”](#) for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. 1000 MHz frequency supports only a 1.3 V core.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL (AV_{DD1}) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL (AV_{DD2}) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL (AV_{DD3}) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL (AV_{DD4}) generates the clocking for the first PCI bus.
5. The PCI2 PLL (AV_{DD5}) generates the clock for the second PCI bus.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , AV_{DD3} , AV_{DD4} , and AV_{DD5} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 50](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

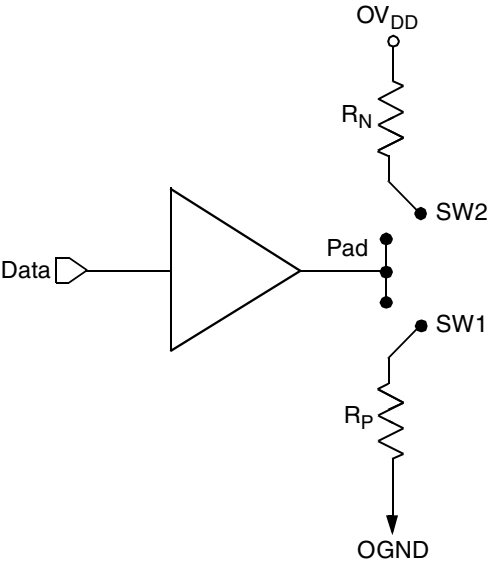


Figure 51. Driver Impedance Measurement

The value of this resistance and the strength of the driver’s current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

[Table 50](#) summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 50. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	Ω
R_P	43 Target	25 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See [Table 1](#), $T_j = 105^\circ\text{C}$.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 52 is common to all known emulators.

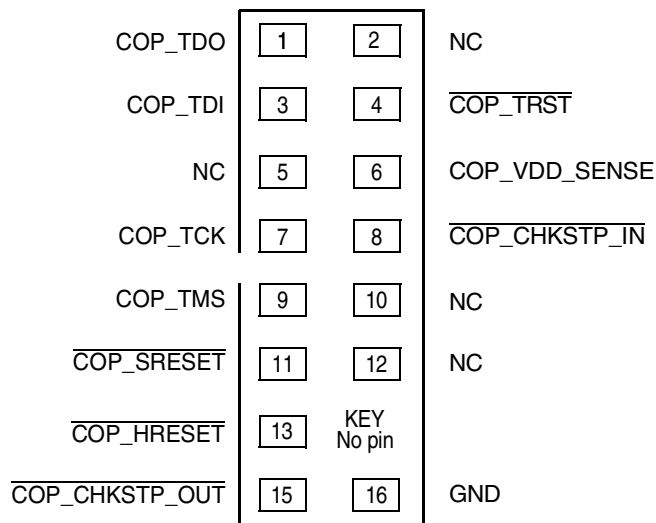
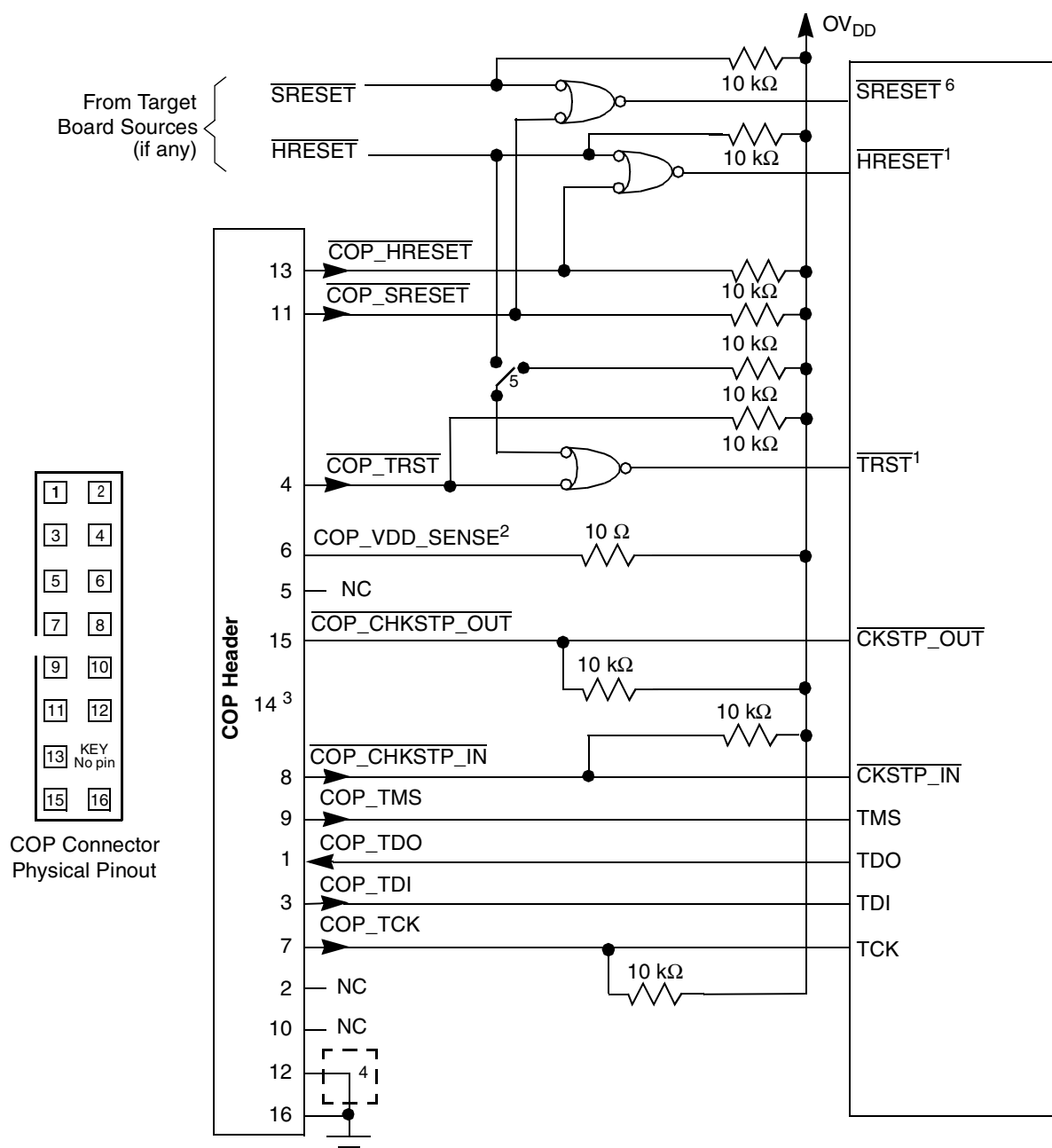


Figure 52. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 10.2, “CPM AC Timing Specifications.”
4.1	7/2007	Inserted Figure 3 , “Maximum AC Waveforms on PCI interface for 3.3-V Signaling.”
4	12/2006	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.2	11/2006	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.1	10/2005	Added footnote 2 about junction temperature in Table 4 . Added max. power values for 1000 MHz core frequency in Table 4 . Removed Figure 3 , “Maximum AC Waveforms on PCI Interface for 3.3-V Signaling.” Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30 . Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values in Table 30 . Added note 3 to $t_{LBKHOV1}$ in Table 30 . Modified note 3 in Table 30 and Table 31 . Added note 3 to $t_{LBKLOV1}$ in Table 31 . Modified values for t_{LBKHKT} , $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31 . Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21 . Modified note for signal CLK_OUT in Table 43 . PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43 . Added column for Encryption Acceleration in Table 52 .
3	8/2005	Modified max. power values in Table 4 . Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43 .
2	8/2005	Previous revision’s history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31 . Added note 2 in Table 7 . Modified min and max values for t_{DDKHMP} in Table 14 .
1	6/2005	Changed V_{DD} to O_{VDD} for the supply voltage Ethernet management interface in Table 27 . Modified footnote 4 and changed typical power for the 1000 MHz core frequency in Table 4 . Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31 .
0	6/2005	Initial release.