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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8555evtajd

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
 - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 32-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI
 - Four inbound windows
 - Four outbound windows plus default translation for PCI
- DDR memory controller
 - Programmable timing supporting first generation DDR SDRAM
 - 64-bit data interface, up to MHz data rate
 - Four banks of memory supported, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontinuous memory mapping
 - Sleep mode support for self refresh DDR SDRAM
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access via JTAG port
 - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8555E may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8555E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V \pm 60 mV 1.3 V \pm 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V \pm 60 mV 1.3 V \pm 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V \pm 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V \pm 165 mV 2.5 V \pm 125 mV	V
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V \pm 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8555E for the 3.3-V signals, respectively.

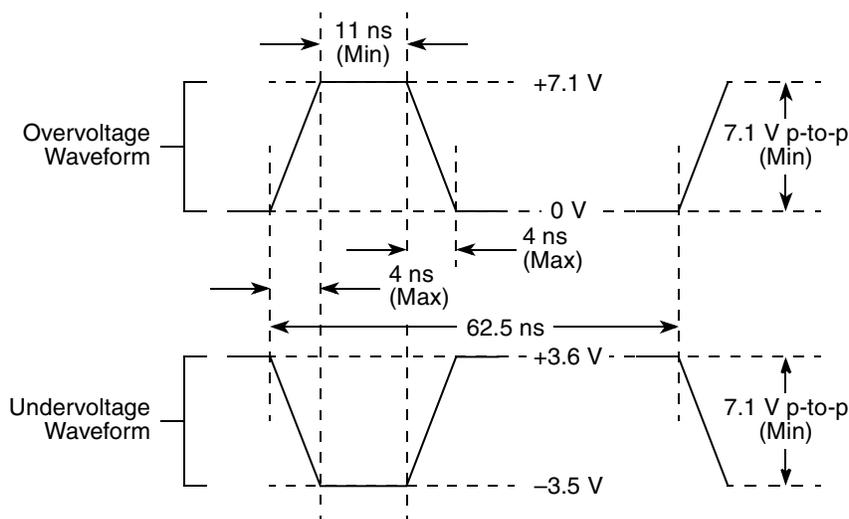


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	$OV_{DD} = 3.3\text{ V}$	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	$GV_{DD} = 2.5\text{ V}$	
TSEC/10/100 signals	42	$LV_{DD} = 2.5/3.3\text{ V}$	
DUART, system control, I2C, JTAG	42	$OV_{DD} = 3.3\text{ V}$	

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the `PCI_GNT1` signal at reset.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	$GV_{DD} + 0.3$	V	—
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR \leq 266 MHz	t_{DISKEW}	—	750 1125	ps	1

Note:

- Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$) or ECC (MECC[{0...7}] if $n = 8$).

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{\text{MCK[n]}}$ crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	-1000 -1100 -1200	200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	2.8 3.45 4.6	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	2.0 2.65 3.8	—	ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.8 3.45 4.6	—	ns	4

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

 At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHGX}	2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKMHM}	-0.9 -1.1 -1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.9$	$-0.5 \times t_{MCK} + 0.3$	ns	7
MDQS epilogue end	t_{DDKLME}	-0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals $\pm 0.1\text{ V}$.
- In the source synchronous mode, MCK/ $\overline{\text{MCK}}$ can be shifted in 1/4 applied cycle increments through the Clock Control Register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except $\overline{\text{MCK}}$, $\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle. The MCSx pins are separated from the ADDR/CMD (address and command) bus in the HW spec. This was separated because the MCSx pins typically have different loadings than the rest of the address and command bus, even though they have the same timings.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). In the source synchronous mode, MDQS can launch later than MCK by 0.3 ns at the maximum. However, MCK may launch later than MDQS by as much as 0.9 ns. t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this typically is set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8555E.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8555E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 provides the AC test load for the DDR bus.

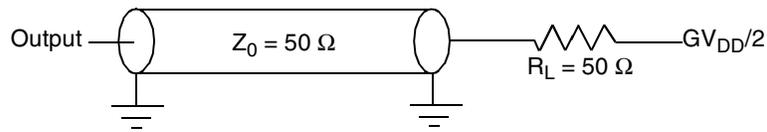


Figure 6. DDR AC Test Load

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31 \text{ V}$	V	1
V_{OUT}	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8555E.

7.1 DUART DC Electrical Characteristics

Table 16 provides the DC electrical characteristics for the DUART interface of the MPC8555E.

Table 16. DUART DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} \text{ (max)}$	-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min,}$ $I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8555E with the DLL enabled.

Table 30. Local Bus General Timing Parameters—DLL Enabled

Parameter	Configuration ⁷	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	7, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	3, 4, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	3, 4, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$\overline{LWE}[0:1] = 00$	$t_{LBKHOV1}$	—	2.3	ns	3, 8
	$\overline{LWE}[0:1] = 11$ (default)			3.8		
Local bus clock to data valid for LAD/LDP	$\overline{LWE}[0:1] = 00$	$t_{LBKHOV2}$	—	2.5	ns	3, 8
	$\overline{LWE}[0:1] = 11$ (default)			4.0		
Local bus clock to address valid for LAD	$\overline{LWE}[0:1] = 00$	$t_{LBKHOV3}$	—	2.6	ns	3, 8
	$\overline{LWE}[0:1] = 11$ (default)			4.1		
Output hold from local bus clock (except LAD/LDP and LALE)	$\overline{LWE}[0:1] = 00$	$t_{LBKHOX1}$	0.7	—	ns	3, 8
	$\overline{LWE}[0:1] = 11$ (default)					
Output hold from local bus clock for LAD/LDP	$\overline{LWE}[0:1] = 00$	$t_{LBKHOX2}$	0.7	—	ns	3, 8
	$\overline{LWE}[0:1] = 11$ (default)					
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$\overline{LWE}[0:1] = 00$	$t_{LBKHOZ1}$	—	2.8	ns	5, 9
	$\overline{LWE}[0:1] = 11$ (default)			4.2		

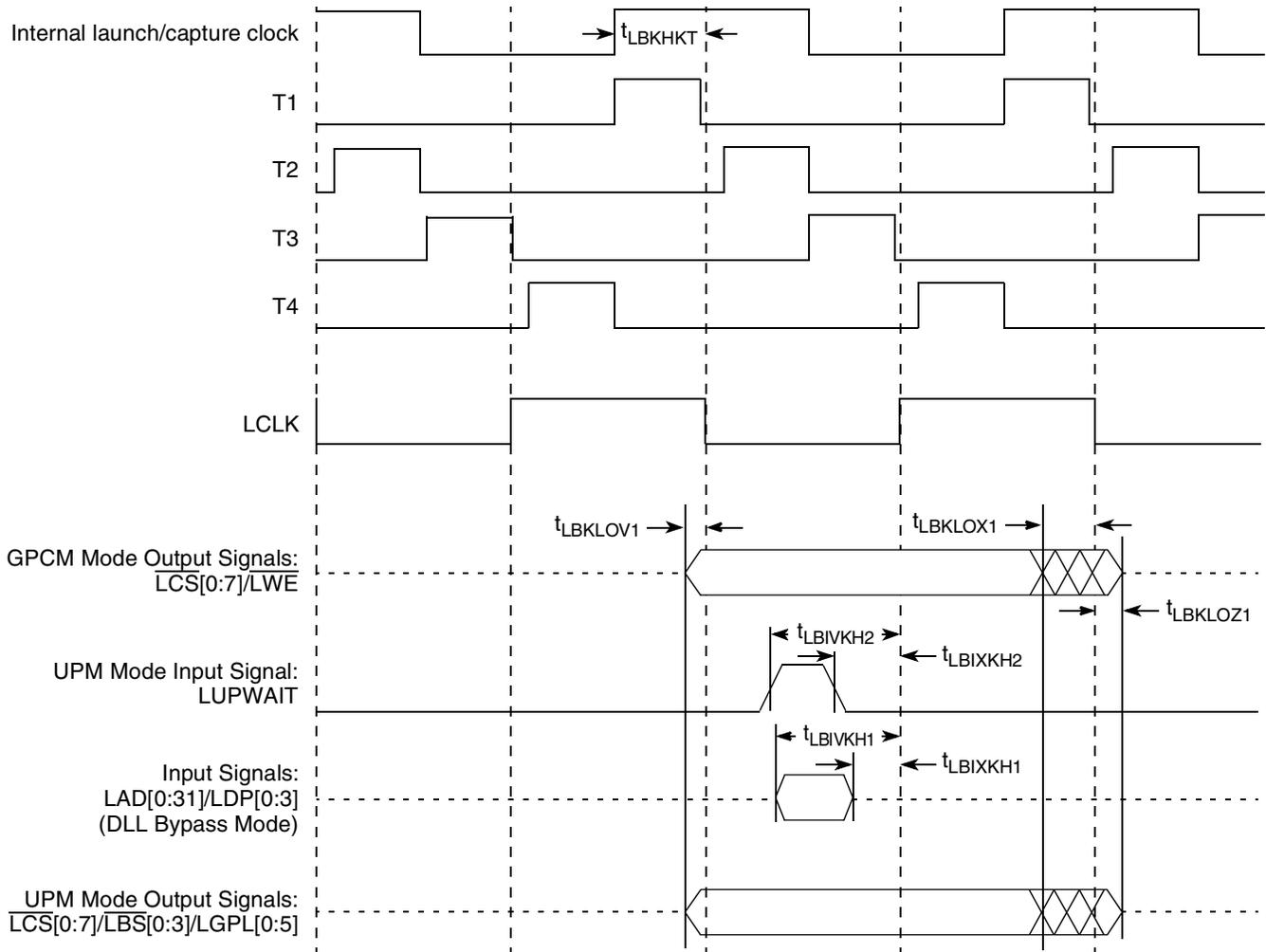
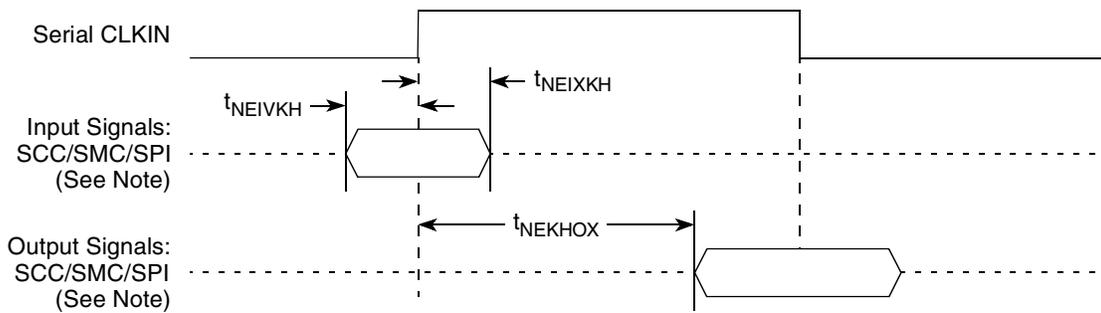


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

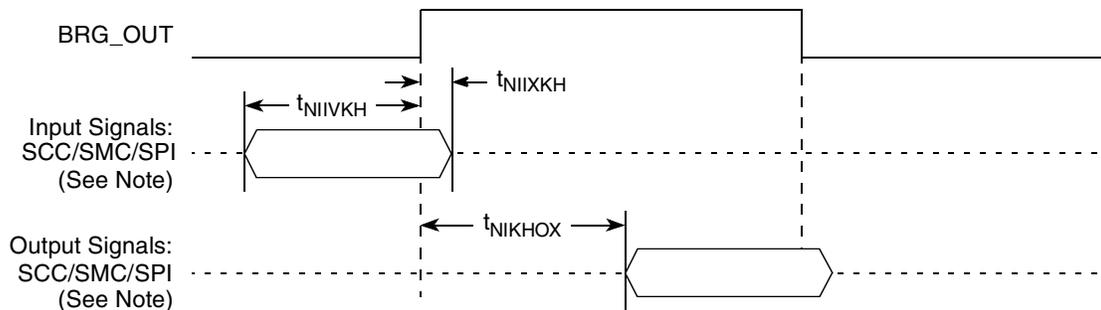
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

¹ SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.

² SPI AC timings refer always to SPICLK.

11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8555E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) ¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
\overline{TRST} assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	— —		4
Valid times:				ns	
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25		5
Output hold times:				ns	
Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	— —	— —		5
JTAG external clock to output high impedance:				ns	
Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9		5, 6

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- \overline{TRST} is an asynchronous level sensitive signal. The setup time is for test purposes only.
- Non-JTAG signal input timing with respect to t_{TCLK} .
- Non-JTAG signal output timing with respect to t_{TCLK} .
- Guaranteed by design.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{REQ64}$ to \overline{HRESET} ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
\overline{HRESET} to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
\overline{HRESET} high to first \overline{FRAME} assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

- Note that the symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
- The setup and hold time is with respect to the rising edge of \overline{HRESET} .
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for \overline{HRESET} is 100 μs .
- Guaranteed by characterization.
- Guaranteed by design.

Figure 16 provides the AC test load for PCI.

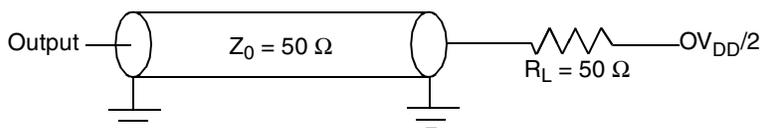


Figure 39. PCI AC Test Load

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_GNT[1:4]	AD18, AE18, AE19, AD19	O	OV _{DD}	5, 9
PCI2_IDSEL	AC22	I	OV _{DD}	—
PCI2_IRDY	AD20	I/O	OV _{DD}	2
PCI2_PERR	AC20	I/O	OV _{DD}	2
PCI2_REQ[0]	AD21	I/O	OV _{DD}	—
PCI2_REQ[1:4]	AE21, AD22, AE22, AC23	I	OV _{DD}	—
PCI2_SERR	AE20	I/O	OV _{DD}	2,4
PCI2_STOP	AC21	I/O	OV _{DD}	2
PCI2_TRDY	AC19	I/O	OV _{DD}	2
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV _{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV _{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV _{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV _{DD}	—
MBA[0:1]	B18, B19	O	GV _{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV _{DD}	—
MWE	D17	O	GV _{DD}	—
MRAS	F17	O	GV _{DD}	—
MCAS	J16	O	GV _{DD}	—
MCS[0:3]	H16, G16, J15, H15	O	GV _{DD}	—
MCKE[0:1]	E26, E28	O	GV _{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV _{DD}	—
MCK[0:5]	F20, G27, B15, E20, F27, L14	O	GV _{DD}	—
MSYNC_IN	M28	I	GV _{DD}	22
MSYNC_OUT	N28	O	GV _{DD}	22
Local Bus Controller Interface				
LA[27]	U18	O	OV _{DD}	5, 9

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV _{DD}	—
TDI	AG21	I	OV _{DD}	12
TDO	AF19	O	OV _{DD}	11
TMS	AF23	I	OV _{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV _{DD}	12
DFT				
LSSD_MODE	AG19	I	OV _{DD}	20
L1_TSTCLK	AB22	I	OV _{DD}	20
L2_TSTCLK	AG22	I	OV _{DD}	20
$\overline{\text{TEST_SEL0}}$	AH20	I	OV _{DD}	3
TEST_SEL1	AG26	I	OV _{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
AV _{DD1}	AH19	Power for e500 PLL (1.2 V)	AV _{DD1}	—
AV _{DD2}	AH18	Power for CCB PLL (1.2 V)	AV _{DD2}	—
AV _{DD3}	AH17	Power for CPM PLL (1.2 V)	AV _{DD3}	—
AV _{DD4}	AF28	Power for PCI1 PLL (1.2 V)	AV _{DD4}	—
AV _{DD5}	AE28	Power for PCI2 PLL (1.2 V)	AV _{DD5}	—

15.3 e500 Core PLL Ratio

Table 47 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 47.

Table 47. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

15.4 Frequency Options

Table 48 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 48. Frequency Options with Respect to Memory Bus Speeds

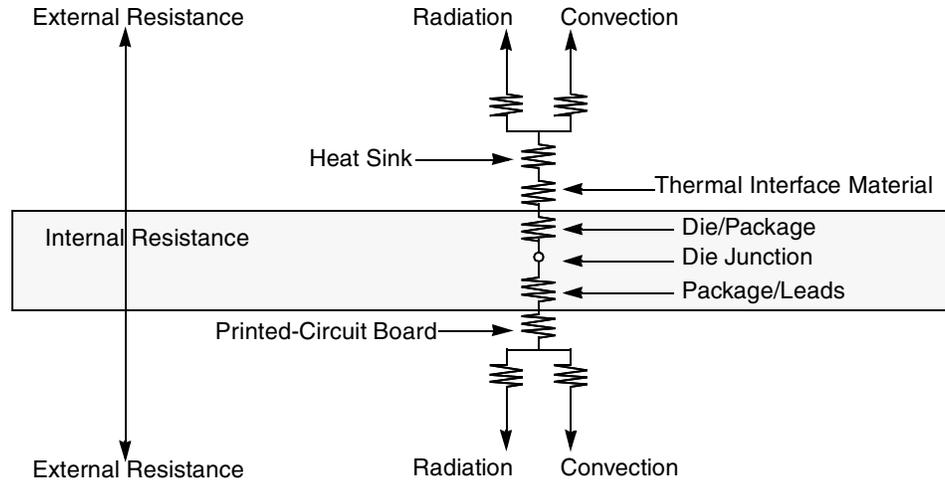
CCB to SYSCLK Ratio	SYSCLK (MHz)								
	17	25	33	42	67	83	100	111	133
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in [Table 49](#), the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

[Figure 45](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, [Figure 46](#) shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see [Figure 42](#)). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

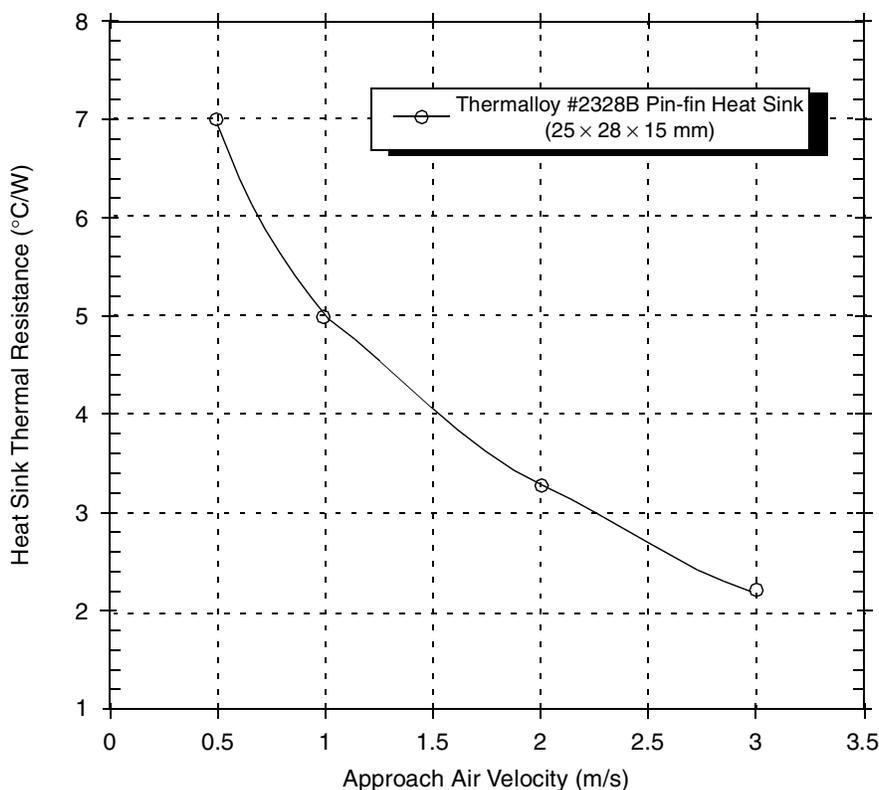


Figure 47. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in [Table 49](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 48](#) and [Figure 49](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 48 and provide exploded views of the plastic fence, heat sink, and spring clip.

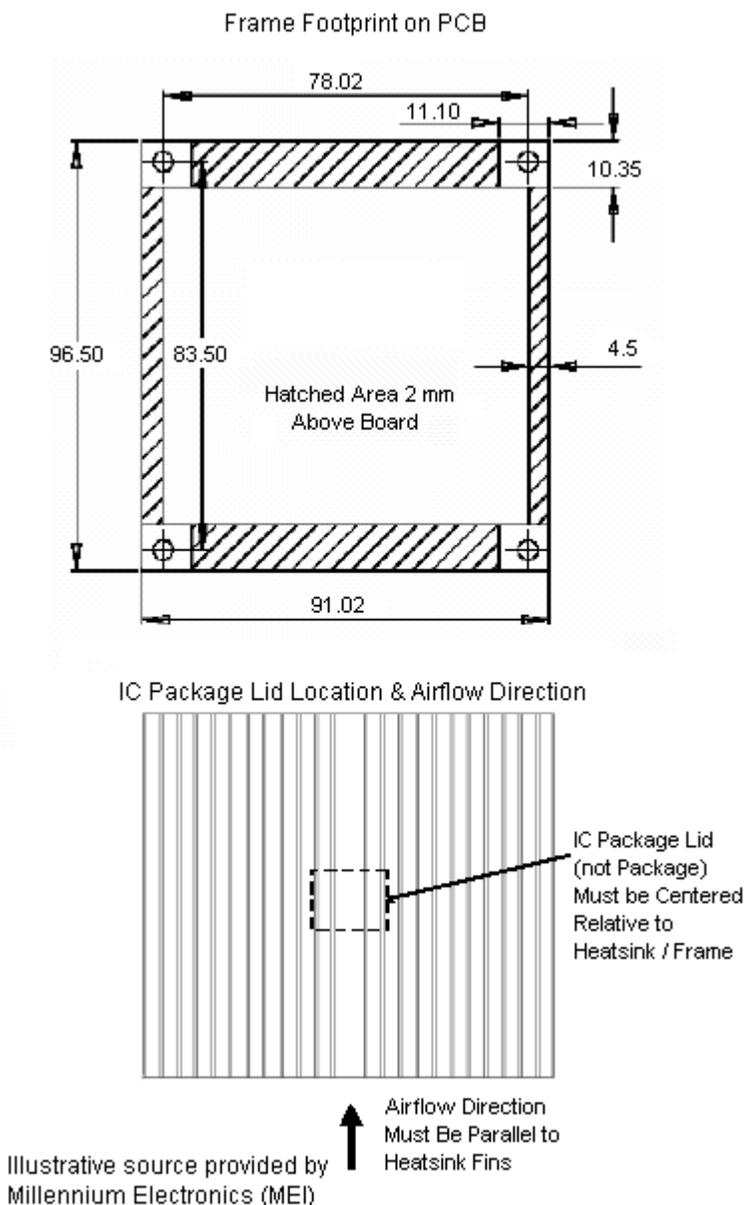


Figure 48. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL (AV_{DD1}) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL (AV_{DD2}) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL (AV_{DD3}) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL (AV_{DD4}) generates the clocking for the first PCI bus.
5. The PCI2 PLL (AV_{DD5}) generates the clock for the second PCI bus.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , AV_{DD3} , AV_{DD4} , and AV_{DD5} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 50](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 52 is common to all known emulators.

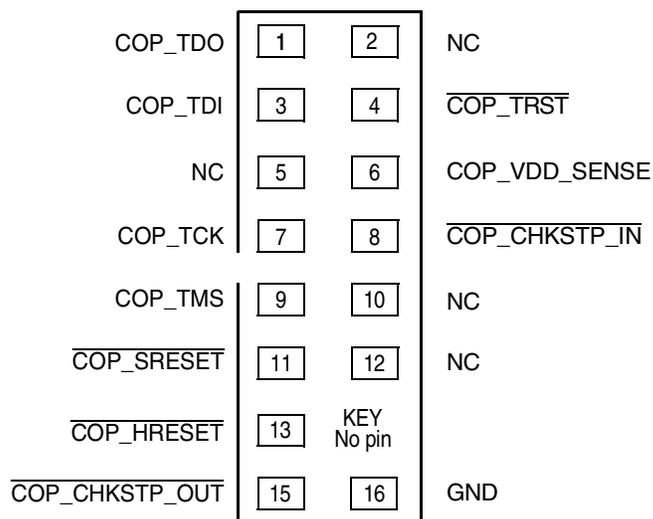


Figure 52. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.