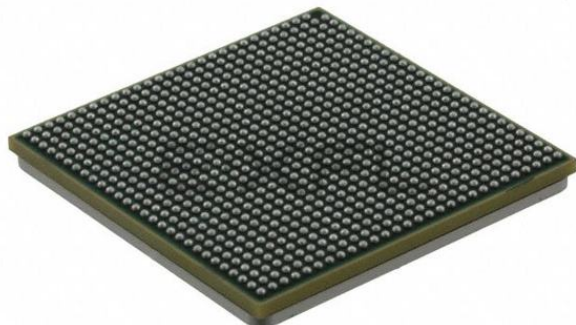




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555pxajd

- Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
- Four global high resolution timers/counters that can generate interrupts
- Supports additional internal interrupt sources
- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- Two I²C controllers (one is contained within the CPM, the other is a stand-alone controller which is not part of the CPM)
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the stand-alone I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (RXD, TXD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Two Three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z AC compliant controllers
 - Support for Ethernet physical interfaces:
 - 10/100/1000 Mbps IEEE 802.3 GMII
 - 10/100 Mbps IEEE 802.3 MII

- 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
 - Three-port crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no-snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI Controllers
 - PCI 2.2 compatible
 - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
 - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes

- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Selectable clock source (SYSCLK or independent PCI_CLK)
- Power management
 - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
 - Supports power save modes: doze, nap, and sleep
 - Employs dynamic power management
 - Selectable clock source (sysclk or independent PCI_CLK)
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8555E. The MPC8555E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.32 0.3 to 1.43 (for 1 GHz only)	V	
PLL supply voltage		AV_{DD}	−0.3 to 1.32 0.3 to 1.43 (for 1 GHz only)	V	
DDR DRAM I/O voltage		GV_{DD}	−0.3 to 3.63	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63 −0.3 to 2.75	V	
CPM, PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to ($LV_{DD} + 0.3$)	V	4, 5
	CPM, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$) ¹	V	5
	PCI	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (M,L,O) V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8555E requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- V_{DD} , AV_{DDn}
- GV_{DD} , LV_{DD} , OV_{DD} (I/O supplies)

4.3 Real Time Clock Timing

Table 8 provides the real time clock (RTC) AC timing specifications.

Table 8. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	2 x t_{CCB_CLK}	—	—	ns	—
RTC clock low time	t_{RTCL}	2 x t_{CCB_CLK}	—	—	ns	—

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8555E. Table 9 provides the RESET initialization AC timing specifications.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$	100	—	μs	—
Minimum assertion time for $\overline{SRESET}$	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{HRESET}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{HRESET}$	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{HRESET}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{HRESET}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8555E. See the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* for more details.

Table 10 provides the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the $SYSCLK \times \text{platform PLL ratio}$.

7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8555E.

Table 17. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB_CLK} / 1048576$	baud	3
Maximum baud rate	$f_{CCB_CLK} / 16$	baud	1, 3
Oversample rate	16	—	2, 3

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
3. Guaranteed by design.

8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 18](#) and [Table 19](#). The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (for example, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}^{5}	–500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}^{6}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ⁴	t_{RGTH}/t_{RGT}^{6}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ³	t_{RGTH}/t_{RGT}^{6}	40	50	60	%
Rise and fall times	$t_{RGTR}^{6,7}, t_{RGTF}^{6,7}$	—	—	0.75	ns

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Guaranteed by characterization.
- Guaranteed by design.
- Signal timings are measured at 0.5 and 2.0 V voltage levels.

Figure 24 through Figure 30 represent the AC timing from Table 33 and Table 34. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 24 shows the FCC internal clock.

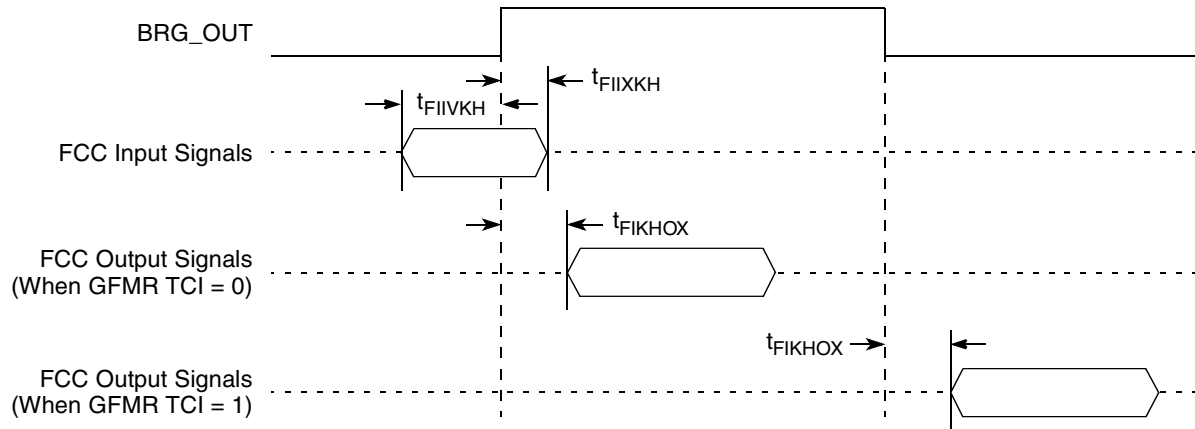


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

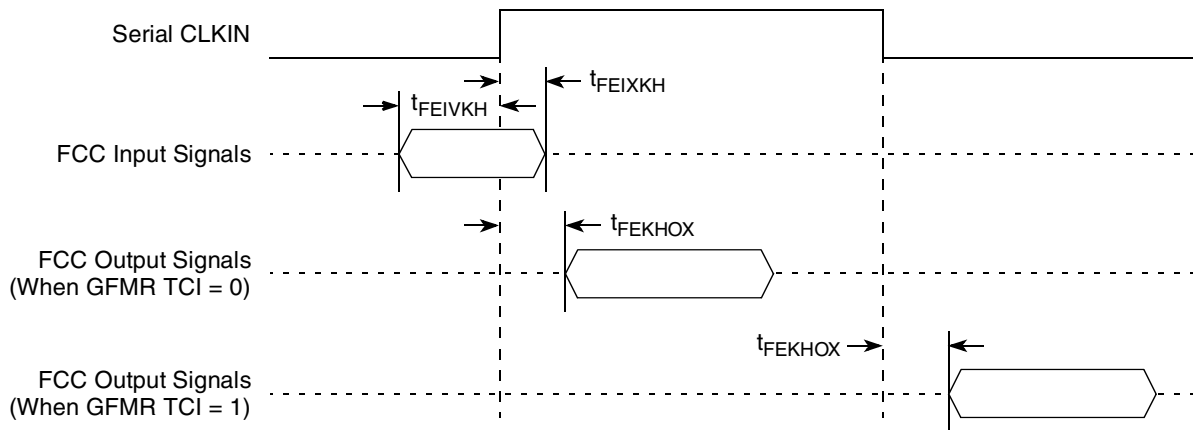


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

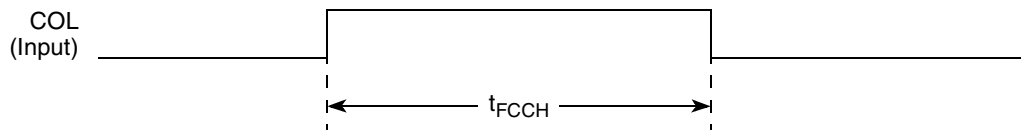
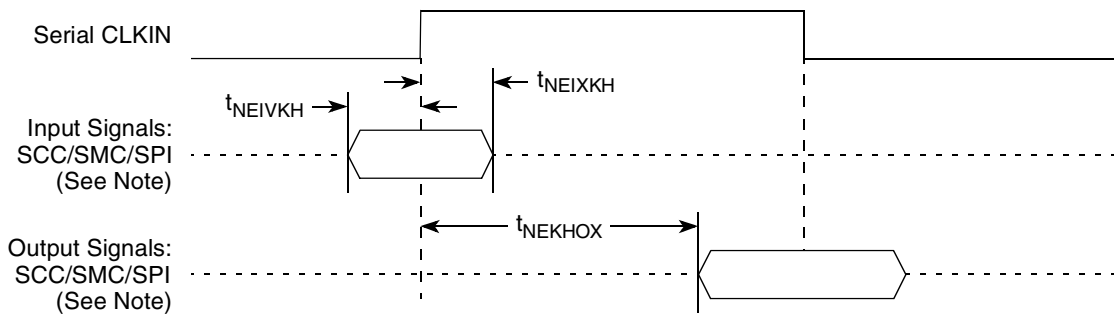


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

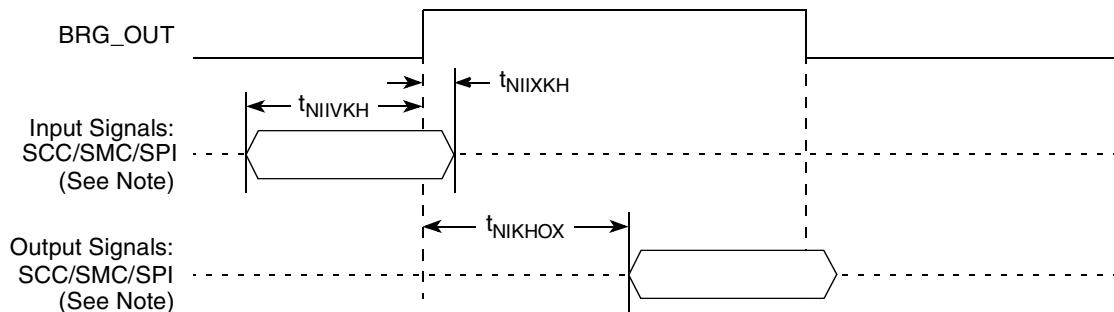
Figure 27 shows the SCC/SMC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SMC/SPI AC Timing External Clock Diagram

Figure 28 shows the SCC/SMC/SPI internal clock.



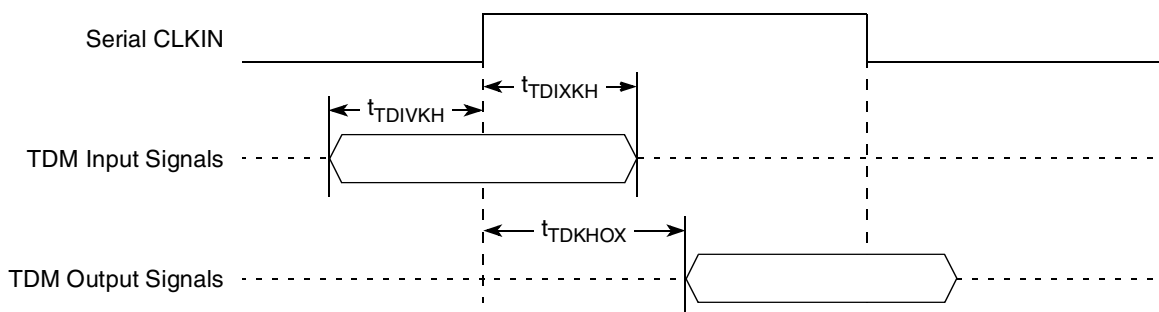
Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SMC/SPI AC Timing Internal Clock Diagram

NOTE

- ¹ SPI AC timings are internal mode when it is master because SPICLK is an output, and external mode when it is slave.
- ² SPI AC timings refer always to SPICLK.

Figure 29 shows TDM input and output signals.



Note: There are 4 possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 29. TDM Signal AC Timing Diagram

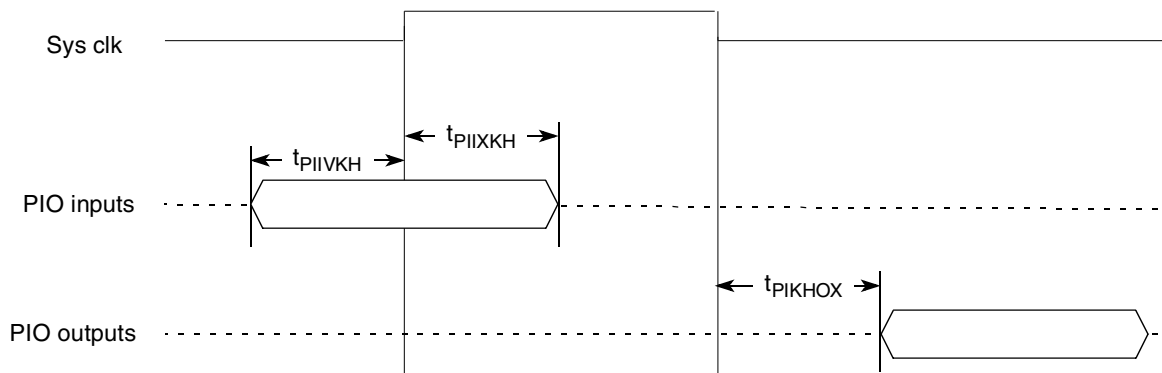


Figure 30. PIO Signal Diagram

10.3 CPM I2C AC Specification

Table 35. I2C Timing

Characteristic	Expression	All Frequencies		Unit
		Min	Max	
SCL clock frequency (slave)	f_{SCL}	0	$F_{MAX}^{(1)}$	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	$1/(2.2 * f_{SCL})$	-	s
Low period of SCL	t_{SCLCH}	$1/(2.2 * f_{SCL})$	-	s
High period of SCL	t_{SCHCL}	$1/(2.2 * f_{SCL})$	-	s
Start condition setup time ²	t_{SCHDL}	$2/(\text{divider} * f_{SCL})$	- ⁽²⁾	s
Start condition hold time ²	t_{SDLCL}	$3/(\text{divider} * f_{SCL})$	-	s
Data hold time ²	t_{SCLDX}	$2/(\text{divider} * f_{SCL})$	-	s
Data setup time ²	t_{SDVCH}	$3/(\text{divider} * f_{SCL})$	-	s
SDA/SCL rise time	t_{SRISE}	-	$1/(10 * f_{SCL})$	s

Figure 16 provides the AC test load for the I²C.

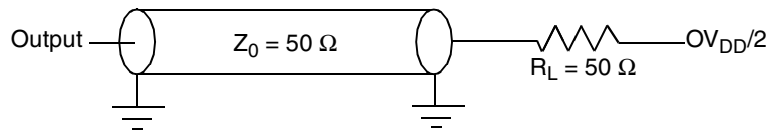


Figure 37. I²C AC Test Load

Figure 38 shows the AC timing diagram for the I²C bus.

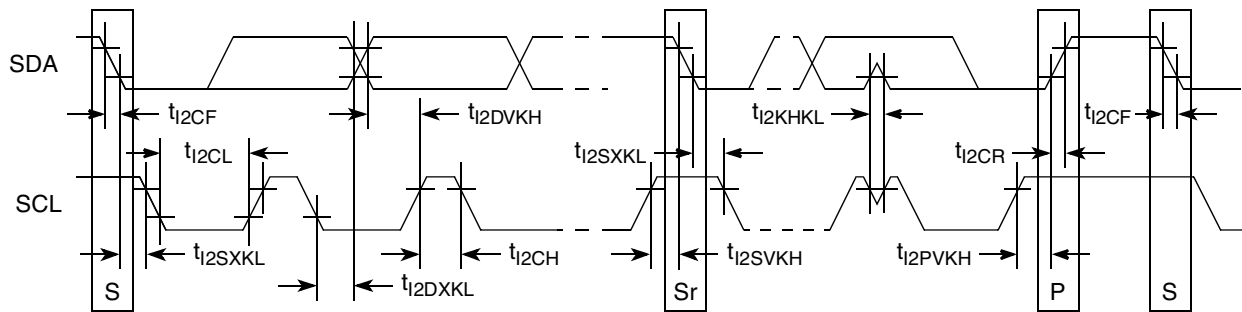


Figure 38. I²C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8555E.

13.1 PCI DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI interface of the MPC8555E.

Table 41. PCI DC Electrical Characteristics ¹

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V _{IH}	V _{OUT} ≥ V _{OH} (min) or V _{OUT} ≤ V _{OL} (max)	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		-0.3	0.8	V
Input current	I _{IN}	V _{IN} ² = 0 V or V _{IN} = V _{DD}	—	±5	μA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = -100 μA	OV _{DD} - 0.2	—	V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 100 μA	—	0.2	V

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AF21	I	OV _{DD}	—
TDI	AG21	I	OV _{DD}	12
TDO	AF19	O	OV _{DD}	11
TMS	AF23	I	OV _{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV _{DD}	12
DFT				
LSSD_MODE	AG19	I	OV _{DD}	20
L1_TSTCLK	AB22	I	OV _{DD}	20
L2_TSTCLK	AG22	I	OV _{DD}	20
$\overline{\text{TEST_SEL0}}$	AH20	I	OV _{DD}	3
TEST_SEL1	AG26	I	OV _{DD}	3
Thermal Management				
THERM0	AG2	—	—	14
THERM1	AH3	—	—	14
Power Management				
ASLEEP	AG18	—	—	9, 18
Power and Ground Signals				
AV _{DD1}	AH19	Power for e500 PLL (1.2 V)	AV _{DD1}	—
AV _{DD2}	AH18	Power for CCB PLL (1.2 V)	AV _{DD2}	—
AV _{DD3}	AH17	Power for CPM PLL (1.2 V)	AV _{DD3}	—
AV _{DD4}	AF28	Power for PCI1 PLL (1.2 V)	AV _{DD4}	—
AV _{DD5}	AE28	Power for PCI2 PLL (1.2 V)	AV _{DD5}	—

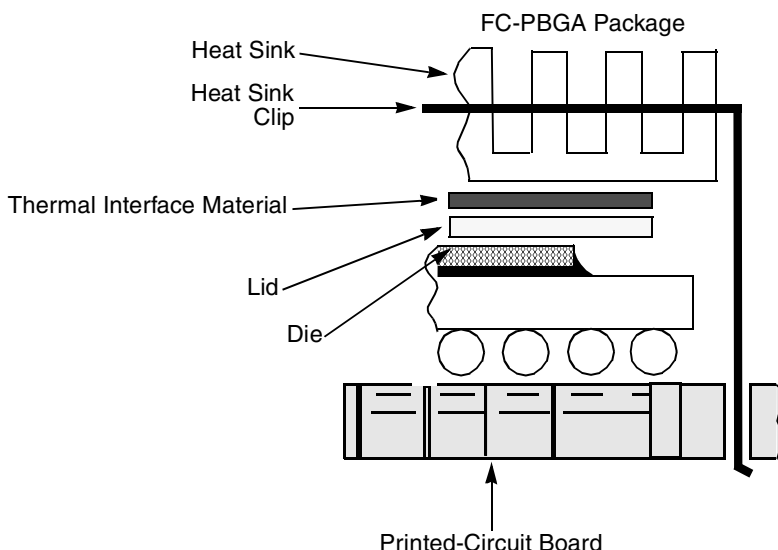


Figure 43. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8555E. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8555E to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8555E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid (11 × 11 × 1 mm)		W/(m × K)
k _x	360	
k _y	360	
k _z	360	
Lid Adhesive—Collapsed resistance (8.7 × 9.3 × 0.05 mm)		
k _z	1.07	
Die (8.7 × 9.3 × 0.75 mm)		
Bump/Underfill—Collapsed resistance (8.7 × 9.3 × 0.07 mm)		
k _z	4.4	
Substrate and Solder Balls (25 × 25 × 1.6 mm)		
k _x	14.2	
k _y	14.2	
k _z	1.2	

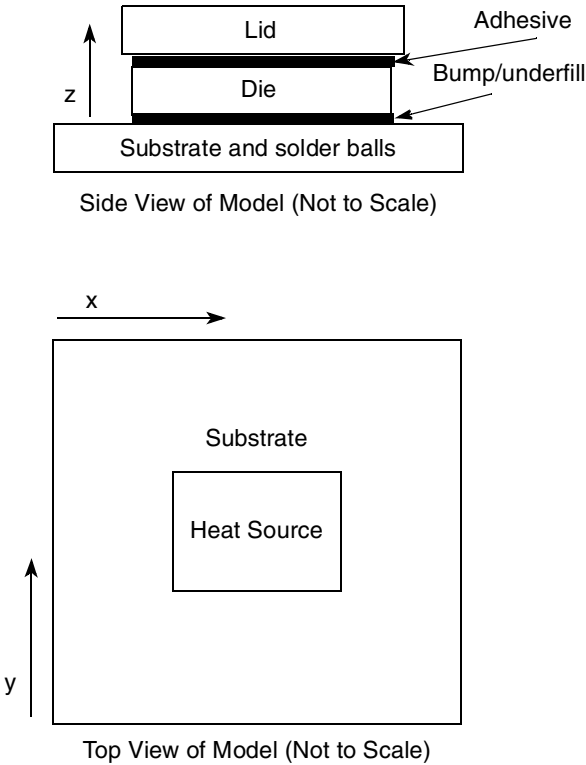


Figure 44. MPC8555E Thermal Model

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL (AV_{DD1}) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL (AV_{DD2}) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL (AV_{DD3}) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL (AV_{DD4}) generates the clocking for the first PCI bus.
5. The PCI2 PLL (AV_{DD5}) generates the clock for the second PCI bus.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , AV_{DD3} , AV_{DD4} , and AV_{DD5} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 50](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

17.6 Configuration Pin Multiplexing

The MPC8555E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8555E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 53](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 52 is common to all known emulators.

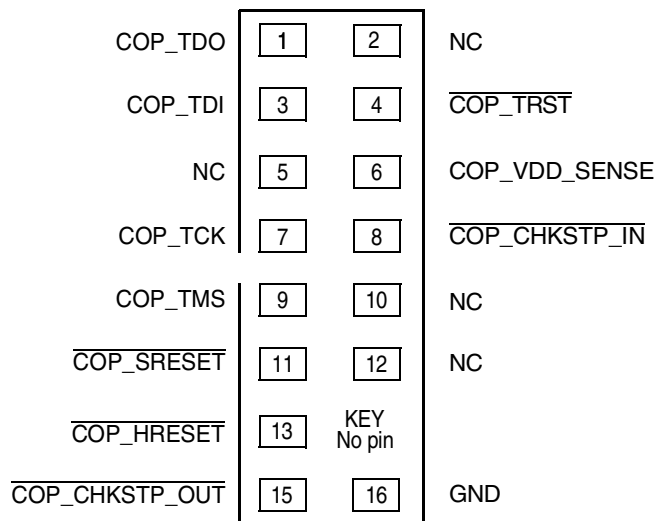


Figure 52. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 53](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

18 Document Revision History

Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

Rev. No.	Date	Substantive Change(s)
4.2	1/2008	Added "Note: Rise/Fall Time on CPM Input Pins" and following note text to Section 10.2, "CPM AC Timing Specifications."
4.1	7/2007	Inserted Figure 3 , "Maximum AC Waveforms on PCI interface for 3.3-V Signaling."
4	12/2006	Updated Section 2.1.2, "Power Sequencing." Updated back page information.
3.2	11/2006	Updated Section 2.1.2, "Power Sequencing." Replaced Section 17.8, "JTAG Configuration Signals."
3.1	10/2005	Added footnote 2 about junction temperature in Table 4 . Added max. power values for 1000 MHz core frequency in Table 4 . Removed Figure 3 , "Maximum AC Waveforms on PCI Interface for 3.3-V Signaling." Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30 . Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values in Table 30 . Added note 3 to $t_{LBKHOV1}$ in Table 30 . Modified note 3 in Table 30 and Table 31 . Added note 3 to $t_{LBKLOV1}$ in Table 31 . Modified values for t_{LBKHKT} , $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31 . Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21 . Modified note for signal CLK_OUT in Table 43 . PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43 . Added column for Encryption Acceleration in Table 52 .
3	8/2005	Modified max. power values in Table 4 . Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43 .
2	8/2005	Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31 . Added note 2 in Table 7 . Modified min and max values for t_{DDKHMP} in Table 14 .
1	6/2005	Changed V_{DD} to O_{VDD} for the supply voltage Ethernet management interface in Table 27 . Modified footnote 4 and changed typical power for the 1000 MHz core frequency in Table 4 . Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31 .
0	6/2005	Initial release.

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