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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

| | |
|---------------------------------|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555pxaqf |

- 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1000 Mbps RGMII/RTBI
- Full- and half-duplex support
- Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
- 9.6-Kbyte jumbo frame support
- RMON statistics support
- 2-Kbyte internal transmit and receive FIFOs
- MII management interface for control and status
- Programmable CRC generation and checking
- OCeaN switch fabric
 - Three-port crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no-snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI Controllers
 - PCI 2.2 compatible
 - One 64-bit or two 32-bit PCI ports supported at 16 to 66 MHz
 - Host and agent mode support, 64-bit PCI port can be host or agent, if two 32-bit ports, only one can be an agent
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|--|------------|--|------|-------|
| Core supply voltage | | V_{DD} | −0.3 to 1.32 0.3 to 1.43 (for 1 GHz only) | V | |
| PLL supply voltage | | AV_{DD} | −0.3 to 1.32 0.3 to 1.43 (for 1 GHz only) | V | |
| DDR DRAM I/O voltage | | GV_{DD} | −0.3 to 3.63 | V | |
| Three-speed Ethernet I/O, MII management voltage | | LV_{DD} | −0.3 to 3.63 −0.3 to 2.75 | V | |
| CPM, PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage | | OV_{DD} | −0.3 to 3.63 | V | 3 |
| Input voltage | DDR DRAM signals | MV_{IN} | −0.3 to ($GV_{DD} + 0.3$) | V | 2, 5 |
| | DDR DRAM reference | MV_{REF} | −0.3 to ($GV_{DD} + 0.3$) | V | 2, 5 |
| | Three-speed Ethernet signals | LV_{IN} | −0.3 to ($LV_{DD} + 0.3$) | V | 4, 5 |
| | CPM, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals | OV_{IN} | −0.3 to ($OV_{DD} + 0.3$) ¹ | V | 5 |
| | PCI | OV_{IN} | −0.3 to ($OV_{DD} + 0.3$) | V | 6 |
| Storage temperature range | | T_{STG} | −55 to 150 | °C | |

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (M,L,O) V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8555E requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- V_{DD} , AV_{DDn}
- GV_{DD} , LV_{DD} , OV_{DD} (I/O supplies)

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8555E.

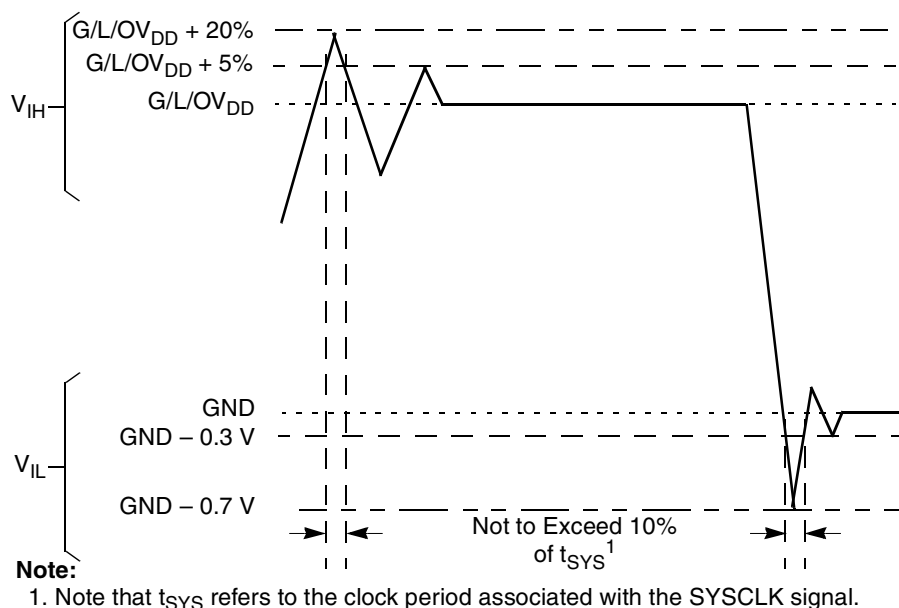


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8555E core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

4 Clock Timing

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8555E.

Table 6. SYSCLK AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---------------------------|------------------------------------|-----|---------|---------|------|-------|
| SYSCLK frequency | f_{SYSCLK} | — | — | 166 | MHz | 1 |
| SYSCLK cycle time | t_{SYSCLK} | 6.0 | — | — | ns | — |
| SYSCLK rise and fall time | $t_{\text{KH}}, t_{\text{KL}}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| SYSCLK duty cycle | $t_{\text{KHK}}/t_{\text{SYSCLK}}$ | 40 | — | 60 | % | 3 |
| SYSCLK jitter | — | — | — | +/- 150 | ps | 4, 5 |

Notes:

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- For spread spectrum clocking, guidelines are $\pm 1\%$ of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8555E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|--|------------------------------------|----------|---------|----------|------|-------|
| EC_GTX_CLK125 frequency | f_{G125} | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | t_{G125} | — | 8 | — | ns | — |
| EC_GTX_CLK125 rise time | t_{G125R} | — | — | 1.0 | ns | 1 |
| EC_GTX_CLK125 fall time | t_{G125F} | — | — | 1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI | $t_{\text{G125H}}/t_{\text{G125}}$ | 45 47 | — | 55 53 | % | 1, 2 |

Notes:

- Timing is guaranteed by design and characterization.
- EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 22 provides the MII transmit AC timing specifications.

Table 22. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V \pm 5%.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|---|-------------------------------|-----|-----|-----|------|
| TX_CLK clock period 10 Mbps | t_{MTX}^2 | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | t_{MTX} | — | 40 | — | ns |
| TX_CLK duty cycle | t_{MTXH}/t_{MTX} | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | t_{MTKHDx} | 1 | 5 | 15 | ns |
| TX_CLK data clock rise and fall time | t_{MTXR} , $t_{MTXF}^{2,3}$ | 1.0 | — | 4.0 | ns |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

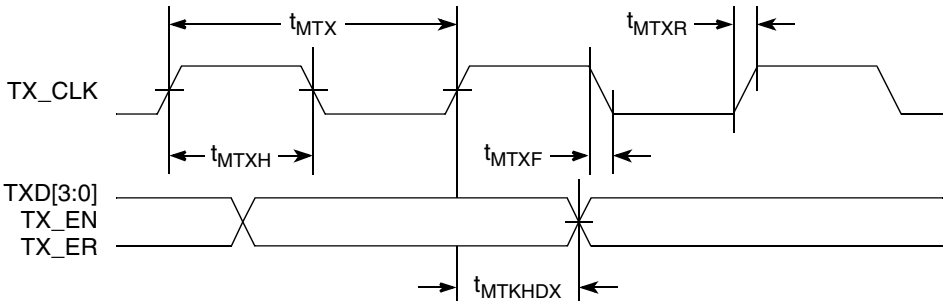


Figure 10. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 23 provides the MII receive AC timing specifications.

Table 23. MII Receive AC Timing Specifications

At recommended operating conditions with V_{DD} of $3.3\text{ V} \pm 5\%$.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|---|----------------------------|------|-----|-----|------|
| RX_CLK clock period 10 Mbps | t_{MRX}^2 | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | t_{MRX} | — | 40 | — | ns |
| RX_CLK duty cycle | t_{MRXH}/t_{MRX} | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | t_{MRDVKH} | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | t_{MRDXKH} | 10.0 | — | — | ns |
| RX_CLK clock rise and fall time | $t_{MRXR}, t_{MRXF}^{2,3}$ | 1.0 | — | 4.0 | ns |

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

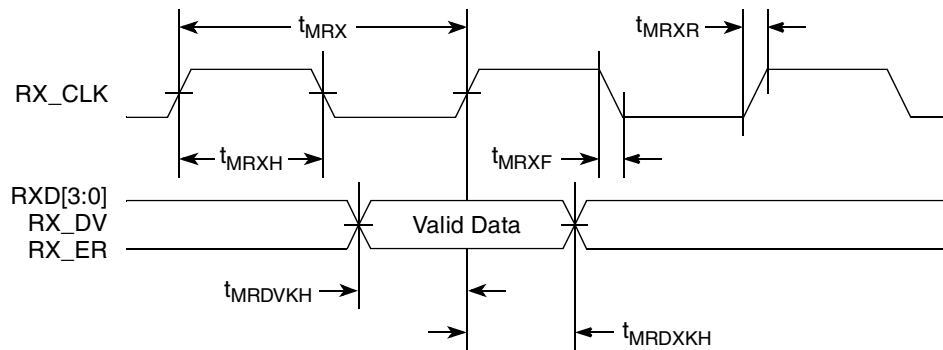


Figure 11. MII Receive AC Timing Diagram

Table 27. MII Management DC Electrical Characteristics (continued)

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|--------------------|----------|------------------------|----------------------------|------|-----|---------------|
| Input high current | I_{IH} | $LV_{DD} = \text{Max}$ | $V_{IN}^1 = 2.1 \text{ V}$ | — | 40 | μA |
| Input low current | I_{IL} | $LV_{DD} = \text{Max}$ | $V_{IN} = 0.5 \text{ V}$ | −600 | — | μA |

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is $3.3 \text{ V} \pm 5\%$.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit | Notes |
|----------------------------|---------------------|-------|-----|--------------------------------|------|-------|
| MDC frequency | f_{MDC} | 0.893 | — | 10.4 | MHz | 2 |
| MDC period | t_{MDC} | 96 | — | 1120 | ns | |
| MDC clock pulse width high | t_{MDCH} | 32 | — | — | ns | |
| MDC to MDIO valid | t_{MDKHDV} | | | $2 \cdot [1/(f_{ccb_clk}/8)]$ | ns | 3 |
| MDC to MDIO delay | t_{MDKHDX} | 10 | — | $2 \cdot [1/(f_{ccb_clk}/8)]$ | ns | 3 |
| MDIO to MDC setup time | t_{MDDVKH} | 5 | — | — | ns | |
| MDIO to MDC hold time | t_{MDDXKH} | 0 | — | — | ns | |
| MDC rise time | t_{MDCR} | — | — | 10 | ns | |
| MDC fall time | t_{MDHF} | — | — | 10 | ns | |

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the system clock speed (that is, for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
- This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
- Guaranteed by design.

Figure 15 shows the MII management AC timing diagram.

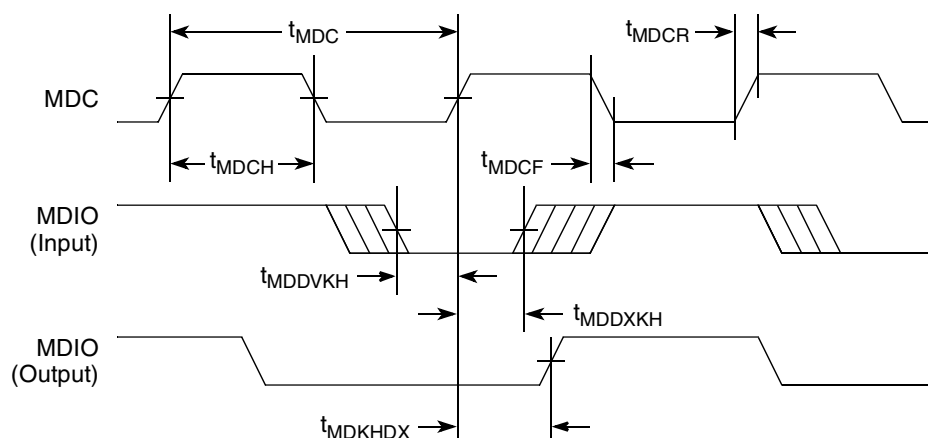


Figure 15. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8555E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---------------------------|----------|---|-----------------|-----------------|---------------|
| High-level input voltage | V_{IH} | $V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$ | 2 | $OV_{DD} + 0.3$ | V |
| Low-level input voltage | V_{IL} | | -0.3 | 0.8 | V |
| Input current | I_{IN} | $V_{IN}^1 = 0 \text{ V or } V_{IN} = V_{DD}$ | — | ± 5 | μA |
| High-level output voltage | V_{OH} | $OV_{DD} = \text{min, } I_{OH} = -2\text{mA}$ | $OV_{DD} - 0.2$ | — | V |
| Low-level output voltage | V_{OL} | $OV_{DD} = \text{min, } I_{OL} = 2\text{mA}$ | — | 0.2 | V |

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Table 31. Local Bus General Timing Parameters—DLL Bypassed (continued)

| Parameter | Configuration ⁷ | Symbol ¹ | Min | Max | Unit | Notes |
|--|---|----------------------|------|-----|------|-------|
| Local bus clock to address valid for LAD | $\overline{\text{LWE}}[0:1] = 00$ | t_{LBKLOV3} | — | 0.8 | ns | 3 |
| | $\overline{\text{LWE}}[0:1] = 11$ (default) | | | 2.3 | | |
| Output hold from local bus clock (except LAD/LDP and LALE) | $\overline{\text{LWE}}[0:1] = 00$ | t_{LBKLOX1} | –2.7 | — | ns | 3 |
| | $\overline{\text{LWE}}[0:1] = 11$ (default) | | –1.8 | | | |
| Output hold from local bus clock for LAD/LDP | $\overline{\text{LWE}}[0:1] = 00$ | t_{LBKLOX2} | –2.7 | — | ns | 3 |
| | $\overline{\text{LWE}}[0:1] = 11$ (default) | | –1.8 | | | |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $\overline{\text{LWE}}[0:1] = 00$ | t_{LBKLOZ1} | — | 1.0 | ns | 5 |
| | $\overline{\text{LWE}}[0:1] = 11$ (default) | | | 2.4 | | |
| Local bus clock to output high impedance for LAD/LDP | $\overline{\text{LWE}}[0:1] = 00$ | t_{LBKLOZ2} | — | 1.0 | ns | 5 |
| | $\overline{\text{LWE}}[0:1] = 11$ (default) | | | 2.4 | | |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. All signals are measured from $\text{OV}_{\text{DD}}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times \text{OV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins $\overline{\text{LWE}}[0:1]$.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{OV}_{\text{DD}}/2$.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 16 provides the AC test load for the local bus.

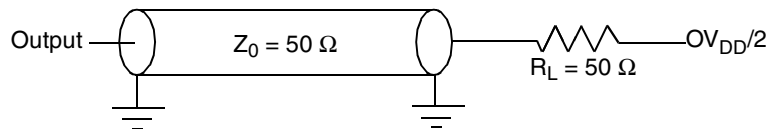

Figure 16. Local Bus C Test Load

Figure 24 through Figure 30 represent the AC timing from Table 33 and Table 34. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 24 shows the FCC internal clock.

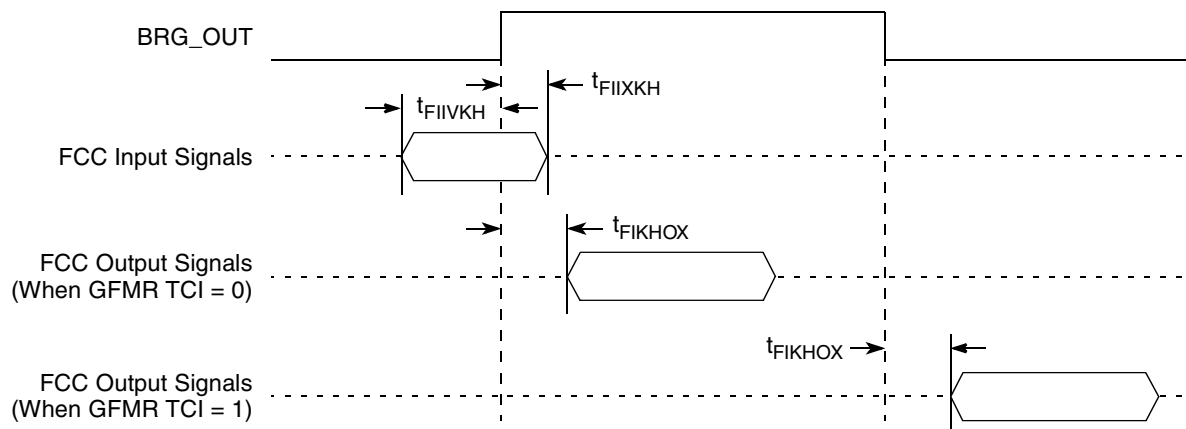


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

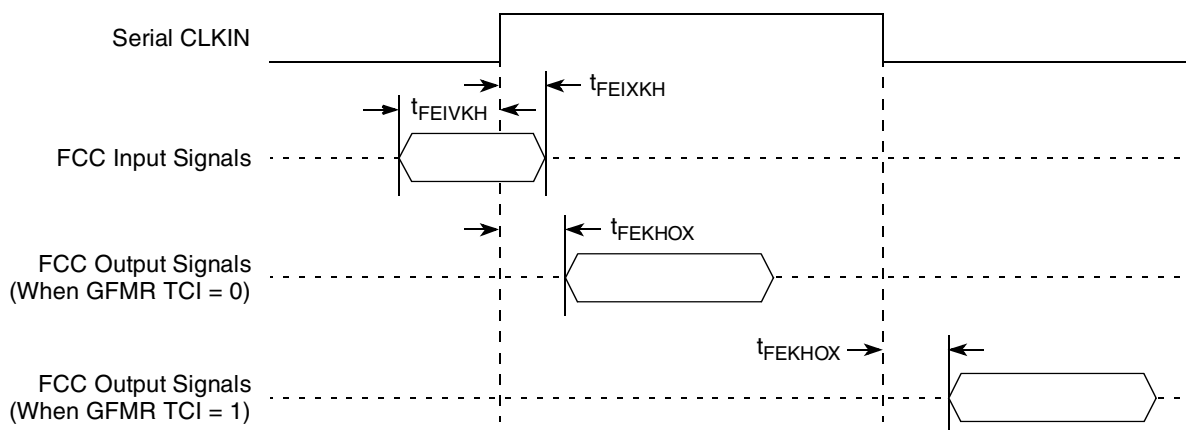


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

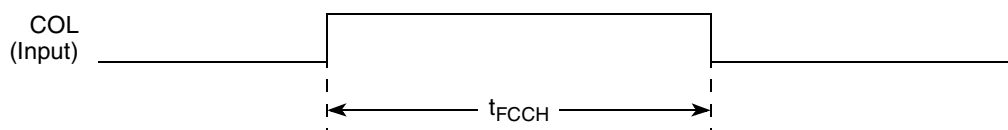


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

Table 43. MPC8555E Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---------------------------------------|--|----------|------------------|-------|
| PCI2_GNT[1:4] | AD18, AE18, AE19, AD19 | O | OV _{DD} | 5, 9 |
| PCI2_IDSEL | AC22 | I | OV _{DD} | — |
| PCI2_IRDY | AD20 | I/O | OV _{DD} | 2 |
| PCI2_PERR | AC20 | I/O | OV _{DD} | 2 |
| PCI2_REQ[0] | AD21 | I/O | OV _{DD} | — |
| PCI2_REQ[1:4] | AE21, AD22, AE22, AC23 | I | OV _{DD} | — |
| PCI2_SERR | AE20 | I/O | OV _{DD} | 2,4 |
| PCI2_STOP | AC21 | I/O | OV _{DD} | 2 |
| PCI2_TRDY | AC19 | I/O | OV _{DD} | 2 |
| DDR SDRAM Memory Interface | | | | |
| MDQ[0:63] | M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12 | I/O | GV _{DD} | — |
| MECC[0:7] | N20, M20, L19, E19, C21, A21, G19, A19 | I/O | GV _{DD} | — |
| MDM[0:8] | L24, H28, F24, L21, E18, E16, G14, B13, M19 | O | GV _{DD} | — |
| MDQS[0:8] | L26, J25, D25, A22, H18, F16, F14, C13, C20 | I/O | GV _{DD} | — |
| MBA[0:1] | B18, B19 | O | GV _{DD} | — |
| MA[0:14] | N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13 | O | GV _{DD} | — |
| MWE | D17 | O | GV _{DD} | — |
| MRAS | F17 | O | GV _{DD} | — |
| MCAS | J16 | O | GV _{DD} | — |
| MCS[0:3] | H16, G16, J15, H15 | O | GV _{DD} | — |
| MCKE[0:1] | E26, E28 | O | GV _{DD} | 11 |
| MCK[0:5] | J20, H25, A15, D20, F28, K14 | O | GV _{DD} | — |
| MCK[0:5] | F20, G27, B15, E20, F27, L14 | O | GV _{DD} | — |
| MSYNC_IN | M28 | I | GV _{DD} | 22 |
| MSYNC_OUT | N28 | O | GV _{DD} | 22 |
| Local Bus Controller Interface | | | | |
| LA[27] | U18 | O | OV _{DD} | 5, 9 |

Table 43. MPC8555E Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---------------------------------|----------------------------------|----------|------------------|----------|
| TSEC2_CRS | D9 | I | LV _{DD} | — |
| TSEC2_COL | F8 | I | LV _{DD} | — |
| TSEC2_RXD[7:0] | F9, E9, C9, B9, A9, H9, G10, F10 | I | LV _{DD} | — |
| TSEC2_RX_DV | H8 | I | LV _{DD} | — |
| TSEC2_RX_ER | A8 | I | LV _{DD} | — |
| TSEC2_RX_CLK | E10 | I | LV _{DD} | — |
| DUART | | | | |
| UART_CTS[0,1] | Y2, Y3 | I | OV _{DD} | — |
| UART_RTS[0,1] | Y1, AD1 | O | OV _{DD} | — |
| UART_SIN[0,1] | P11, AD5 | I | OV _{DD} | — |
| UART_SOUT[0,1] | N6, AD2 | O | OV _{DD} | — |
| I²C interface | | | | |
| IIC_SDA | AH22 | I/O | OV _{DD} | 4, 19 |
| IIC_SCL | AH23 | I/O | OV _{DD} | 4, 19 |
| System Control | | | | |
| HRESET | AH16 | I | OV _{DD} | — |
| HRESET_REQ | AG20 | O | OV _{DD} | 18 |
| SRESET | AF20 | I | OV _{DD} | — |
| CKSTP_IN | M11 | I | OV _{DD} | — |
| CKSTP_OUT | G1 | O | OV _{DD} | 2, 4 |
| Debug | | | | |
| TRIG_IN | N12 | I | OV _{DD} | — |
| TRIG_OUT/READY | G2 | O | OV _{DD} | 6, 9, 18 |
| MSRCID[0:1] | J9, G3 | O | OV _{DD} | 5, 6, 9 |
| MSRCID[2:3] | F3, F5 | O | OV _{DD} | 6 |
| MSRCID4 | F2 | O | OV _{DD} | 6 |
| MDVAL | F4 | O | OV _{DD} | 6 |
| Clock | | | | |
| SYSCLK | AH21 | I | OV _{DD} | — |
| RTC | AB23 | I | OV _{DD} | — |
| CLK_OUT | AF22 | O | OV _{DD} | — |

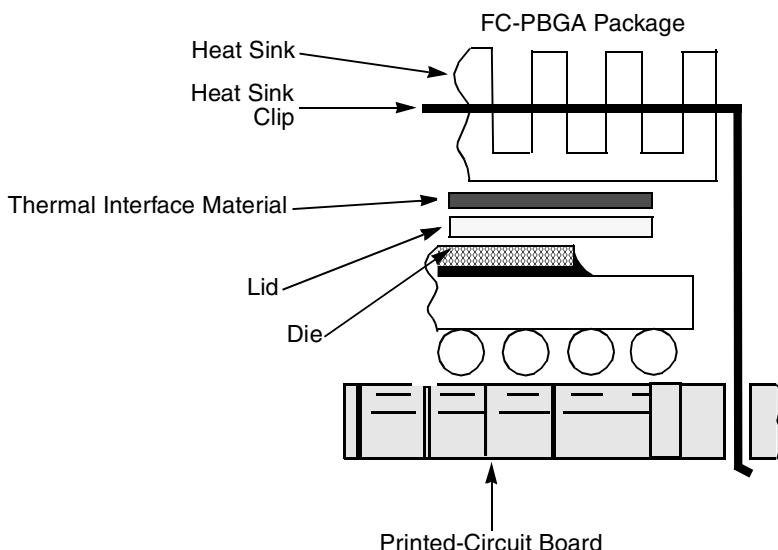


Figure 43. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8555E. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 49, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 45 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

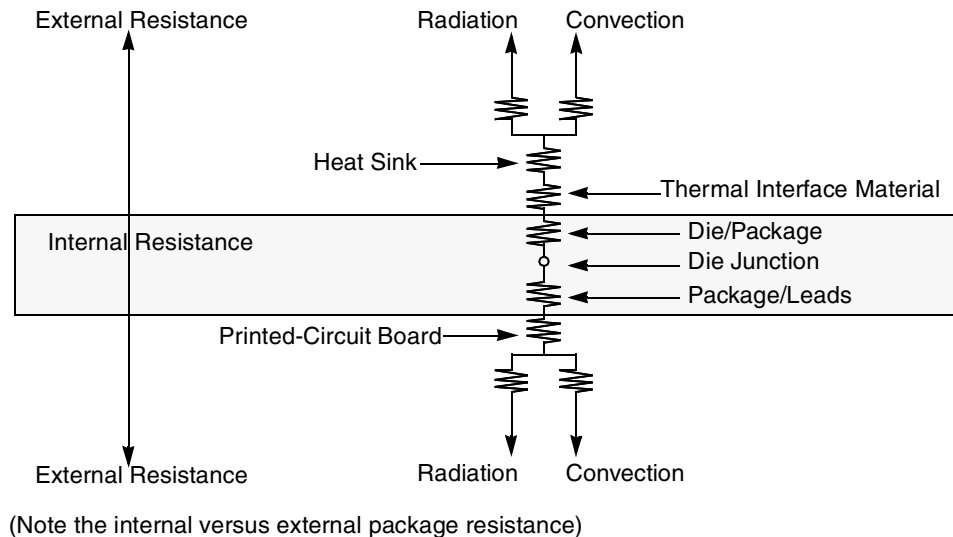


Figure 45. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 46 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 42). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink,

Chanhassen, MN 55317
 Internet: www.bergquistcompany.com
 Thermagon Inc.
 4707 Detroit Ave.
 Cleveland, OH 44102
 Internet: www.thermagon.com

888-246-9050

16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device. See [Table 4](#) and [Table 5](#).

During operation the die-junction temperatures (T_J) should be maintained within the range specified in [Table 2](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. For the purposes of this example, the θ_{JC} value given in [Table 49](#) that includes the thermal grease interface and is documented in note 4 is used. If a thermal pad is used, θ_{INT} must be added.

Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package $\theta_{JC} = 0.96$, and a power consumption (P_D) of 8.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + \theta_{SA}) \times 8.0 \text{ W}$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in [Figure 47](#).

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

$$T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.96^\circ\text{C/W} + 3.3^\circ\text{C/W}) \times 8.0 \text{ W},$$

resulting in a die-junction temperature of approximately 69°C which is well within the maximum operating temperature of the component.

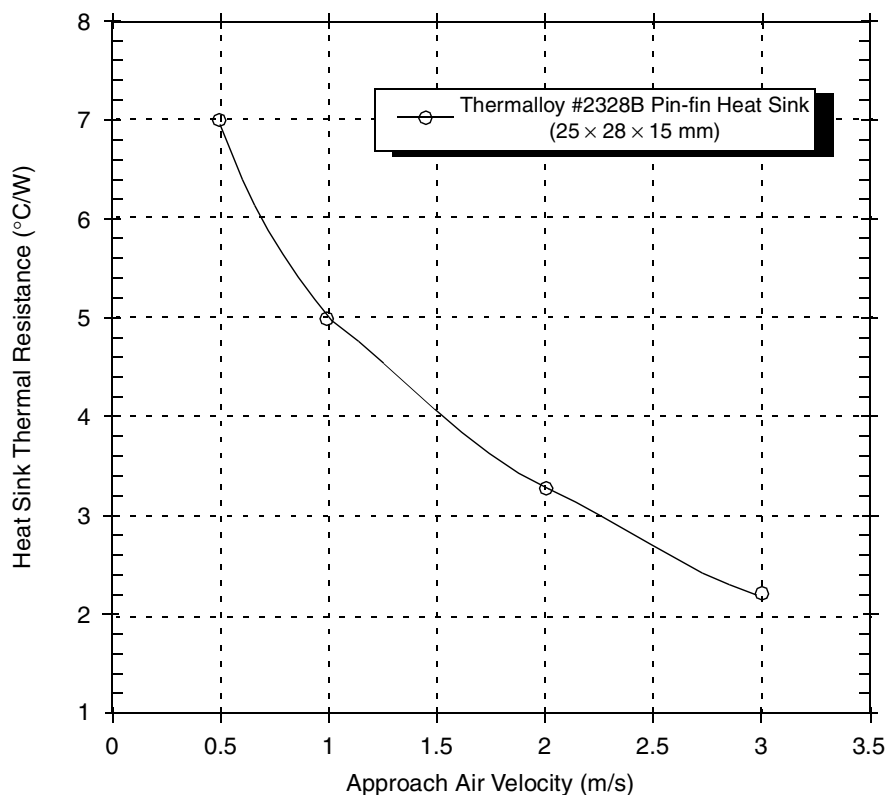


Figure 47. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in Table 49 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 48 and Figure 49. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8555E.

17.1 System Clocking

The MPC8555E includes five PLLs.

1. The platform PLL (AV_{DD1}) generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 15.2, “Platform/System PLL Ratio.”](#)
2. The e500 Core PLL (AV_{DD2}) generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 15.3, “e500 Core PLL Ratio.”](#)
3. The CPM PLL (AV_{DD3}) is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.
4. The PCI1 PLL (AV_{DD4}) generates the clocking for the first PCI bus.
5. The PCI2 PLL (AV_{DD5}) generates the clock for the second PCI bus.

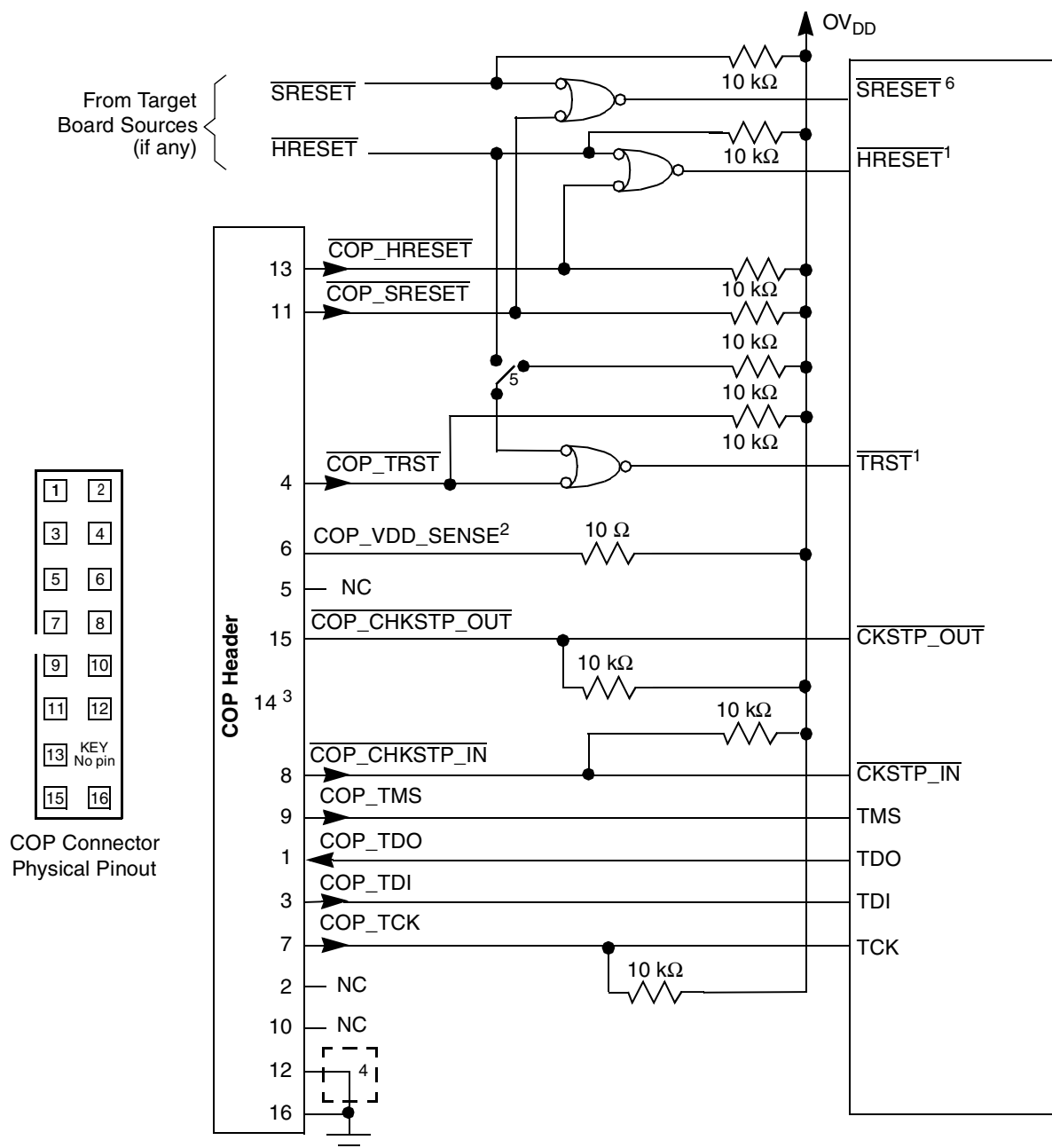
17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , AV_{DD3} , AV_{DD4} , and AV_{DD5} respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 50](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

18 Document Revision History

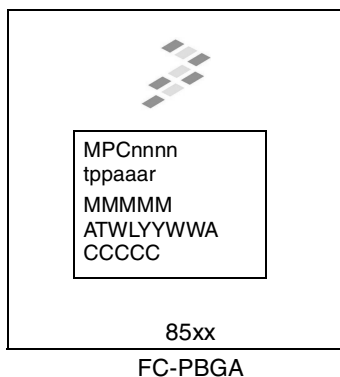
Table 51 provides a revision history for this hardware specification.

Table 51. Document Revision History

| Rev. No. | Date | Substantive Change(s) |
|----------|---------|--|
| 4.2 | 1/2008 | Added "Note: Rise/Fall Time on CPM Input Pins" and following note text to Section 10.2, "CPM AC Timing Specifications." |
| 4.1 | 7/2007 | Inserted Figure 3 , "Maximum AC Waveforms on PCI interface for 3.3-V Signaling." |
| 4 | 12/2006 | Updated Section 2.1.2, "Power Sequencing." Updated back page information. |
| 3.2 | 11/2006 | Updated Section 2.1.2, "Power Sequencing." Replaced Section 17.8, "JTAG Configuration Signals." |
| 3.1 | 10/2005 | Added footnote 2 about junction temperature in Table 4 . Added max. power values for 1000 MHz core frequency in Table 4 . Removed Figure 3 , "Maximum AC Waveforms on PCI Interface for 3.3-V Signaling." Modified note to $t_{LBKSKEW}$ from 8 to 9 in Table 30 . Changed $t_{LBKHOZ1}$ and $t_{LBKHOV2}$ values in Table 30 . Added note 3 to $t_{LBKHOV1}$ in Table 30 . Modified note 3 in Table 30 and Table 31 . Added note 3 to $t_{LBKLOV1}$ in Table 31 . Modified values for t_{LBKHKT} , $t_{LBKLOV1}$, $t_{LBKLOV2}$, $t_{LBKLOV3}$, $t_{LBKLOZ1}$, and $t_{LBKLOZ2}$ in Table 31 . Changed Input Signals: LAD[0:31]/LDP[0:3] in Figure 21 . Modified note for signal CLK_OUT in Table 43 . PCI1_CLK and PCI2_CLK changed from I/O to I in Table 43 . Added column for Encryption Acceleration in Table 52 . |
| 3 | 8/2005 | Modified max. power values in Table 4 . Modified notes for signals TSEC1_TXD[3:0], TSEC2_TXD[3:0], TRIG_OUT/READY, MSRCID4, CLK_OUT, and MDVAL in Table 43 . |
| 2 | 8/2005 | Previous revision's history listed incorrect cross references. Table 2 is now correctly listed as Table 27 and Table 38 is now listed as Table 31 . Added note 2 in Table 7 . Modified min and max values for t_{DDKHMP} in Table 14 . |
| 1 | 6/2005 | Changed V_{DD} to V_{DD} for the supply voltage Ethernet management interface in Table 27 . Modified footnote 4 and changed typical power for the 1000 MHz core frequency in Table 4 . Corrected symbols for body rows 9–15, effectively changing them from a high state to a low state in Table 31 . |
| 0 | 6/2005 | Initial release. |

19.2 Part Marking

Parts are marked as the example shown in [Figure 54](#).



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device