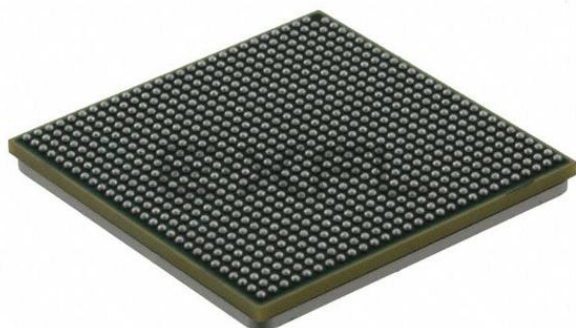




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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8555vtaqf

1 Overview

The following section provides a high-level overview of the MPC8555E features. Figure 1 shows the major functional units within the MPC8555E.

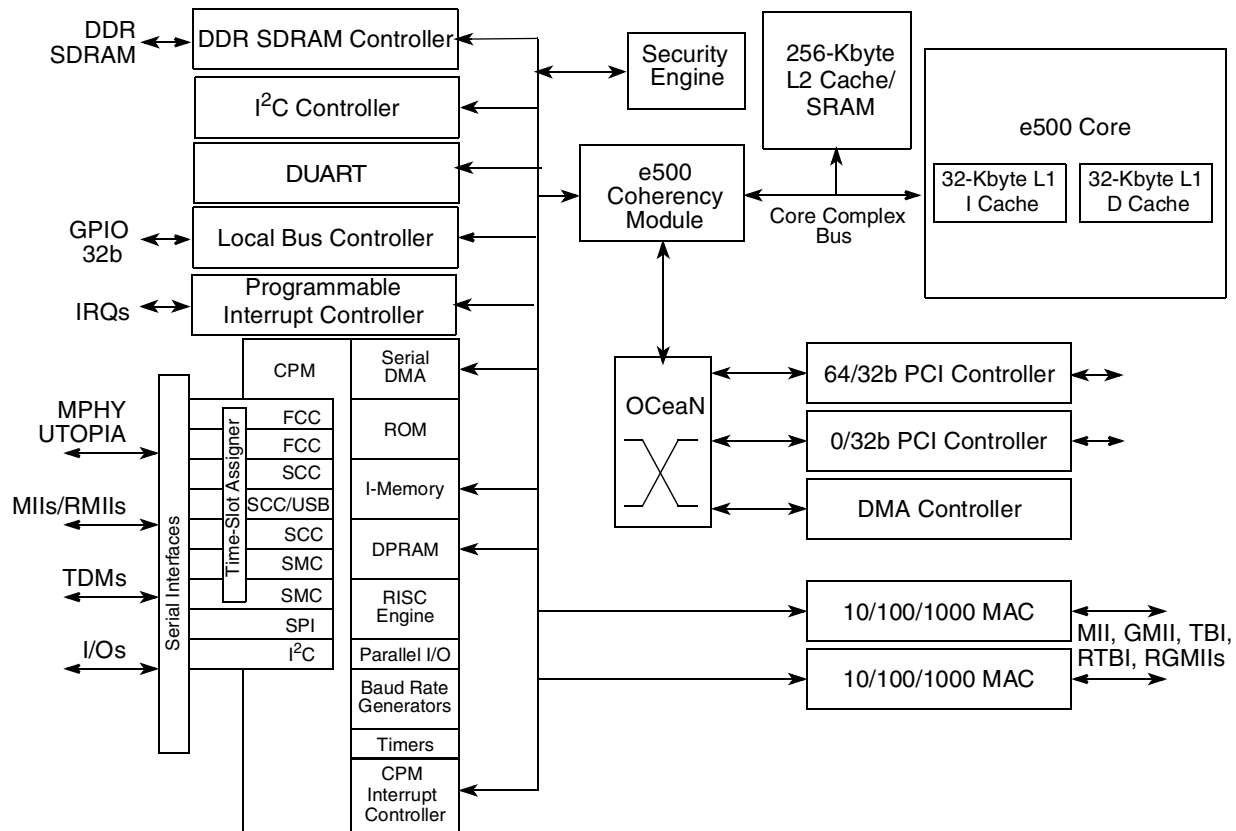


Figure 1. MPC8555E Block Diagram

1.1 Key Features

The following lists an overview of the MPC8555E feature set.

- Embedded e500 Book E-compatible core
 - High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
 - Dual-issue superscalar, 7-stage pipeline design
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
 - Lockable L1 caches—entire cache or on a per-line basis
 - Separate locking for instructions and data
 - Single-precision floating-point operations
 - Memory management unit especially designed for embedded applications
 - Enhanced hardware and software debug support
 - Dynamic power management
 - Performance monitor facility

- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
 - Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 32-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI
 - Four inbound windows
 - Four outbound windows plus default translation for PCI
- DDR memory controller
 - Programmable timing supporting first generation DDR SDRAM
 - 64-bit data interface, up to MHz data rate
 - Four banks of memory supported, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Sleep mode support for self refresh DDR SDRAM
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access via JTAG port
 - 2.5-V SSTL2 compatible I/O
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach ten percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay does not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8555E may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8555E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		V_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
PLL supply voltage		AV_{DD}	1.2 V $\pm$ 60 mV 1.3 V $\pm$ 50 mV (for 1 GHz only)	V
DDR DRAM I/O voltage		GV_{DD}	2.5 V $\pm$ 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV	V
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V $\pm$ 165 mV	V
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI, local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction Temperature		T_j	0 to 105	°C

7.2 DUART AC Electrical Specifications

Table 17 provides the AC timing parameters for the DUART interface of the MPC8555E.

Table 17. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{\text{CCB_CLK}} / 1048576$	baud	3
Maximum baud rate	$f_{\text{CCB_CLK}} / 16$	baud	1, 3
Oversample rate	16	—	2, 3

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
3. Guaranteed by design.

8 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), the MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 V or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 18](#) and [Table 19](#). The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver’s power supply (for example, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

8.2.4.2 TBI Receive AC Timing Specifications

Table 25 provides the TBI receive AC timing specifications.

Table 25. TBI Receive AC Timing Specifications

At recommended operating conditions with V_{DD} of 3.3 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}		16.0		ns
RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF} ^{2,3}	0.7	—	2.4	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

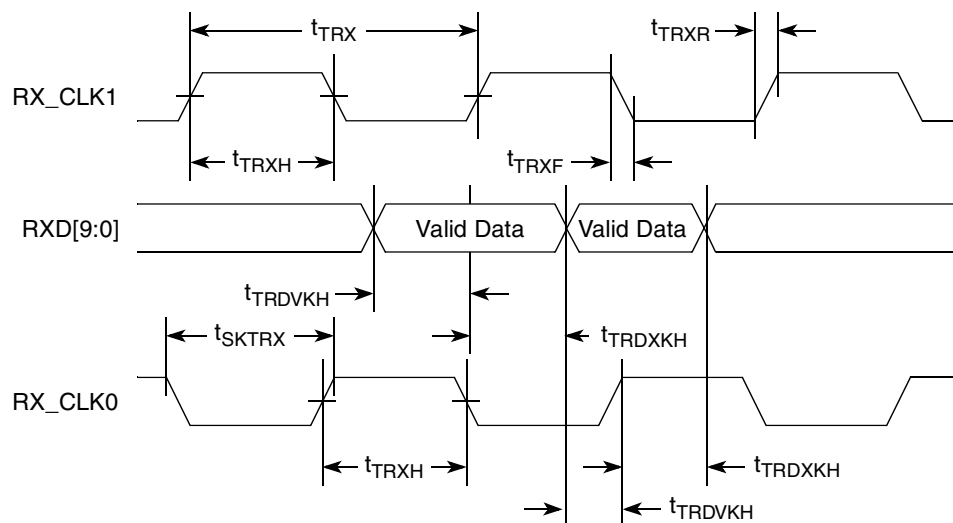


Figure 13. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 26 presents the RGMII and RTBI AC timing specifications.

Table 26. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}^{5}	–500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}^{6}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ⁴	t_{RGTH}/t_{RGT}^{6}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ³	t_{RGTH}/t_{RGT}^{6}	40	50	60	%
Rise and fall times	$t_{RGTR}^{6,7}, t_{RGTF}^{6,7}$	—	—	0.75	ns

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device functions with only 1.0 ns of delay.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Guaranteed by characterization.
- Guaranteed by design.
- Signal timings are measured at 0.5 and 2.0 V voltage levels.

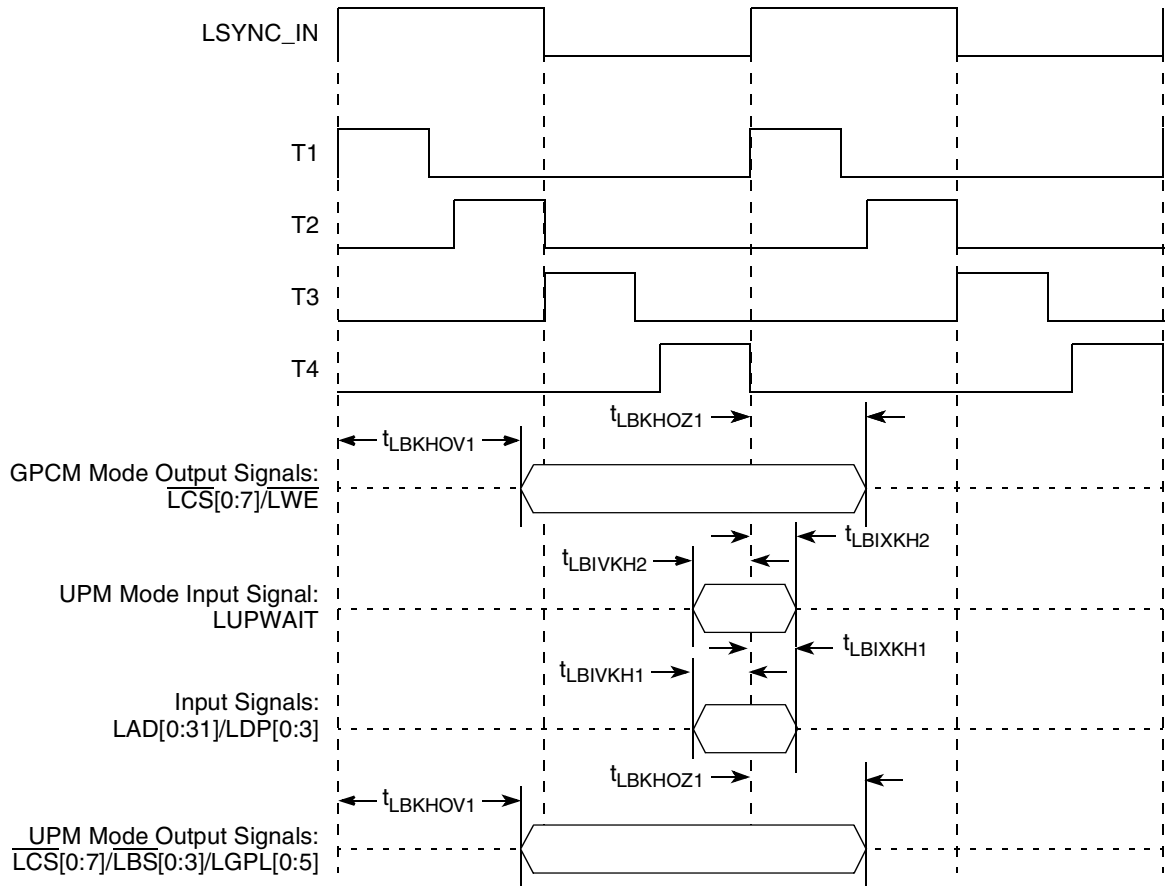


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

10 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8555E.

10.1 CPM DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the CPM.

Table 32. CPM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	3.465	V	1
Input low voltage	V_{IL}		GND	0.8	V	1, 2
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V	1
Output high voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1

Note:

1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. $V_{IL}(\text{max})$ for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

10.2 CPM AC Timing Specifications

Table 33 and Table 34 provide the CPM input and output AC timing specifications, respectively.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 33. CPM Input AC Timing Specifications ¹

Characteristic	Symbol ²	Min ³	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	6	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	t_{FEIXKH}^b	2	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	6	ns
SCC/SMC/SPI inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SMC/SPI inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SMC/SPI inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	4	ns

11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8555E.

Table 38 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 38. JTAG AC Timing Specifications (Independent of SYSCLK) ¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	— —	ns	4
Input hold times: Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	— —	ns	4
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	— —	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{CLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{CLK} .
5. Non-JTAG signal output timing with respect to t_{CLK} .
6. Guaranteed by design.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8555E. Note that the SYSCLK signal is used as the PCI input clock. Table 42 provides the PCI AC timing specifications at 66 MHz.

NOTE

PCI Clock can be PCI1_CLK or SYSCLK based on POR config input.

NOTE

The input setup time does not meet the PCI specification.

Table 42. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from Clock	t_{PCKHOX}	2.0	—	ns	2, 9
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to Clock	t_{PCIVKH}	3.3	—	ns	2, 4, 9
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{REQ64}$ to $\overline{HRESET}$ ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

- Note that the symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
- The setup and hold time is with respect to the rising edge of $\overline{HRESET}$.
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for $\overline{HRESET}$ is 100 μs .
- Guaranteed by characterization.
- Guaranteed by design.

Figure 16 provides the AC test load for PCI.

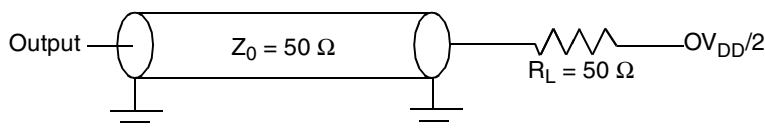


Figure 39. PCI AC Test Load

14.2 Mechanical Dimensions of the FC-PBGA

Figure 42 the mechanical dimensions and bottom surface nomenclature of the MPC8555E 783 FC-PBGA package.

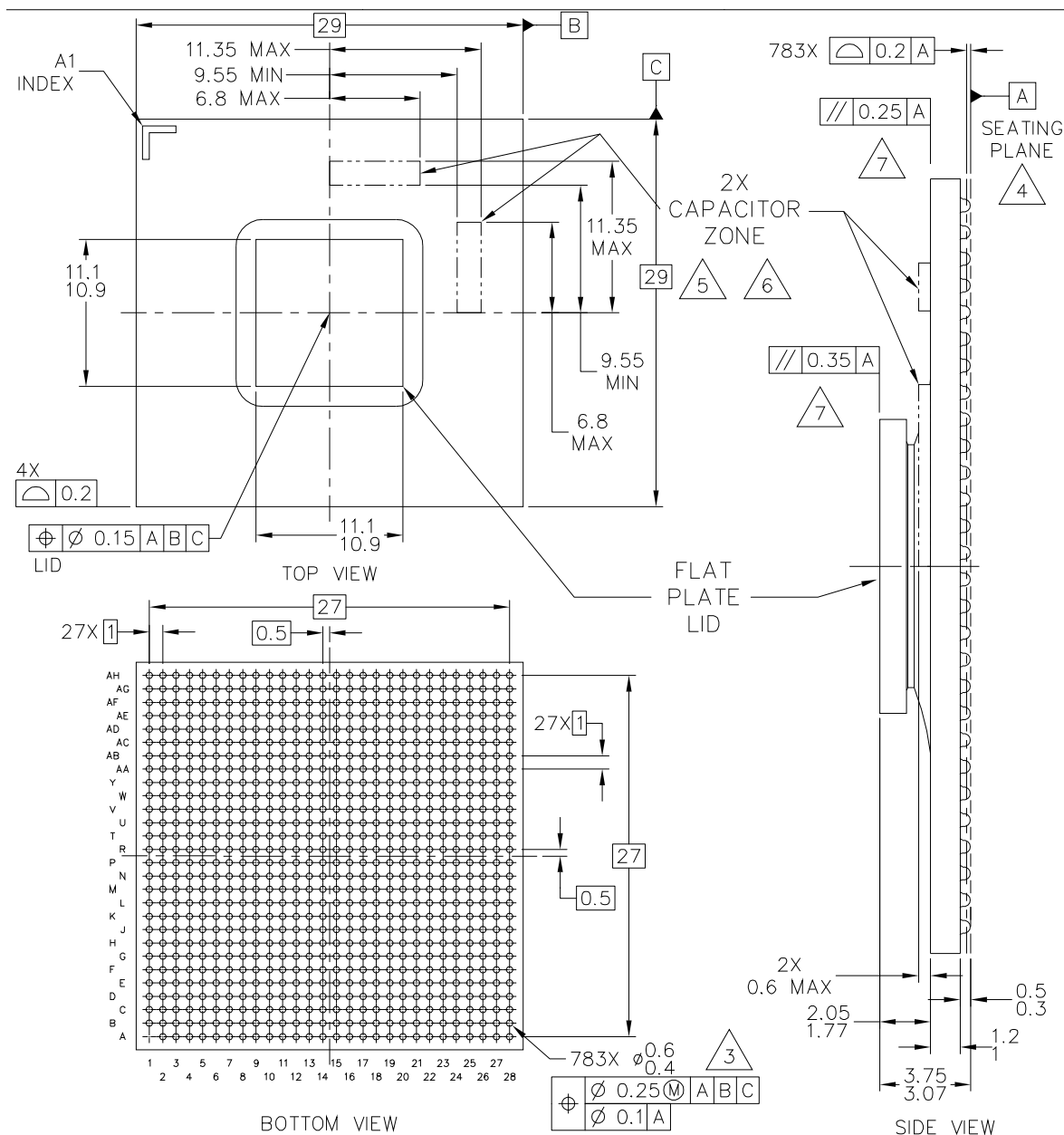


Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA

Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV _{DD}	—
IRQ8	AB20	I	OV _{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV _{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV _{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV _{DD}	1
IRQ_OUT	AB21	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV _{DD}	5, 9
EC_MDIO	E1	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV _{DD}	—
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV _{DD}	9, 18
TSEC1_TX_EN	C8	O	LV _{DD}	11
TSEC1_TX_ER	B8	O	LV _{DD}	—
TSEC1_TX_CLK	C6	I	LV _{DD}	—
TSEC1_GTX_CLK	B6	O	LV _{DD}	—
TSEC1_CRS	C3	I	LV _{DD}	—
TSEC1_COL	G7	I	LV _{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV _{DD}	—
TSEC1_RX_DV	D2	I	LV _{DD}	—
TSEC1_RX_ER	E5	I	LV _{DD}	—
TSEC1_RX_CLK	D6	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV _{DD}	—
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV _{DD}	5, 9, 18
TSEC2_TX_EN	B11	O	LV _{DD}	11
TSEC2_TX_ER	D11	O	LV _{DD}	—
TSEC2_TX_CLK	D10	I	LV _{DD}	—
TSEC2_GTX_CLK	C10	O	LV _{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_CRS	D9	I	LV _{DD}	—
TSEC2_COL	F8	I	LV _{DD}	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV _{DD}	—
TSEC2_RX_DV	H8	I	LV _{DD}	—
TSEC2_RX_ER	A8	I	LV _{DD}	—
TSEC2_RX_CLK	E10	I	LV _{DD}	—
DUART				
UART_CTS[0,1]	Y2, Y3	I	OV _{DD}	—
UART_RTS[0,1]	Y1, AD1	O	OV _{DD}	—
UART_SIN[0,1]	P11, AD5	I	OV _{DD}	—
UART_SOUT[0,1]	N6, AD2	O	OV _{DD}	—
I²C interface				
IIC_SDA	AH22	I/O	OV _{DD}	4, 19
IIC_SCL	AH23	I/O	OV _{DD}	4, 19
System Control				
HRESET	AH16	I	OV _{DD}	—
HRESET_REQ	AG20	O	OV _{DD}	18
SRESET	AF20	I	OV _{DD}	—
CKSTP_IN	M11	I	OV _{DD}	—
CKSTP_OUT	G1	O	OV _{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV _{DD}	—
TRIG_OUT/READY	G2	O	OV _{DD}	6, 9, 18
MSRCID[0:1]	J9, G3	O	OV _{DD}	5, 6, 9
MSRCID[2:3]	F3, F5	O	OV _{DD}	6
MSRCID4	F2	O	OV _{DD}	6
MDVAL	F4	O	OV _{DD}	6
Clock				
SYSCLK	AH21	I	OV _{DD}	—
RTC	AB23	I	OV _{DD}	—
CLK_OUT	AF22	O	OV _{DD}	—

Table 43. MPC8555E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11, C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7	—	—	—
GV _{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV _{DD}	—
LV _{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV _{DD}	—
MV _{REF}	N27	Reference Voltage Signal; DDR	MV _{REF}	—
No Connects	AA24, AA25, AA3, AA4, AA7, AA8, AB24, AB25, AC24, AC25, AD23, AD24, AD25, AE23, AE24, AE25, AE26, AE27, AF24, AF25, H1, H2, J1, J2, J3, J4, J5, J6, M1, N1, N10, N11, N4, N5, N7, N8, N9, P10, P8, P9, R10, R11, T24, T25, U24, U25, V24, V25, W24, W25, W9, Y24, Y25, Y5, Y6, Y9, AH26, AH28, AG28, AH1, AG1, AH2, B1, B2, A2, A3	—	—	16
OV _{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV _{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V _{DD}	13
SENSEVSS	K12	—	—	13
V _{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V _{DD}	—
CPM				
PA[8:31]	J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/O	OV _{DD}	—

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in [Table 46](#).

There is no default for this PLL ratio; these signals must be pulled to the desired values.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 46. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that allows the MPC8555E to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8555E thermal model is shown in Figure 44. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.6 mm with the conductivity adjusted accordingly. The die is modeled as 8.7 x 9.3 mm at a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 4.4 W/m•K in the thickness dimension of 0.07 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 8.7 x 9.3 x 0.05 mm and the conductivity of 1.07 W/m•K. The nickel plated copper lid is modeled as 11 x 11 x 1 mm.

Conductivity	Value	Unit
Lid (11 × 11 × 1 mm)		W/(m × K)
k _x	360	
k _y	360	
k _z	360	
Lid Adhesive—Collapsed resistance (8.7 × 9.3 × 0.05 mm)		
k _z	1.07	
Die (8.7 × 9.3 × 0.75 mm)		
Bump/Underfill—Collapsed resistance (8.7 × 9.3 × 0.07 mm)		
k _z	4.4	
Substrate and Solder Balls (25 × 25 × 1.6 mm)		
k _x	14.2	
k _y	14.2	
k _z	1.2	

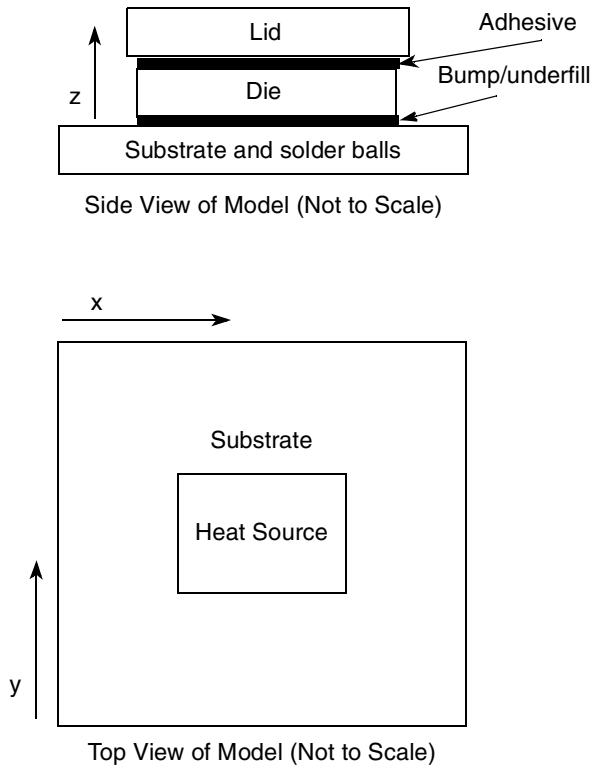


Figure 44. MPC8555E Thermal Model

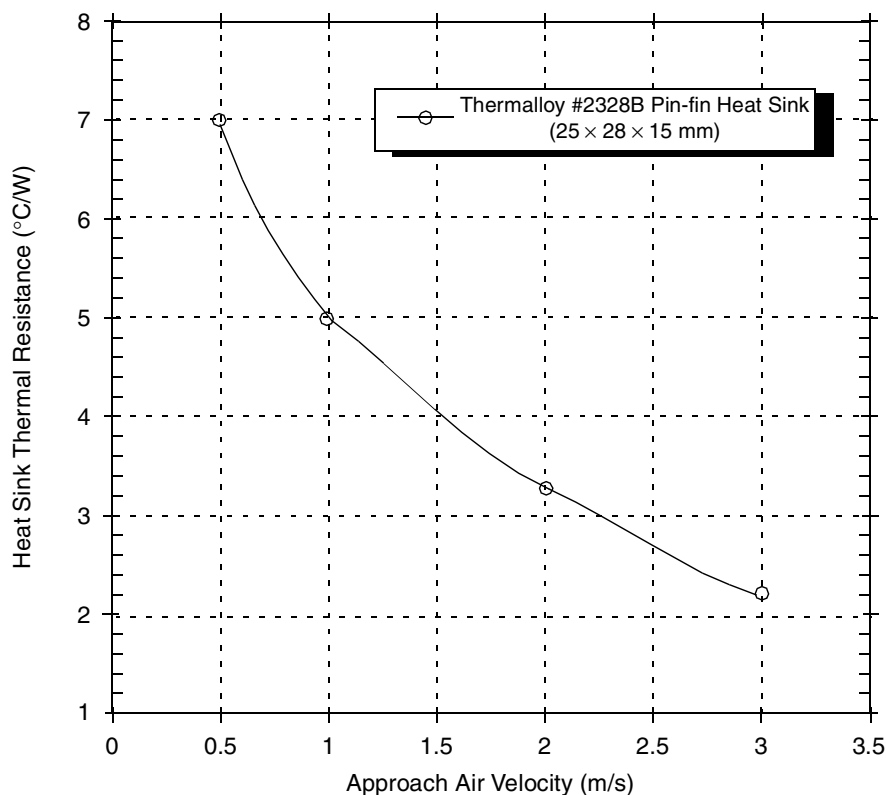


Figure 47. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 8 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.5 °C/W. The value of the junction to case thermal resistance in [Table 49](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 1.5 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 48](#) and [Figure 49](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 48 and provide exploded views of the plastic fence, heat sink, and spring clip.

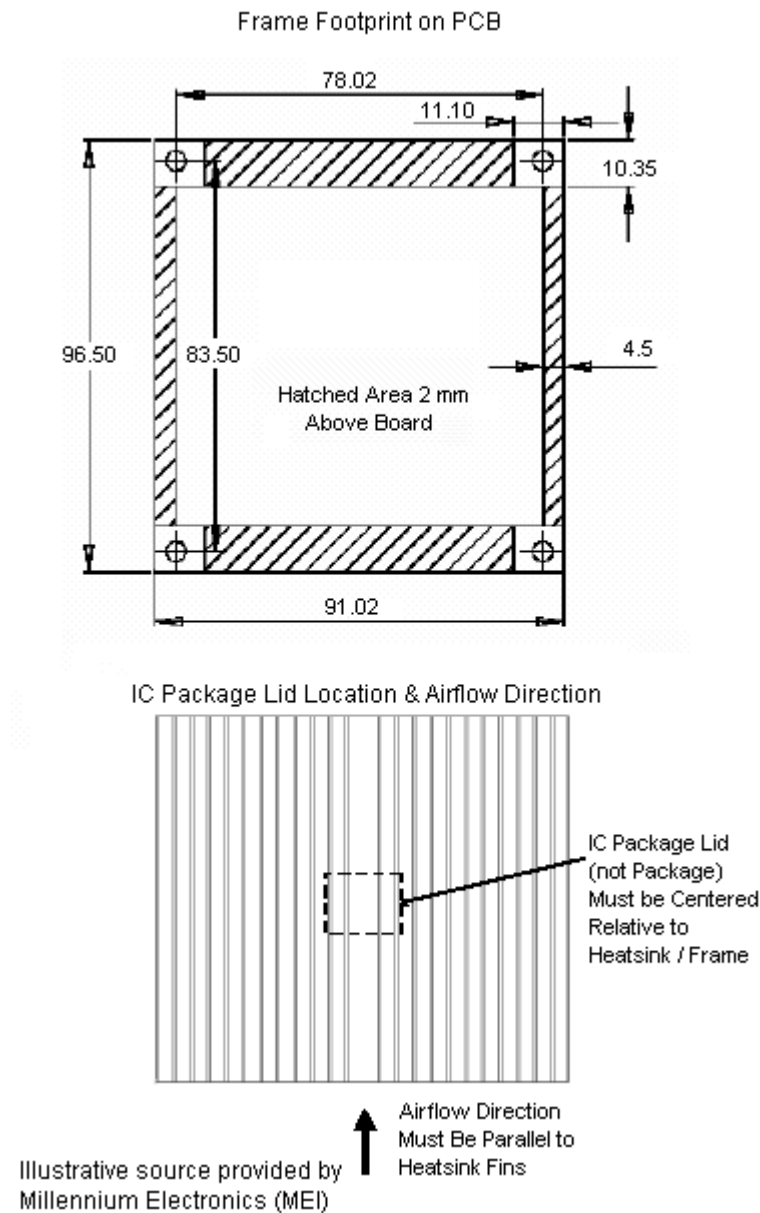
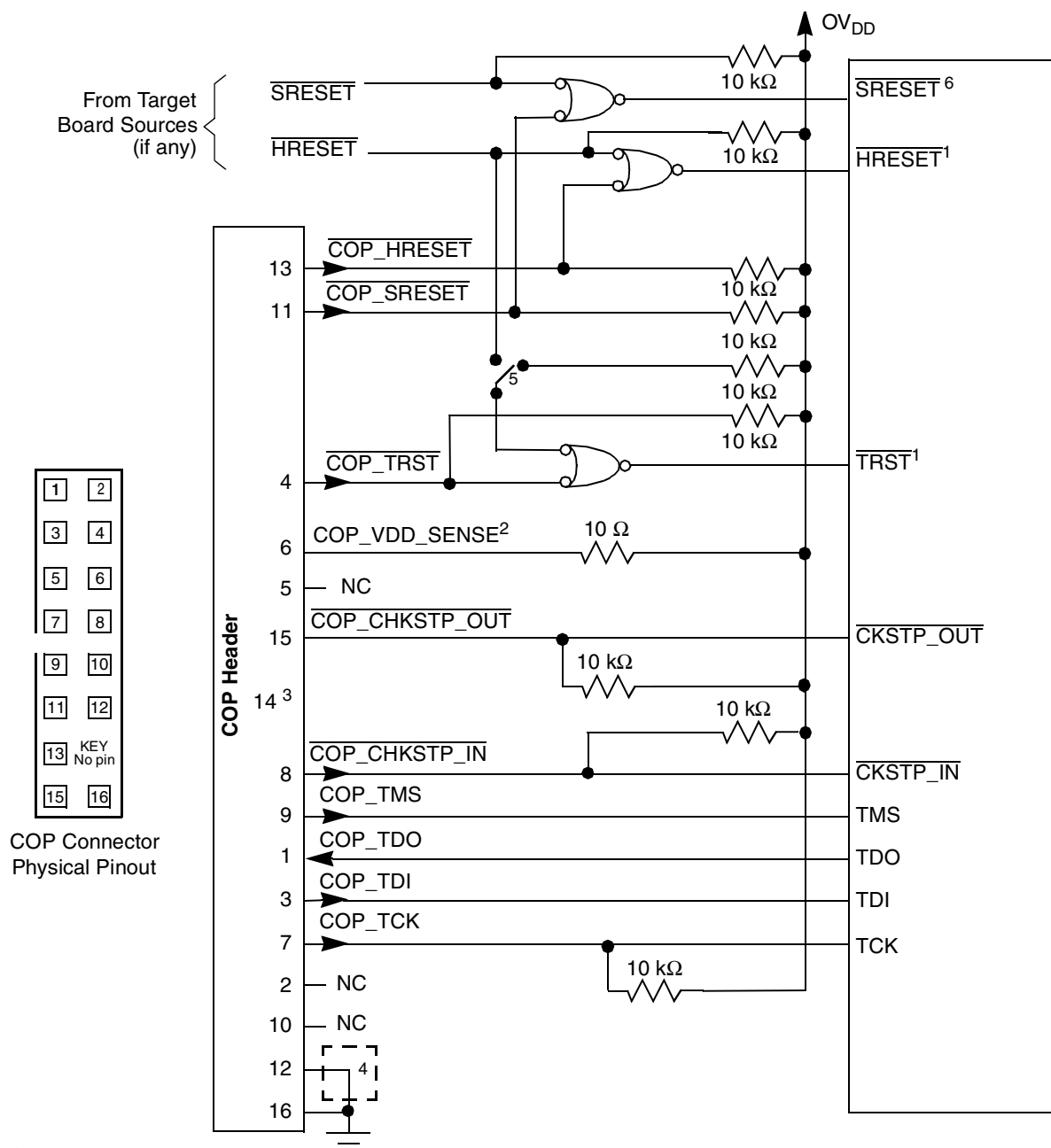


Figure 48. Exploded Views (1) of a Heat Sink Attachment using a Plastic Fence



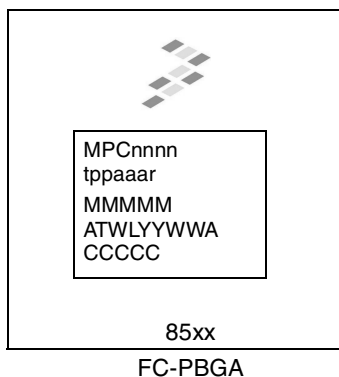
Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 53. JTAG Interface Connection

19.2 Part Marking

Parts are marked as the example shown in [Figure 54](#).



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 54. Part Marking for FC-PBGA Device