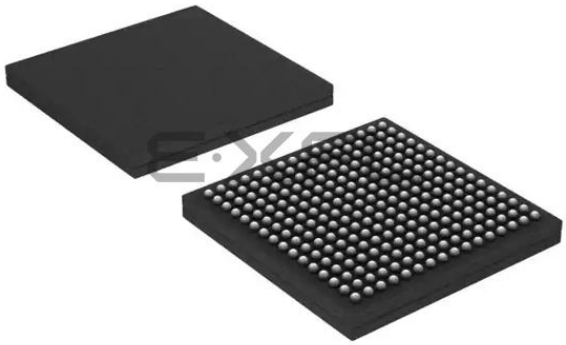


Welcome to E-XFL.COM

Embedded - FPGAs (Field Programmable Gate Array) with Microcontrollers: Enhancing Flexibility and Performance

Embedded - FPGAs (Field Programmable Gate Arrays) with Microcontrollers represent a cutting-edge category of electronic components that combine the flexibility of FPGA technology with the processing power of integrated microcontrollers. This hybrid approach offers a versatile solution for designing and implementing complex digital systems that require both programmable logic and embedded processing capabilities.

What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	4K-16K
FPGA SRAM	2kb
EEPROM Size	256K x 8
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	256
FPGA Gates	5K
FPGA Registers	436
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C
Package / Case	256-LBGA, CABGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94s05al-25dgi

- **V_{CC}: 3.0V - 3.6V**
- **5V Tolerant I/O**
- **3.3V 33 MHz PCI Compliant FPGA I/O**
  - **20 mA Sink/Source High-performance I/O Structures**
  - **All FPGA I/O Individually Programmable**
- **High-performance, Low-power 0.35µ CMOS Five-layer Metal Process**
- **State-of-the-art Integrated PC-based Software Suite including Co-verification**

1. Description

The AT94S Series (Secure FPSLIC family) shown in Table 1-1 is a combination of the popular Atmel AT40K Series SRAM FPGAs, the AT17 Series Configuration Memories and the high-performance Atmel AVR 8-bit RISC microcontroller with standard peripherals. Extensive data and instruction SRAM as well as device control and management logic are included in this multi-chip module (MCM).

The embedded AT40K FPGA core is a fully 3.3V PCI-compliant, SRAM-based FPGA with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data) and 5,000 to 40,000 usable gates.

Table 1-1. The AT94S Series Family

Device		AT94S05AL	AT94S10AL	AT94S40AL
Configuration Memory Size		1 Mbit	1 Mbit	1 Mbit
FPGA Gates		5K	10K	40K
FPGA Core Cells		256	576	2304
FPGA SRAM Bits		2048	4096	18432
FPGA Registers (Total)		436	846	2862
Maximum FPGA User I/O		93	137	162
AVR Programmable I/O Lines		8	16	16
Program SRAM Bytes		4K - 16K	20K - 32K	20K - 32K
Data SRAM Bytes		4K - 16K	4K - 16K	4K - 16K
Hardware Multiplier (8-bit)		Yes	Yes	Yes
2-wire Serial Interface		Yes	Yes	Yes
UARTs		2	2	2
Watchdog Timer		Yes	Yes	Yes
Timer/Counters		3	3	3
Real-time Clock		Yes	Yes	Yes
JTAG ICE		Yes	Yes	Yes
Typical AVR Throughput	@ 25 MHz	19 MIPS	19 MIPS	19 MIPS
	@ 40 MHz	30 MIPS	30 MIPS	30 MIPS
Operating Voltage		3.0 - 3.6V	3.0 - 3.6V	3.0 - 3.6V

2. Internal Architecture

For details of the AT94S Secure FPSLIC architecture, please refer to the AT94K FPSLIC datasheet and the AT17 Series Configuration Memory datasheet, available on the Atmel web site at http://www.atmel.com. This document only describes the differences between the AT94S Secure FPSLIC and the AT94K FPSLIC.

3. FPSLIC and Configurator Interface

- Fully In-System Programmable and Re-programmable
- When Security Bit Set:
  - Data Verification Disabled
  - Data Transfer to FPSLIC not Externally Visible
  - Secured EEPROM Will Only Boot the FPSLIC Device or Respond to a Chip Erase
- When Security Bit Cleared:
  - Entire Chip Erase Performed
  - In-System Programming Enabled
  - Data Verification Enabled

External Data pins allow for In-System Programming of the device and setting of the EEPROM-based security bit. When the security bit is set (active) this programming connection will only respond to a device erase command. Data cannot be read out of the external programming/data pins when the security bit is set. The part can be re-programmed, but only after first being erased.

4. Programming and Configuration Timing Characteristics

Atmel's Configurator Programming Software (CPS), available from the Atmel web site (http://www.atmel.com/dyn/products/tools_card.asp?tool_id=3191), creates the programming algorithm for the embedded configurator; however, if you are planning to write your own software or use other means to program the embedded configurator, the section below includes the algorithm and other details.

4.1 The FPSLIC Configurator

The FPSLIC Configurator is a serial EEPROM memory which is used to load programmable devices. This document describes the features needed to program the Configurator from within its programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low).

Reference schematics are supplied for ISP applications.

4.2 Serial Bus Overview

The serial bus is a two-wire bus; one wire (cSCK) functions as a clock and is provided by the programmer, the second wire (cSDA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a Start Condition and ends with a Stop Condition. The message consists of an integer number of bytes, each byte consisting of 8 bits of data, followed by a ninth Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted byte. This is possible because devices

may only drive the cSDA line Low. The system must provide a small pull-up current (1 kΩ equivalent) for the cSDA line.

The MESSAGE FORMAT for read and write instructions consists of the bytes shown in "Bit Format" on page 5.

While writing, the programmer is responsible for issuing the instruction and data. While reading, the programmer issues the instruction and acknowledges the data from the Configurator as necessary.

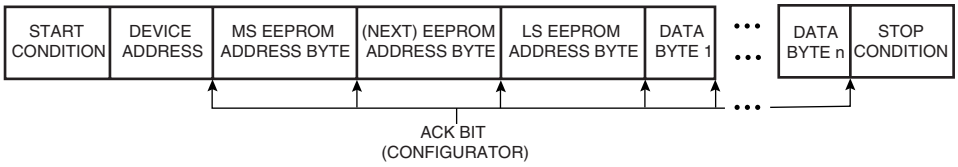
Again, the Acknowledge Bit is asserted on the cSDA line by the receiving device on a byte-by-byte basis.

The factory blanks devices to all zeros before shipping. The array cannot otherwise be "initialized" except by explicitly writing a known value to each location using the serial protocol described herein.

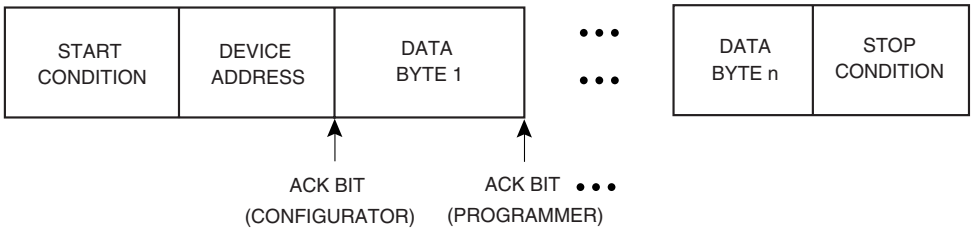
4.3 Bit Format

Data on the cSDA pin may change only during the cSCK Low time; whereas Start and Stop Conditions are identified as transitions during the cSCK High time.

Write Instruction Message Format



Current Address Read (Extended to Sequential Read) Instruction Message Format



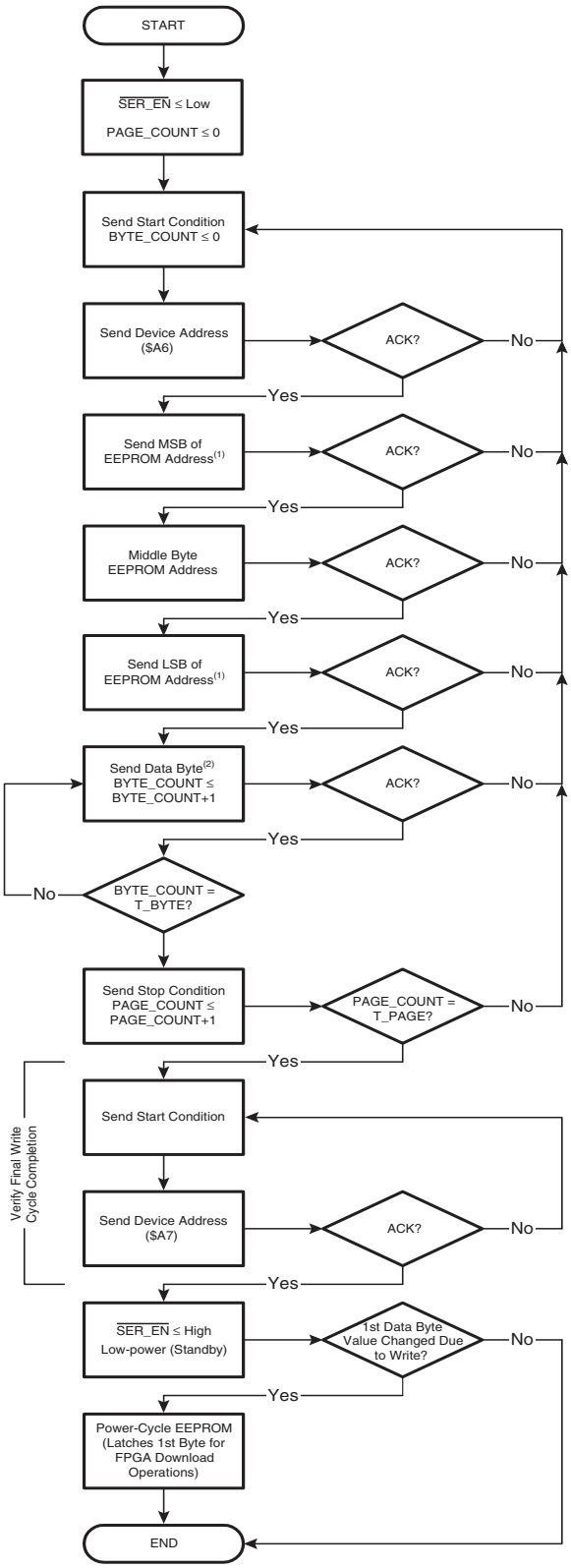
4.4 Start and Stop Conditions

The Start Condition is indicated by a high-to-low transition of the cSDA line when the cSCK line is High. Similarly, the Stop Condition is generated by a low-to-high transition of the cSDA line when the cSCK line is High, as shown in Figure 4-1.

The Start Condition will return the device to the state where it is waiting for a Device Address (its normal quiescent mode).

The Stop Condition initiates an internally timed write signal whose maximum duration is t_{WR} (refer to AC Characteristics table for actual value). During this time, the Configurator must remain in programming mode (i.e., $\overline{\text{SER\_EN}}$ is driven Low). cSDA and cSCK lines are ignored until the cycle is completed. Since the write cycle typically completes in less than t_{WR} seconds, we recommend the use of "polling" as described in later sections. Input levels to all other pins should be held constant until the write cycle has been completed.

4.8 Programming Summary: Write to Whole Device



Notes: 1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.

2. Data byte received/sent LSB to MSB.

4.8.1 EEPROM Address is Defined as:

AT17LV010 0000 $000x_9$ $x_8x_7x_6x_5$ $x_4x_3x_2x_1$ x_0000 0000

Note: where X_n ... X_0 is (PAGE_COUNT)\b

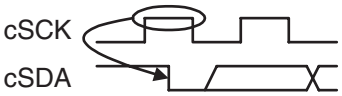
4.8.2 T_BYTE

AT17LV010 128

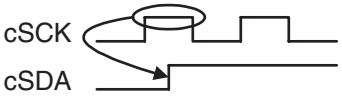
4.8.3 T_PAGE

AT17LV010 1024

START CONDITION

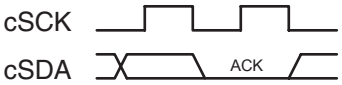


STOP CONDITION

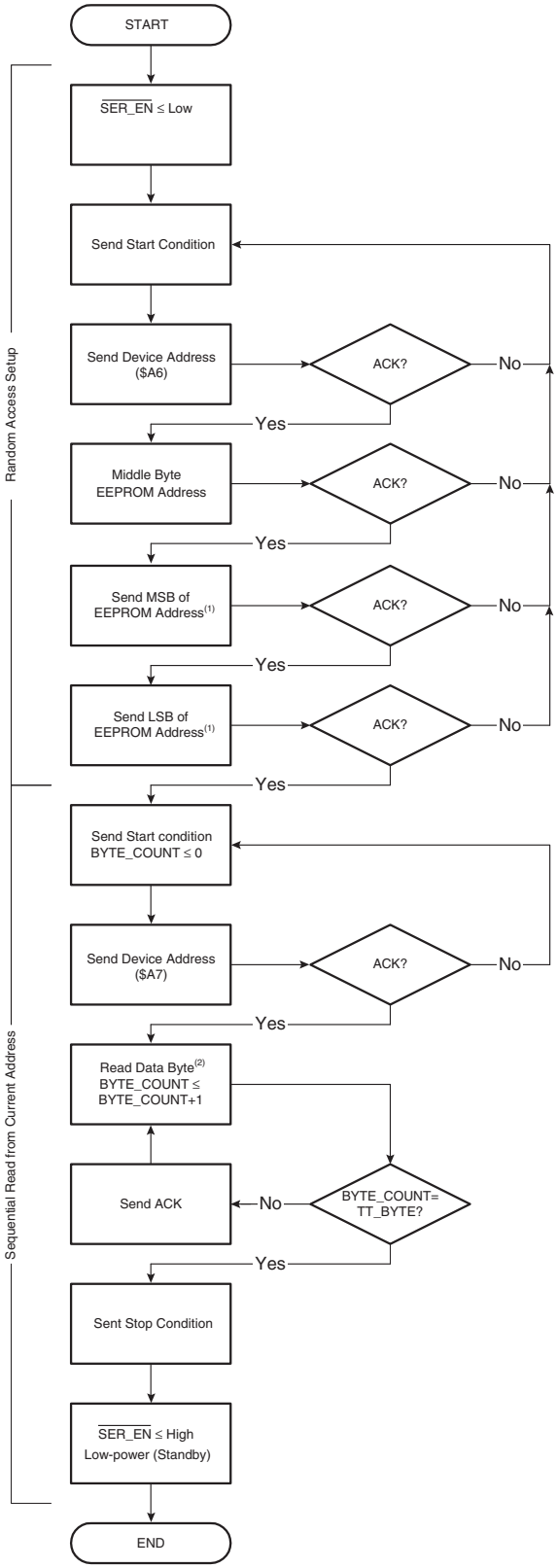


DATA BIT

ACK BIT



4.9 Programming Summary: Read from Whole Device



Notes: 1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.

2. Data byte received/sent LSB to MSB

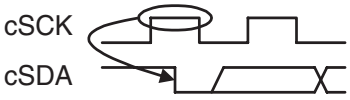
4.9.1 EEPROM Address is Defined as:

AT17LV010	00 00 00 \h

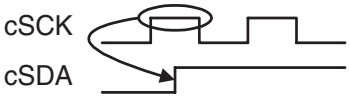
4.9.2 TT_BYTE

AT17LV010	131072 \d

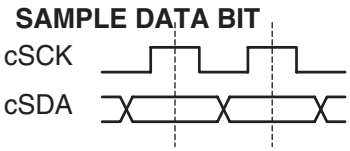
START CONDITION



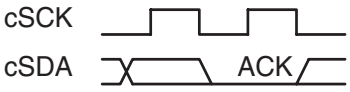
STOP CONDITION



SAMPLE DATA BIT



ACK BIT



4.9.5.3 *Sequential Read*

Sequential Reads follow either a Current Address Read or a Random Address Read. After the programmer receives a Data Byte, it may respond with an Acknowledge Bit. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached.(1) The Sequential Read instruction is terminated when the programmer does not respond with an Acknowledge Bit but instead generates a Stop Condition following the receipt of a Data Byte.

Note: 1. If an ACK is sent by the programmer after the data in the last memory address is sent by the configurator, the internal address counter will "rollover" to the first byte address of the memory array and continue to send data as long as an ACK is sent by the programmer.

4.9.6 Programmer Functions

The following programmer functions are supported while the Configurator is in programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low):

1. Read the Manufacturer's Code and the Device Code (optional for ISP).
2. Program the device.
3. Verify the device.

In the order given above, they are performed in the following manner.

4.9.7 Reading Manufacturer's and Device Codes

On AT17LV010 Configurator, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 040000H.

The correct codes are:

```
Manufacturers Code -Byte 0    1E
Device Code      - Byte 1 F7   AT17LV010
```

Note: The Manufacturer's Code and Device Code are read using the byte ordering specified for Data Bytes; i.e., LSB first, MSB last.

4.9.8 Programming the Device

All the bytes in a given page must be written. The page access order is not important but it is suggested that the Configurator be written sequentially from address 0. Writing is accomplished by using the cSDA and cSCK pins.

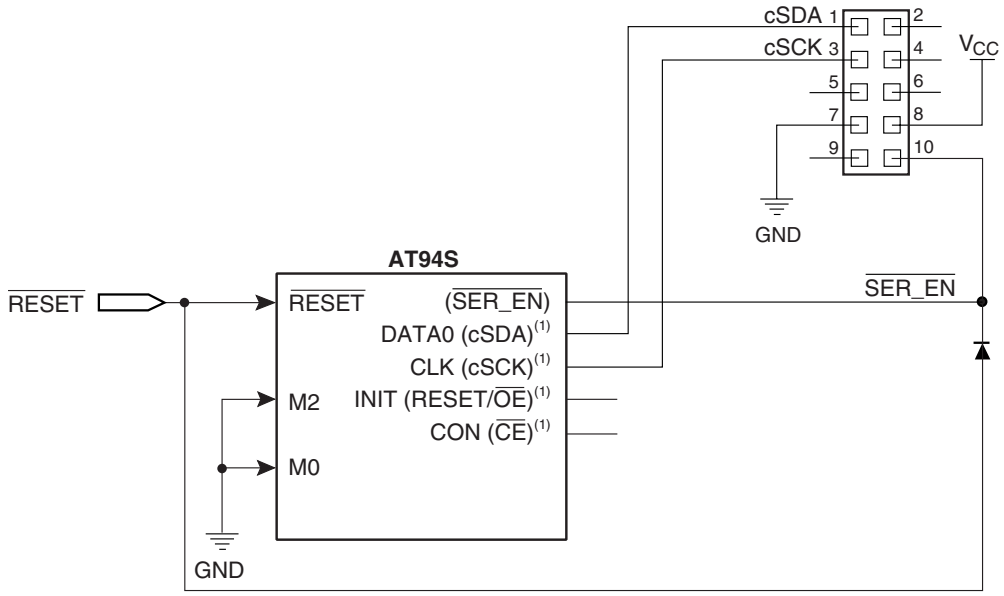
4.9.8.1 *Important Note on AT94S Series Configurators Programming*

The first byte of data will not be cached for read back during FPGA Configuration (i.e., when $\overline{\text{SER\_EN}}$ is driven High) until the Configurator is power-cycled.

4.9.9 Verifying the Device

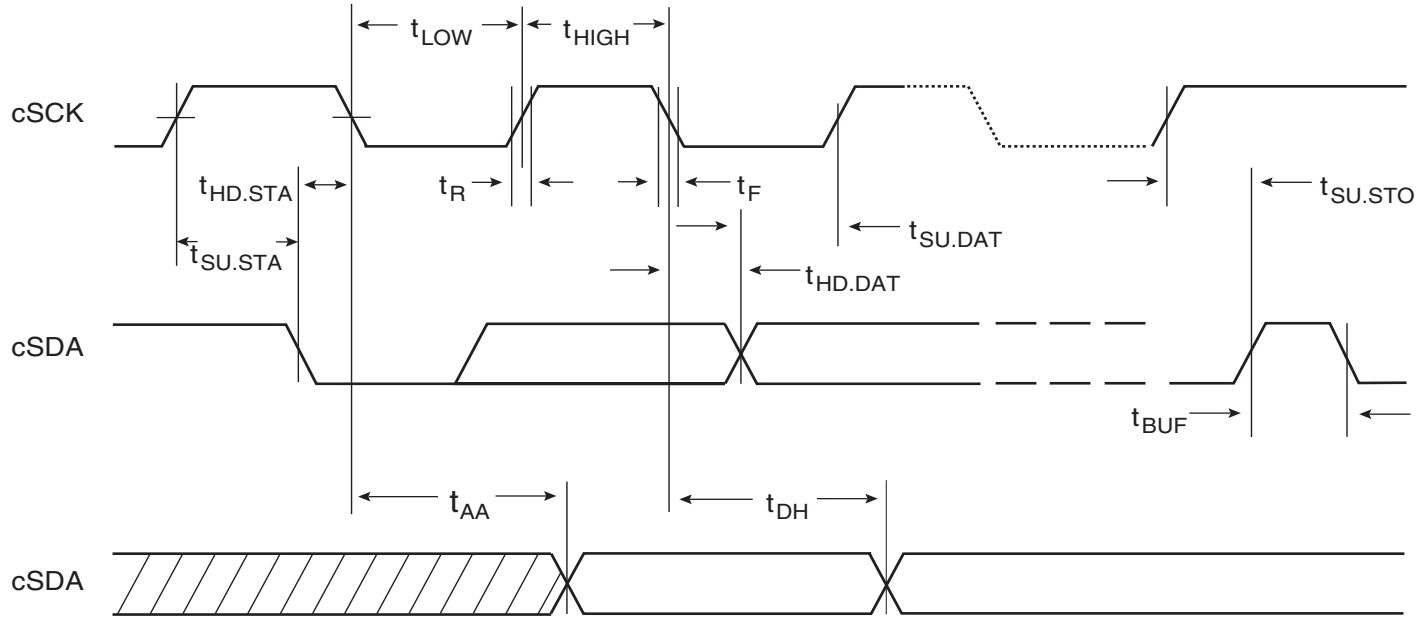
All bytes in the Configurator should be read and compared to their intended values. Reading is done using the cSDA and cSCK pins.

Figure 4-3. ISP of the AT17LV512/010 in an AT94S FPSLIC Application



Note: 1. Configurator signal names are shown in parenthesis.

Figure 4-4. Serial Data Timing Diagram



4.11 DC Characteristics[1]

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C[2][3][4]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Supply Current	V_{CC} = 3.6		2	3	mA
I_{LL}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.2	V
V_{OL}	Output Low-level Voltage	I_{OL} = 2.1 mA			0.4	V

Notes: 1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

4.12 AC Characteristics[1]

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C[2][3][4]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		100	KHz
t_{LOW}	Clock Pulse Width Low	4		µs
t_{HIGH}	Clock Pulse Width High	4		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.5		µs
$t_{HD;STA}$	Start Hold Time	2		µs
$t_{SU;STA}$	Start Setup Time	2		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Setup Time	0.2		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	2		µs
t_{DH}	Data Out Hold Time	0.1		µs
t_{WR}	Write Cycle Time		20	ms

Notes: 1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

4.13 Secure FPSLIC Configurator Pin Configurations

144-pin LQFP	256-pin CABGA	Name	I/O	Description
105	D16	cSDA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
107	C16	cSCK	O	CLOCK output. Used to increment the internal address and bit counter for reading and programming.
53	K9	RESET/$\overline{OE}$	I	RESET/$\overline{OE}$ input (when $\overline{SER\_EN}$ is High). A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This document describes the pin as RESET/$\overline{OE}$.
72	N16	$\overline{CE}$	I	Chip Enable input. Used for device selection only when $\overline{SER\_EN}$ is High. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power mode. Note this pin will not enable/disable the device in the 2-wire Serial mode (i.e., when $\overline{SER\_EN}$ is driven Low).
81	M5	$\overline{SER\_EN}$	I	Serial enable is normally High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the programming mode.

4.14 Security Bit

Once the security bit is programmed, data will no longer output from the normal data pad. Once the fuse is set, any attempt to erase the fuse will cause the configurator to erase all of it contents.

4.14.1 AT17LV512/010 Security Bit Programming

4.14.1.1 Disabling the Security Bit

Write 4 bytes “00 00 00 00” to addresses 800000-800003 two consecutive times, using the previously defined 2-wire write algorithm. Thereafter, either cycle the power or toggle (HI-LO-HI) the $\overline{SER\_EN}$ pin in order to disable the security.

4.14.1.2 Enabling the Security Bit

Write 4 bytes “FF FF FF FF” to addresses 800000-800003 using the previously defined 2-wire write algorithm.

4.14.1.3 Verifying the Security Bit

Read 4 bytes of data from addresses 800000-800003 using the previously defined 2-wire Random Read algorithm. If the data is “FF FF FF FF”, the security bit has been enabled. If the data is “00 00 00 00”, the security bit has been disabled.

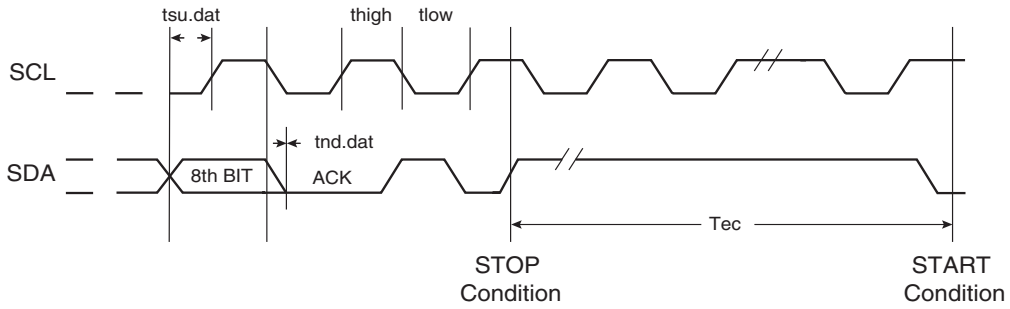
4.15 Chip Erase Timing

The entire device can be erased at once by writing to a specific address. This operation will erase the entire array. See Table 4-2 for specifics on the write algorithm.

Table 4-2. Chip Erase Cycle Characteristics

Symbol	Parameter
Tec	Chip Erase Cycle Time (25 ms)

Figure 4-5. Chip Erase Timing Diagram



5. Packaging and Pin List information

Table 5-1. Part and Package Combinations Available

Part #	Package	AT94S05	AT94S10	AT94S40
BG256	DG	93	137	162
LQ144	BQ	–	84	84

Table 5-2. AT94K JTAG ICE Pin List

Pin	AT94S05 96 FPGA I/O	AT94S10 192 FPGA I/O	AT94S40 384 FPGA I/O
TDI	IO34	IO50	IO98
TDO	IO38	IO54	IO102
TMS	IO43	IO63	IO123
TCK	IO44	IO64	IO124

Table 5-3. AT94S Pin List

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
FPSLIC Array				
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	A1	2
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	D4	3
I/O3	I/O3	I/O3	D3	4
I/O4	I/O4	I/O4	B1	5
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	C2	6
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	C1	7
		I/O7		
		I/O8		
NC	NC	I/O9	D2	
NC	NC	I/O10	D1	
		I/O11		
		I/O12		
		I/O13		
		I/O14		
I/O7	I/O7	I/O15	E3	
I/O8	I/O8	I/O16	E4	
NC	I/O9	I/O17	E2	
NC	I/O10	I/O18	E1	
		I/O19		
		I/O20		
NC	I/O11	I/O21	F4	
NC	I/O12	I/O22	F3	
		I/O23		
		I/O24		
I/O9, FCK1	I/O13, FCK1	I/O25, FCK1	F1	9
I/O10	I/O14	I/O26	G7	10
I/O11 (A20)	I/O15 (A20)	I/O27 (A20)	G6	11
I/O12 (A21)	I/O16 (A21)	I/O28 (A21)	G4	12
NC	I/O17	I/O29	G5	
NC	I/O18	I/O30	G2	
		I/O31		
		I/O32		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
		I/O33		
		I/O34		
NC	NC	I/O35	G1	
NC	NC	I/O36	H7	
		I/O37		
		I/O38		
NC	NC	I/O39	H6	
NC	NC	I/O40	H5	
NC	I/O19	I/O41	H3	
NC	I/O20	I/O42	H4	
I/O13	I/O21	I/O43	H2	13
I/O14	I/O22	I/O44	H1	14
		I/O45		
		I/O46		
I/O15 (A22)	I/O23 (A22)	I/O47 (A22)	J7	15
I/O16 (A23)	I/O24 (A23)	I/O48 (A23)	J1	16
I/O17 (A24)	I/O25 (A24)	I/O49 (A24)	J4	19
I/O18 (A25)	I/O26 (A25)	I/O50 (A25)	J5	20
		I/O51		
		I/O52		
I/O19	I/O27	I/O53	J6	21
I/O20	I/O28	I/O54	J8	22
NC	I/O29	I/O55	K1	
NC	I/O30	I/O56	K2	
		I/O57		
		I/O58		
		I/O59		
		I/O60		
NC	NC	I/O61	K4	
NC	NC	I/O62	K5	
		I/O63		
		I/O64		
NC	NC	I/O65	K6	
NC	NC	I/O66	L1	

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
NC	I/O31	I/O67	L2	
NC	I/O32	I/O68	L5	
I/O21 (A26)	I/O33 (A26)	I/O69 (A26)	L4	23
I/O22 (A27)	I/O34 (A27)	I/O70 (A27)	M1	24
I/O23	I/O35	I/O71	M2	25
I/O24, FCK2	I/O36, FCK2	I/O72, FCK2	N1	26
		I/O73		
		I/O74		
	I/O37	I/O75		
	I/O38	I/O76		
		I/O77		
		I/O78		
		I/O79		
		I/O80		
I/O25	I/O39	I/O81	M3	
I/O26	I/O40	I/O82	N2	
	I/O41	I/O83		
	I/O42	I/O84		
		I/O85		
		I/O86		
		I/O87		
		I/O88		
I/O27 (A28)	I/O43 (A28)	I/O89 (A28)	P1	28
I/O28	I/O44	I/O90	P2	29
		I/O91		
		I/O92		
I/O29	I/O45	I/O93	R1	30
I/O30	I/O46	I/O94	N3	31
I/O31 ($\overline{\text{OTS}}$)	I/O47 ($\overline{\text{OTS}}$)	I/O95 ($\overline{\text{OTS}}$)	T1	32
I/O32, GCK2 (A29)	I/O48, GCK2 (A29)	I/O96, GCK2 (A29)	P3	33
AVRRESET	$\overline{\text{AVRRESET}}$	$\overline{\text{AVRRESET}}$	R2	34
M0	M0	M0	R3	36
FPSLIC Array				
M2	M2	M2	T3	38

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
I/O33, GCK3	I/O49, GCK3	I/O97, GCK3	R4	39
I/O34 (HDC/TDI)	I/O50 (HDC/TDI)	I/O98 (HDC/TDI)	T4	40
I/O35	I/O51	I/O99	N5	41
I/O36	I/O52	I/O100	P5	42
	I/O53	I/O101		43
SER_EN	SER_EN	SER_EN	M5	81
I/O38 (LDC/TDO)	I/O54 (LDC/TDO)	I/O102 (LDC/TDO)	R5	44
		I/O103		
		I/O104		
		I/O105		
		I/O106		
NC	NC	I/O107	T5	
NC	NC	I/O108	M6	
I/O39	I/O55	I/O109	P6	
I/O40	I/O56	I/O110	R6	
NC	I/O57	I/O111	L6	
NC	I/O58	I/O112	T6	
		I/O113		
		I/O114		
		I/O115		
		I/O116		
	I/O59	I/O117		
	I/O60	I/O118		
		I/O119		
		I/O120		
I/O41	I/O61	I/O121	M7	46
I/O42	I/O62	I/O122	N7	47
I/O43 (TMS)	I/O63 (TMS)	I/O123 (TMS)	P7	48
I/O44 (TCK)	I/O64 (TCK)	I/O124 (TCK)	R7	49
NC	I/O65	I/O125	K7	
NC	I/O66	I/O126	K8	
		I/O127		
		I/O128		
		I/O129		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
FPSLIC Array				
Testclock	Testclock	Testclock	C15	109
I/O97 (A0)	I/O145 (A0)	I/O289 (A0)	C14	111
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O290, GCK7 (A1)	B15	112
I/O99	I/O147	I/O291	A16	113
I/O100	I/O148	I/O292	D13	114
		I/O293		
		I/O294		
NC	NC	I/O295	C13	
NC	NC	I/O296	B14	
I/O101 ($\overline{CS1}$, A2)	I/O149 ($\overline{CS1}$, A2)	I/O297 ($\overline{CS1}$, A2)	A15	115
I/O102 (A3)	I/O150 (A3)	I/O298 (A3)	A14	116
		I/O299		
		I/O300		
I/O104	I/O151	I/O301	Shared with Test clock	
NC	I/O152	I/O302	D12	
I/O103	I/O153	I/O303	C12	117
NC	I/O154	I/O304	A13	
NC	NC	I/O305	B12	
		I/O306		
		I/O307		
		I/O308		
NC	I/O155	I/O309	A12	
NC	I/O156	I/O310	E11	
NC	NC	I/O311	C11	
NC	NC	I/O312	D11	
I/O105	I/O157	I/O313	A11	119
I/O106	I/O158	I/O314	F10	120
NC	I/O159	I/O315	E10	
NC	I/O160	I/O316	D10	
NC	NC	I/O317	C10	
NC	NC	I/O318	B10	
		I/O319		
		I/O320		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
		I/O321		
		I/O322		
		I/O323		
		I/O324		
I/O107 (A4)	I/O161 (A4)	I/O325 (A4)	A10	121
I/O108 (A5)	I/O162 (A5)	I/O326 (A5)	G10	122
NC	I/O163	I/O327	G9	
NC	I/O164	I/O328	F9	
I/O109	I/O165	I/O329	E9	123
I/O110	I/O166	I/O330	C9	124
		I/O331		
		I/O332		
		I/O333		
		I/O334		
I/O111 (A6)	I/O167 (A6)	I/O335 (A6)	B9	125
I/O112 (A7)	I/O168 (A7)	I/O336 (A7)	A9	126
I/O113 (A8)	I/O169 (A8)	I/O337 (A8)	A8	129
I/O114 (A9)	I/O170 (A9)	I/O338 (A9)	B8	130
		I/O339		
		I/O340		
		I/O341		
		I/O342		
I/O115	I/O171	I/O343	C8	131
I/O116	I/O172	I/O344	D8	132
NC	I/O173	I/O345	E8	
NC	I/O174	I/O346	F8	
I/O117 (A10)	I/O175 (A10)	I/O347 (A10)	H8	133
I/O118 (A11)	I/O176 (A11)	I/O348 (A11)	A7	134
NC	NC	I/O349	C7	
NC	NC	I/O350	D7	
		I/O351		
		I/O352		
		I/O353		
		I/O354		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
		I/O355		
		I/O356		
NC	I/O177	I/O357	F7	
NC	I/O178	I/O358	A6	
I/O119	I/O179	I/O359	F6	135
I/O120	I/O180	I/O360	B6	136
		I/O361		
		I/O362		
NC	I/O181	I/O363	D6	
NC	I/O182	I/O364	E6	
		I/O365		
		I/O366		
		I/O367		
		I/O368		
I/O121	I/O183	I/O369	A5	
I/O122	I/O184	I/O370	B5	
I/O123 (A12)	I/O185 (A12)	I/O371 (A12)	E5	138
I/O124 (A13)	I/O186 (A13)	I/O372 (A13)	C5	139
		I/O373		
		I/O374		
		I/O375		
		I/O376		
		I/O377		
		I/O378		
NC	I/O187	I/O379	A4	
NC	I/O188	I/O380	B4	
I/O125	I/O189	I/O381	A3	140
I/O126	I/O190	I/O382	C4	141
I/O127 (A14)	I/O191 (A14)	I/O383 (A14)	B3	142
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O384, GCK8 (A15)	A2	143

Note: 1. LQ144 is only offered in the AT94S10 and AT94S40.

Table 5-4. 256 CABGA and LQ144 V_{DD}, V_{CC} and GND Pins[1]

Package	V_{DD} (core)	V_{CC} (I/O)	GND
256 CABGA	D14, E7, F12, G3, H9, K10, L13, M13, P4, T9	B2, G8, G13, H10, K13, L3, M10, R14, T3, T7	B11, B13, B16, B7, C3, C6, D5, D9, F11, F13, T15, F16, F2, F5, G16, H11, H16, J15, J2, K16, K3, T2, L14, L16, L7, M4, N15, N4, N6, P11, R9, R10, R15, T8
LQ144	18, 54, 90, 128	37, 73, 108, 144	1, 8, 17, 27, 35, 45, 55, 64, 71, 91, 100, 110, 118, 127, 137

Note: 1. For power rail support for product migration to lower-power devices, refer to the “Designing in Split Power Supply Support for AT94KAL/AX and AT94SAL/AX Devices” application note (doc2308.pdf), available on the Atmel web site, at http://www.atmel.com/dyn/products/app_notes.asp?family_id=627.

6. Thermal Coefficient Table

Package Style	Lead Count	Theta J-A [°C/W] 0 LFPM	Theta J-A [°C/W] 225 LFPM	Theta J-A [°C/W] 500 LPFM
CABGA	256	27	23	20
LQFP	144	35	—	—

7. Ordering Information

Usable Gates	Speed Grade	Ordering Code	Package	Operation Range
5,000	25 MHz	AT94S05AL-25DGC AT94S05AL-25BQC	256ZA 144L1	Commercial (0°C - 70°C)
		AT94S05AL-25DGI AT94S05AL-25BQI	256ZA 144L1	Industrial (-40°C - 85°C)
10,000	25 MHz	AT94S10AL-25DGC	256ZA	Commercial (0°C - 70°C)
		AT94S10AL-25BQC	144L1	
		AT94S10AL-25DGI	256ZA	Industrial (-40°C - 85°C)
		AT94S10AL-25BQI	144L1	
40,000	16 MHz	AT94S40AL-25DGC	256ZA	Commercial (0°C - 70°C)
		AT94S40AL-25DGI	256ZA	Industrial (-40°C - 85°C)

Package Type	
256ZA	256-ball, Chip Array Ball Grid Array Package (CABGA)
144L1	144-lead, Low Profile Plastic Gull Wing Quad Flat Package (LQFP)

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

2314E–FPSLI–6/05