Microchip Technology - AT94S10AL-25BQC Datasheet

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What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	20K-32K
FPGA SRAM	4kb
EEPROM Size	512K x 8
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	576
FPGA Gates	10K
FPGA Registers	846
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94s10al-25bqc

- **V_{CC}: 3.0V - 3.6V**
- **5V Tolerant I/O**
- **3.3V 33 MHz PCI Compliant FPGA I/O**
  - **20 mA Sink/Source High-performance I/O Structures**
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- **High-performance, Low-power 0.35µ CMOS Five-layer Metal Process**
- **State-of-the-art Integrated PC-based Software Suite including Co-verification**

1. Description

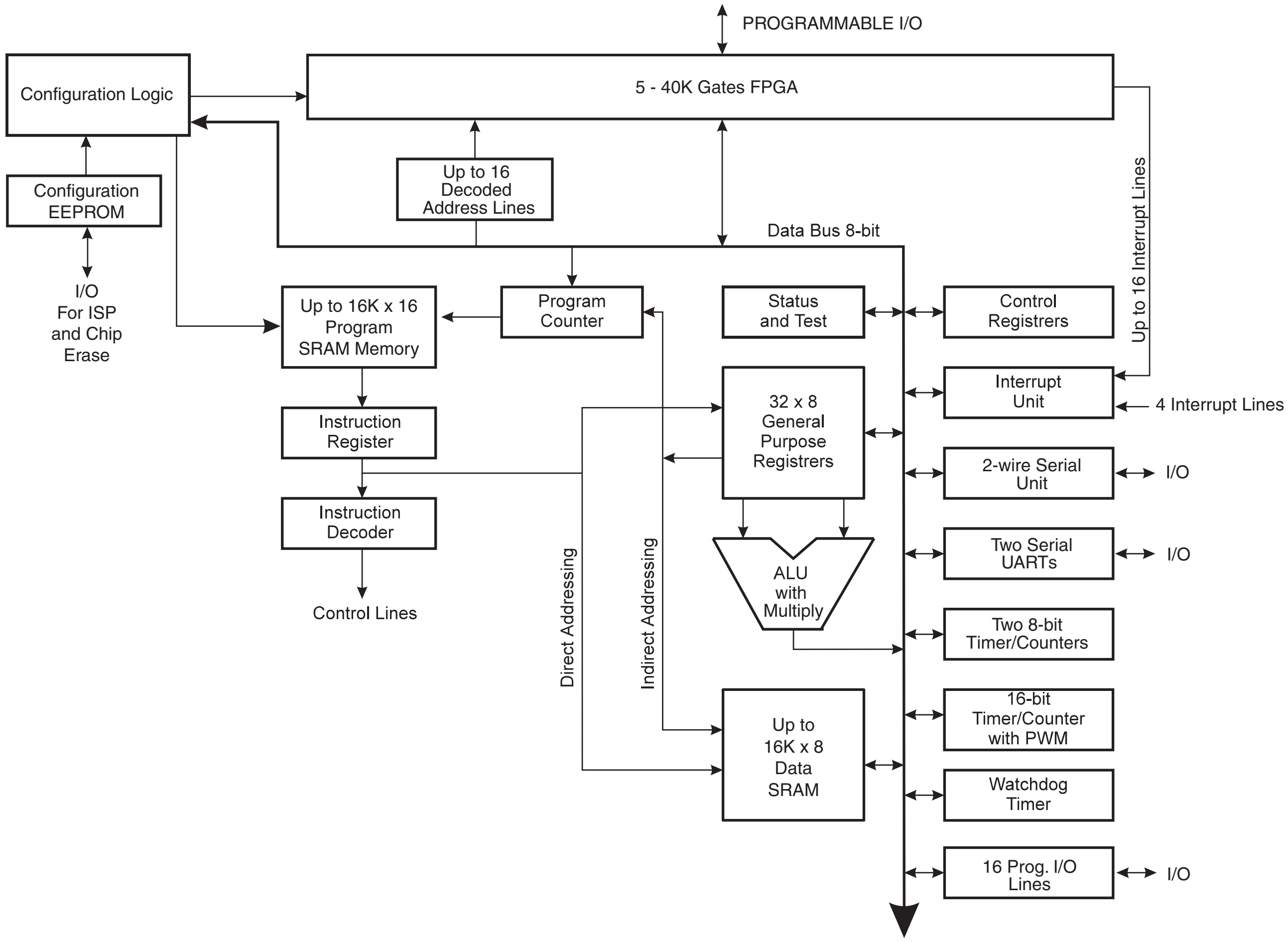
The AT94S Series (Secure FPSLIC family) shown in Table 1-1 is a combination of the popular Atmel AT40K Series SRAM FPGAs, the AT17 Series Configuration Memories and the high-performance Atmel AVR 8-bit RISC microcontroller with standard peripherals. Extensive data and instruction SRAM as well as device control and management logic are included in this multi-chip module (MCM).

The embedded AT40K FPGA core is a fully 3.3V PCI-compliant, SRAM-based FPGA with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data) and 5,000 to 40,000 usable gates.

Table 1-1. The AT94S Series Family

Device		AT94S05AL	AT94S10AL	AT94S40AL
Configuration Memory Size		1 Mbit	1 Mbit	1 Mbit
FPGA Gates		5K	10K	40K
FPGA Core Cells		256	576	2304
FPGA SRAM Bits		2048	4096	18432
FPGA Registers (Total)		436	846	2862
Maximum FPGA User I/O		93	137	162
AVR Programmable I/O Lines		8	16	16
Program SRAM Bytes		4K - 16K	20K - 32K	20K - 32K
Data SRAM Bytes		4K - 16K	4K - 16K	4K - 16K
Hardware Multiplier (8-bit)		Yes	Yes	Yes
2-wire Serial Interface		Yes	Yes	Yes
UARTs		2	2	2
Watchdog Timer		Yes	Yes	Yes
Timer/Counters		3	3	3
Real-time Clock		Yes	Yes	Yes
JTAG ICE		Yes	Yes	Yes
Typical AVR Throughput	@ 25 MHz	19 MIPS	19 MIPS	19 MIPS
	@ 40 MHz	30 MIPS	30 MIPS	30 MIPS
Operating Voltage		3.0 - 3.6V	3.0 - 3.6V	3.0 - 3.6V

Figure 1-1. AT94S Architecture



The embedded AVR core achieves throughputs approaching 1 MIPS per MHz by executing powerful instructions in a single-clock-cycle, and allows system designers to optimize power consumption versus processing speed. The AVR core is based on an enhanced RISC architecture that combines a rich instruction set with 32 general-purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code-efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers at the same clock frequency. The AVR executes out of on-chip SRAM. Both the FPGA configuration SRAM and AVR instruction code SRAM are automatically loaded at system power-up using Atmel's in-system programmable AT17 Series EEPROM configuration memories, which are part of the AT94S Multi-chip Module (MCM).

State-of-the-art FPSLIC design tools, System Designer, were developed in conjunction with the FPSLIC architecture to help reduce overall time-to-market by integrating microcontroller development and debugging, FPGA development, place and route, and complete system co-verification in one easy-to-use software tool.

may only drive the cSDA line Low. The system must provide a small pull-up current (1 kΩ equivalent) for the cSDA line.

The MESSAGE FORMAT for read and write instructions consists of the bytes shown in "Bit Format" on page 5.

While writing, the programmer is responsible for issuing the instruction and data. While reading, the programmer issues the instruction and acknowledges the data from the Configurator as necessary.

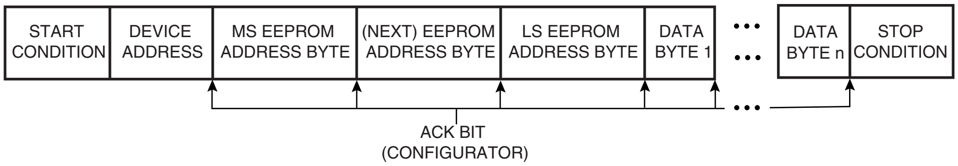
Again, the Acknowledge Bit is asserted on the cSDA line by the receiving device on a byte-by-byte basis.

The factory blanks devices to all zeros before shipping. The array cannot otherwise be "initialized" except by explicitly writing a known value to each location using the serial protocol described herein.

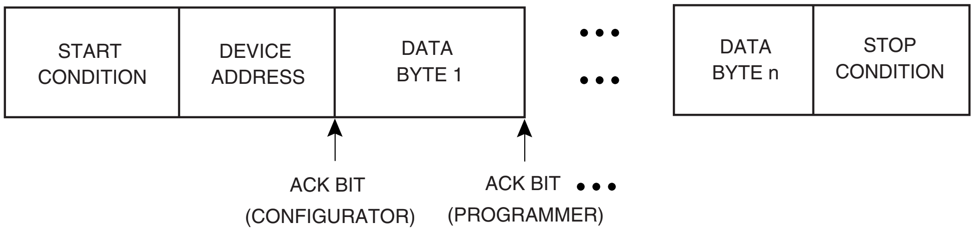
4.3 Bit Format

Data on the cSDA pin may change only during the cSCK Low time; whereas Start and Stop Conditions are identified as transitions during the cSCK High time.

Write Instruction Message Format



Current Address Read (Extended to Sequential Read) Instruction Message Format



4.4 Start and Stop Conditions

The Start Condition is indicated by a high-to-low transition of the cSDA line when the cSCK line is High. Similarly, the Stop Condition is generated by a low-to-high transition of the cSDA line when the cSCK line is High, as shown in Figure 4-1.

The Start Condition will return the device to the state where it is waiting for a Device Address (its normal quiescent mode).

The Stop Condition initiates an internally timed write signal whose maximum duration is t_{WR} (refer to AC Characteristics table for actual value). During this time, the Configurator must remain in programming mode (i.e., $\overline{\mathrm{SER\_EN}}$ is driven Low). cSDA and cSCK lines are ignored until the cycle is completed. Since the write cycle typically completes in less than t_{WR} seconds, we recommend the use of "polling" as described in later sections. Input levels to all other pins should be held constant until the write cycle has been completed.

4.5 Acknowledge Bit

The Acknowledge (ACK) Bit shown in Figure 4-1 is provided by the Configurator receiving the byte. The receiving Configurator can accept the byte by asserting a Low value on the cSDA line, or it can refuse the byte by asserting (allowing the signal to be externally pulled up to) a High value on the cSDA line. All bytes from accepted messages must be terminated by either an Acknowledge Bit or a Stop Condition. Following an ACK Bit, when the cSDA line is released during an exchange of control between the Configurator and the programmer, the cSDA line may be pulled High temporarily due to the open-collector output nature of the line. Control of the line must resume before the next rising edge of the clock.

4.6 Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on the cSDA line for the Device Address Byte and the EEPROM Address Bytes. It is followed by the lesser significant bits until the eighth bit, the least significant bit, is transmitted. However, for Data Bytes (both writing and reading), the first bit transmitted is the least significant bit. This protocol is shown in the diagrams below.

4.7 Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device.

The $\overline{\text{CE}}$ pin cannot be used for device selection in programming mode (i.e., when $\overline{\text{SER\_EN}}$ is drive Low).

Figure 4-1. Start and Stop Conditions

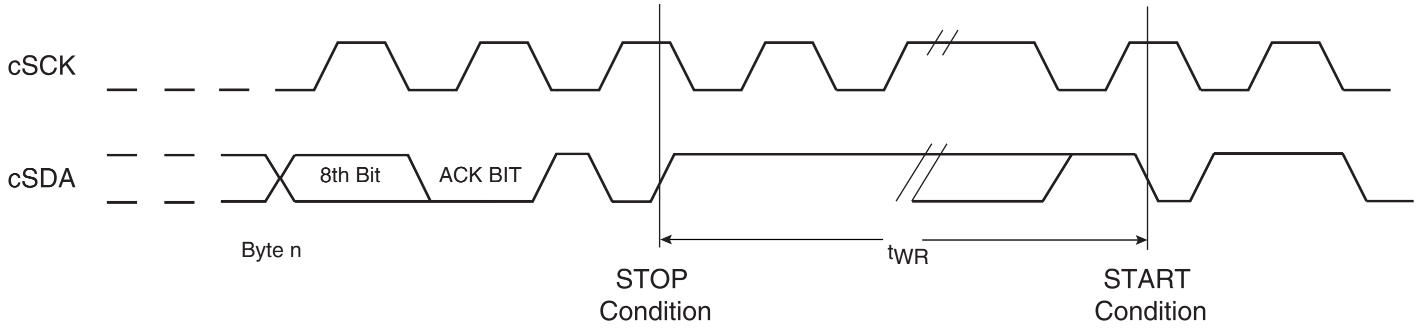
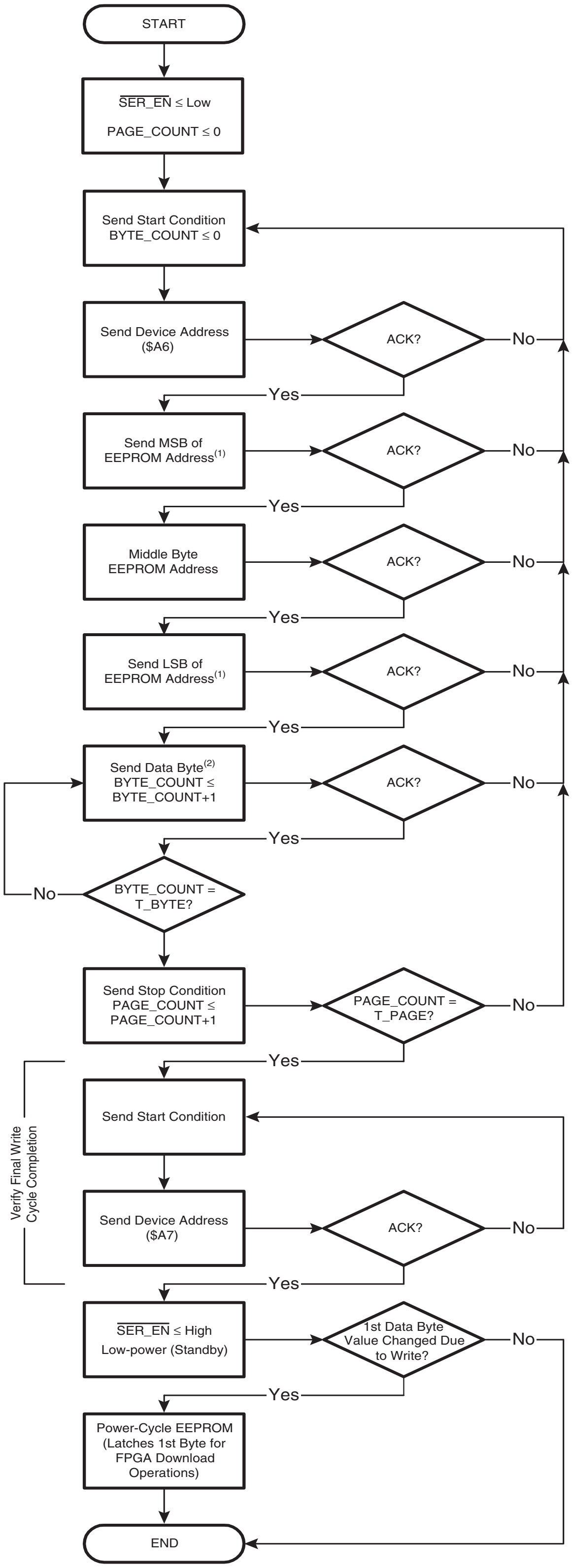


Table 4-1. Device Address Byte

MSB							LSB
1	0	1	0	0	1	1	R/$\overline{\text{W}}$
1st	2nd	3rd	4th	5th	6th	7th	8th

```
Where:R/W=1 Read
        = 0 Write
```

4.8 Programming Summary: Write to Whole Device



Notes:
1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.
2. Data byte received/sent LSB to MSB.

4.8.1 EEPROM Address is Defined as:

AT17LV010 0000 $000x_9$ $x_8x_7x_6x_5$ $x_4x_3x_2x_1$ x_0000 0000

Note: where X_n ... X_0 is (PAGE_COUNT)\b

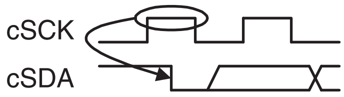
4.8.2 T_BYTE

AT17LV010	128

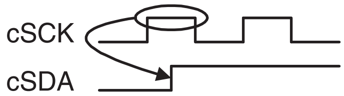
4.8.3 T_PAGE

AT17LV010	1024

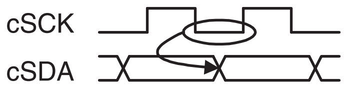
START CONDITION



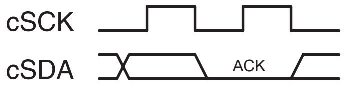
STOP CONDITION



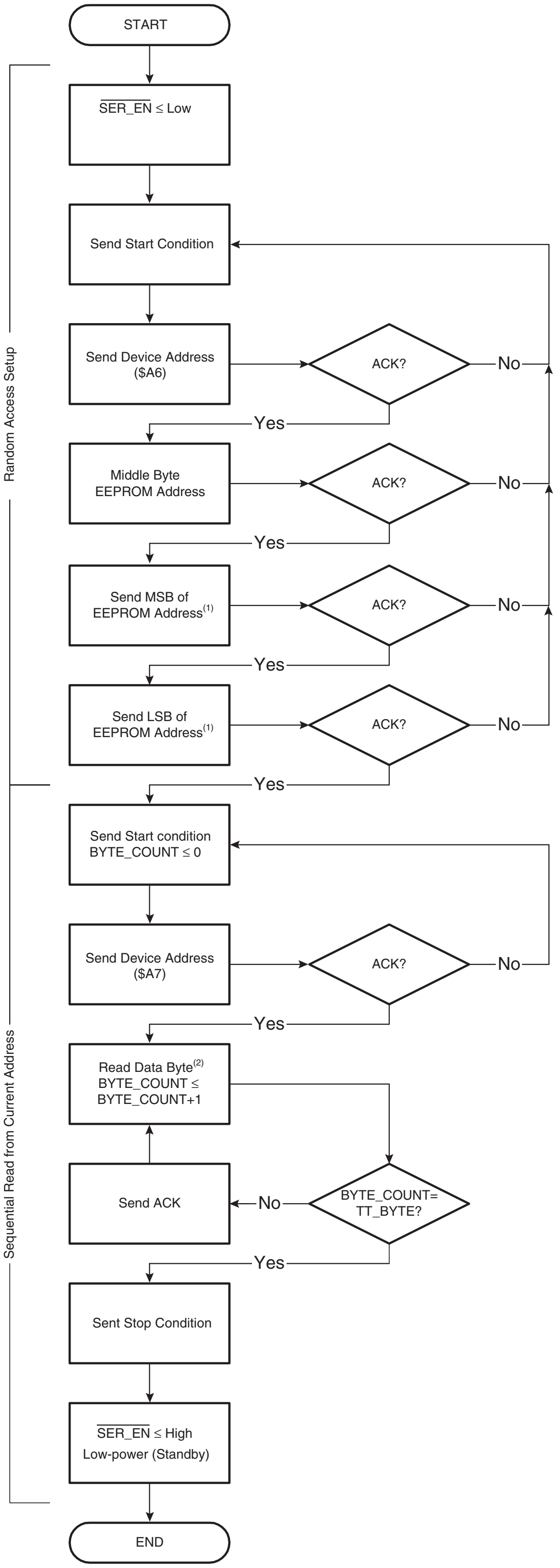
DATA BIT



ACK BIT



4.9 Programming Summary: Read from Whole Device



Notes:
1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.
2. Data byte received/sent LSB to MSB

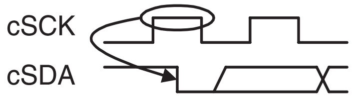
4.9.1 EEPROM Address is Defined as:

AT17LV010	00 00 00 \h

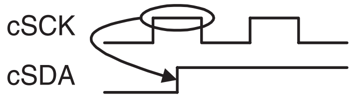
4.9.2 TT_BYTE

AT17LV010	131072 \d

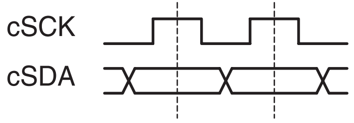
START CONDITION



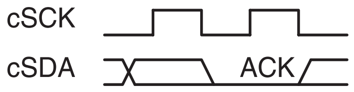
STOP CONDITION



SAMPLE DATA BIT



ACK BIT



4.9.3 Data Byte

LSB							MSB
D0	D1	D2	D3	D4	D5	D6	D7
1st	2nd	3rd	4th	5th	6th	7th	8th

The organization of the Data Byte is shown above. Note that in this case, the Data Byte is clocked into the device LSB first and MSB last.

4.9.4 Writing

Writing to the normal address space takes place in pages. A page is 128-bytes long in the 1-Mbit part. The page boundaries are, respectively, addresses where A_{E0} down to A_{EOS} are all zero, and A_{E6} down to A_{E0} are all zero. Writing can start at any address within a page and the number of bytes written must be 128 for the 1-Mbit part. The first byte is written at the transmitted address. The address is incremented in the Configurator following the receipt of each Data Byte. Only the lower 7 bits of the address are incremented. Thus, after writing to the last byte address within the given page, the address will roll over to the first byte address of the same page. A Write Instruction consists of:

- a Start Condition
- a Device Address Byte with $R/\overline{W}$ = 0
  - An Acknowledge Bit from the Configurator
- MS Byte of the EEPROM Address
  - An Acknowledge Bit from the Configurator
- Next Byte of the EEPROM Address
  - An Acknowledge Bit from the Configurator
- LS Byte of EEPROM Address
  - An Acknowledge Bit from the Configurator
- One or more Data Bytes (sent to the Configurator)
  - Each followed by an Acknowledge Bit from the Configurator
- a Stop Condition

4.9.4.1 Write Polling

On receipt of the Stop Condition, the Configurator enters an internally-timed write cycle. While the Configurator is busy with this write cycle, it will not acknowledge any transfers. The programmer can start the next page write by sending the Start Condition followed by the Device Address, in effect polling the Configurator. If this is not acknowledged, then the programmer should abandon the transfer without asserting a Stop Condition. The programmer can then repeatedly initiate a write instruction as above, until an acknowledge is received. When the Acknowledge Bit is received, the write instruction should continue by sending the first EEPROM Address Byte to the Configurator.

An alternative to write polling would be to wait a period of t_{WR} before sending the next page of data or exiting the programming mode. All signals must be maintained during the entire write cycle.

4.9.5 Reading

Read instructions are initiated similarly to write instructions. However, with the R/$\overline{W}$ bit in the Device Address set to one. There are three variants of the read instruction: current address read, random read and sequential read.

For all reads, it is important to understand that the internal Data Byte address counter maintains the last address accessed during the previous read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode (i.e., $\overline{\text{SER\_EN}}$ is driven Low). If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the last byte address in the page, the incremented address n + 1 would “roll over” to the first byte address on the next page.

4.9.5.1 *Current Address Read*

Once the Device Address (with the R/$\overline{W}$ select bit set to High) is clocked in and acknowledged by the Configurator, the Data Byte at the current address is serially clocked out by the Configurator in response to the clock from the programmer. The programmer generates a Stop Condition to accept the single byte of data and terminate the read instruction.

```
A Current Address Read instruction consists of
    a Start Condition
    a Device Address with R/$\overline{W}$ = 1
      An Acknowledge Bit from the Configurator
    a Data Byte from the Configurator
    a Stop Condition from the programmer.
```

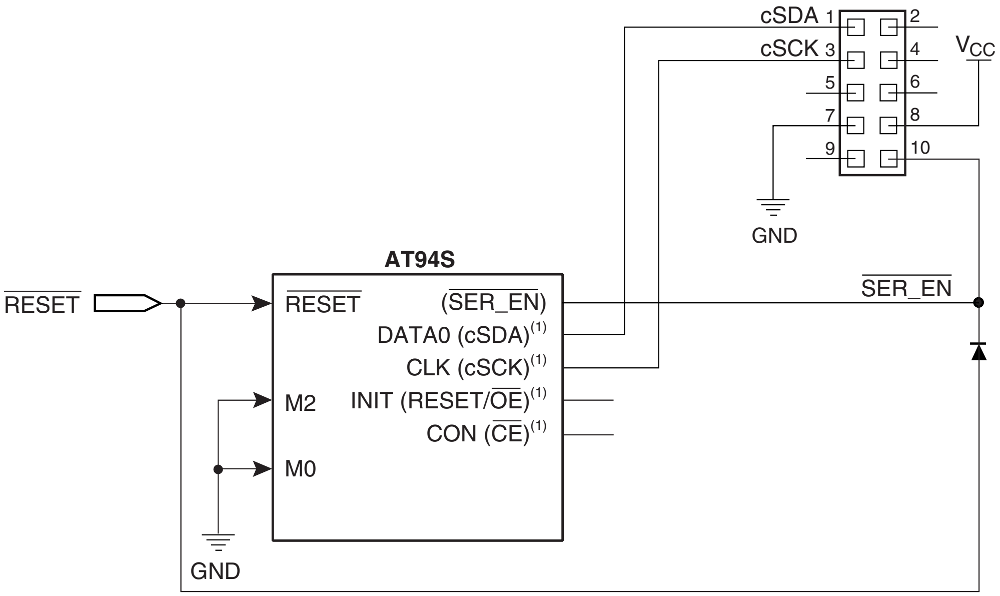
4.9.5.2 *Random Read*

A Random Read is a Current Address Read preceded by an aborted write instruction. The write instruction is only initiated for the purpose of loading the EEPROM Address Bytes. Once the Device Address Byte and the EEPROM Address Bytes are clocked in and acknowledged by the Configurator, the programmer immediately initiates a Current Address Read.

A Random Address Read instruction consists of :

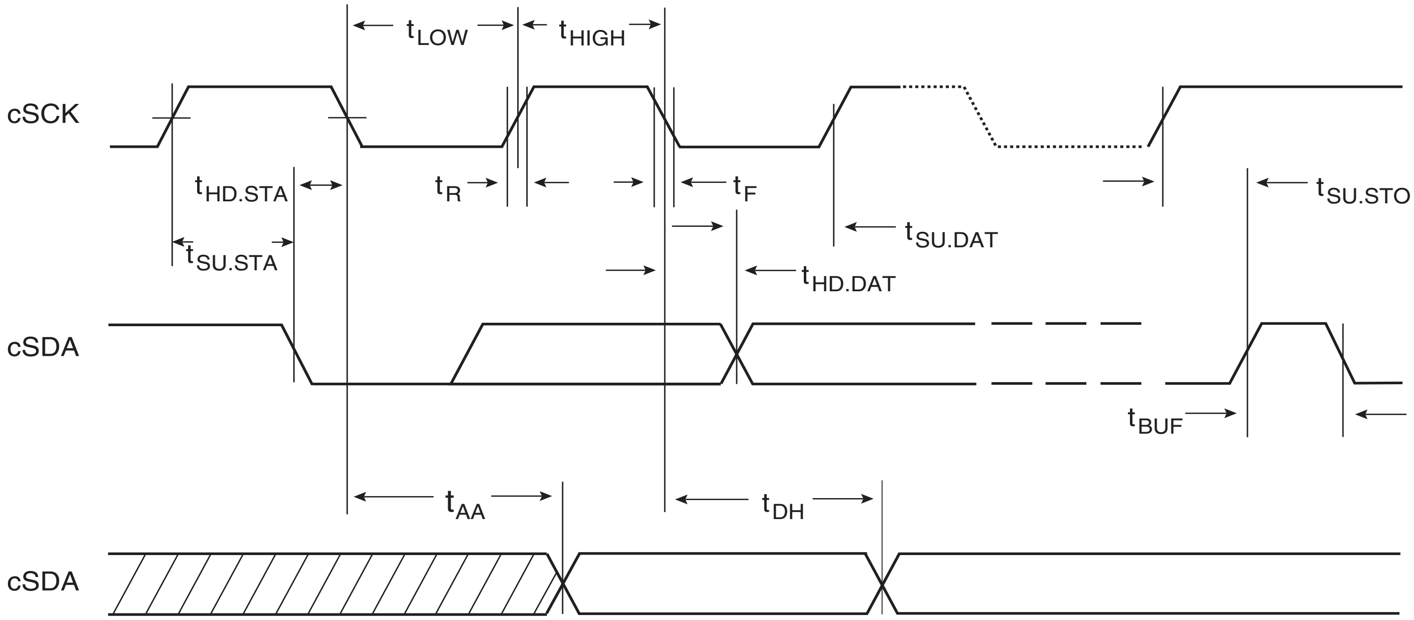
```
a Start Condition
a Device Address with R/$\overline{W}$ = 0
  An Acknowledge Bit from the Configurator
MS Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
Next Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
LS Byte of EEPROM Address
  An Acknowledge bit from the Configurator
a Start Condition
a Device Address with R/$\overline{W}$ = 1
  An Acknowledge Bit from the Configurator
a Data Byte from the Configurator
a Stop Condition from the programmer.
```

Figure 4-3. ISP of the AT17LV512/010 in an AT94S FPSLIC Application



Note: 1. Configurator signal names are shown in parenthesis.

Figure 4-4. Serial Data Timing Diagram



4.11 DC Characteristics(1)

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C(2)(3)(4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Supply Current	V_{CC} = 3.6		2	3	mA
I_{LL}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.2	V
V_{OL}	Output Low-level Voltage	I_{OL} = 2.1 mA			0.4	V

Notes:
1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

4.12 AC Characteristics(1)

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C(2)(3)(4)

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		100	KHz
t_{LOW}	Clock Pulse Width Low	4		µs
t_{HIGH}	Clock Pulse Width High	4		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.5		µs
$t_{HD;STA}$	Start Hold Time	2		µs
$t_{SU;STA}$	Start Setup Time	2		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Setup Time	0.2		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	2		µs
t_{DH}	Data Out Hold Time	0.1		µs
t_{WR}	Write Cycle Time		20	ms

Notes:
1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

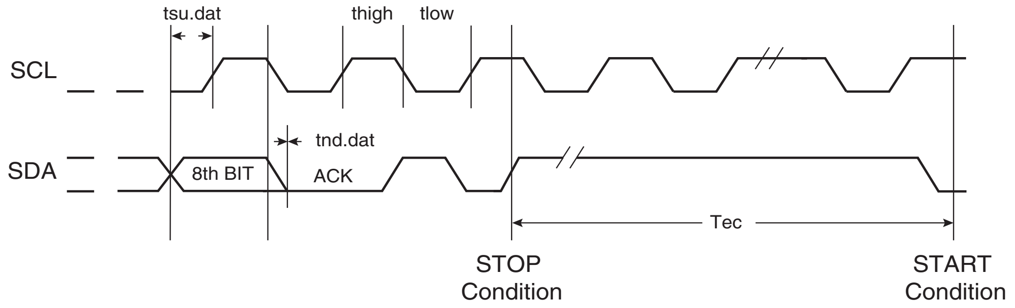
4.15 Chip Erase Timing

The entire device can be erased at once by writing to a specific address. This operation will erase the entire array. See Table 4-2 for specifics on the write algorithm.

Table 4-2. Chip Erase Cycle Characteristics

Symbol	Parameter
Tec	Chip Erase Cycle Time (25 ms)

Figure 4-5. Chip Erase Timing Diagram



5. Packaging and Pin List information

Table 5-1. Part and Package Combinations Available

Part #	Package	AT94S05	AT94S10	AT94S40
BG256	DG	93	137	162
LQ144	BQ	–	84	84

Table 5-2. AT94K JTAG ICE Pin List

Pin	AT94S05 96 FPGA I/O	AT94S10 192 FPGA I/O	AT94S40 384 FPGA I/O
TDI	IO34	IO50	IO98
TDO	IO38	IO54	IO102
TMS	IO43	IO63	IO123
TCK	IO44	IO64	IO124

Table 5-3. AT94S Pin List (Continued)

AT94S05 **96 FPGA I/O**	**AT94S10** **144 FPGA I/O**	**AT94S40** **288 FPGA I/O**	**Package**	
			Chip Array 256 CABGA	**LQ144**(1)
NC	I/O31	I/O67	L2	
NC	I/O32	I/O68	L5	
I/O21 (A26)	I/O33 (A26)	I/O69 (A26)	L4	23
I/O22 (A27)	I/O34 (A27)	I/O70 (A27)	M1	24
I/O23	I/O35	I/O71	M2	25
I/O24, FCK2	I/O36, FCK2	I/O72, FCK2	N1	26
		I/O73		
		I/O74		
	I/O37	I/O75		
	I/O38	I/O76		
		I/O77		
		I/O78		
		I/O79		
		I/O80		
I/O25	I/O39	I/O81	M3	
I/O26	I/O40	I/O82	N2	
	I/O41	I/O83		
	I/O42	I/O84		
		I/O85		
		I/O86		
		I/O87		
		I/O88		
I/O27 (A28)	I/O43 (A28)	I/O89 (A28)	P1	28
I/O28	I/O44	I/O90	P2	29
		I/O91		
		I/O92		
I/O29	I/O45	I/O93	R1	30
I/O30	I/O46	I/O94	N3	31
I/O31 ($\overline{\text{OTS}}$)	I/O47 ($\overline{\text{OTS}}$)	I/O95 ($\overline{\text{OTS}}$)	T1	32
I/O32, GCK2 (A29)	I/O48, GCK2 (A29)	I/O96, GCK2 (A29)	P3	33
AVRRESET	$\overline{\text{AVRRESET}}$	$\overline{\text{AVRRESET}}$	R2	34
M0	M0	M0	R3	36
FPSLIC Array				
M2	M2	M2	T3	38

Table 5-3. AT94S Pin List (Continued)

AT94S05 **96 FPGA I/O**	**AT94S10** **144 FPGA I/O**	**AT94S40** **288 FPGA I/O**	**Package**	
			Chip Array 256 **CABGA**	**LQ144**[(1)]
		I/O130		
		I/O131		
		I/O132		
		I/O133		
		I/O134		
NC	I/O67	I/O135	M8	
NC	I/O68	I/O136	R8	
I/O45	I/O69	I/O137	P8	50
I/O46	I/O70	I/O138	N8	51
		I/O139		
		I/O140		
		I/O141		
		I/O142		
I/O47 (TD7)	I/O71 (TD7)	I/O143 (TD7)	L8	52
I/O48 (InitErr) RESET/$\overline{\text{OE}}$	I/O72 (InitErr) RESET/$\overline{\text{OE}}$	I/O144 (InitErr) RESET/$\overline{\text{OE}}$	K9	53
I/O49 (TD6)	I/O73 (TD6)	I/O145 (TD6)	P9	56
I/O50 (TD5)	I/O74 (TD5)	I/O146 (TD5)	N9	57
		I/O147		
		I/O148		
		I/O149		
		I/O150		
I/O51	I/O75	I/O151	M9	58
I/O52	I/O76	I/O152	L9	59
NC	I/O77	I/O153	J9	
NC	I/O78	I/O154	T10	
		I/O155		
		I/O156		
		I/O157		
		I/O158		
		I/O159		
		I/O160		
		I/O161		
		I/O162		
NC	I/O79	I/O163	P10	

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package Chip Array 256 CABGA	Package LQ144[(1)]
NC	I/O80	I/O164	N10	
I/O53 (TD4)	I/O81 (TD4)	I/O165 (TD4)	L10	60
I/O54 (TD3)	I/O82 (TD3)	I/O166 (TD3)	T11	61
I/O55	I/O83	I/O167	R11	62
I/O56	I/O84	I/O168	M11	63
NC	NC	I/O169	N11	
NC	NC	I/O170	T12	
NC	I/O85	I/O171	R12	
NC	I/O86	I/O172	T13	
		I/O173		
		I/O174		
		I/O175		
		I/O176		
NC	I/O87	I/O177	N12	
NC	I/O88	I/O178	P12	
I/O57	I/O89	I/O179	R13	
I/O58	I/O90	I/O180	T14	
NC	NC	I/O181	N13	
NC	NC	I/O182	P13	
I/O59 (TD2)	I/O91 (TD2)	I/O183 (TD2)	T16	65
I/O60 (TD1)	I/O92 (TD1)	I/O184 (TD1)	P14	66
		I/O185		
		I/O186		
		I/O187		
		I/O188		
I/O61	I/O93	I/O189	R16	67
I/O62	I/O94	I/O190	P15	68
I/O63 (TD0)	I/O95 (TD0)	I/O191 (TD0)	N14	69
I/O64, GCK4	I/O96, GCK4	I/O192, GCK4	P16	70
$\overline{\text{CON}}$/CE	$\overline{\text{CON}}$/CE	$\overline{\text{CON}}$/CE	N16	72
FPSLIC Array				
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	M14	74
PE0	PE0	PE0	M12	75
PE1	PE1	PE1	M15	76

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[(1)]
		I/O321		
		I/O322		
		I/O323		
		I/O324		
I/O107 (A4)	I/O161 (A4)	I/O325 (A4)	A10	121
I/O108 (A5)	I/O162 (A5)	I/O326 (A5)	G10	122
NC	I/O163	I/O327	G9	
NC	I/O164	I/O328	F9	
I/O109	I/O165	I/O329	E9	123
I/O110	I/O166	I/O330	C9	124
		I/O331		
		I/O332		
		I/O333		
		I/O334		
I/O111 (A6)	I/O167 (A6)	I/O335 (A6)	B9	125
I/O112 (A7)	I/O168 (A7)	I/O336 (A7)	A9	126
I/O113 (A8)	I/O169 (A8)	I/O337 (A8)	A8	129
I/O114 (A9)	I/O170 (A9)	I/O338 (A9)	B8	130
		I/O339		
		I/O340		
		I/O341		
		I/O342		
I/O115	I/O171	I/O343	C8	131
I/O116	I/O172	I/O344	D8	132
NC	I/O173	I/O345	E8	
NC	I/O174	I/O346	F8	
I/O117 (A10)	I/O175 (A10)	I/O347 (A10)	H8	133
I/O118 (A11)	I/O176 (A11)	I/O348 (A11)	A7	134
NC	NC	I/O349	C7	
NC	NC	I/O350	D7	
		I/O351		
		I/O352		
		I/O353		
		I/O354		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[(1)]
		I/O355		
		I/O356		
NC	I/O177	I/O357	F7	
NC	I/O178	I/O358	A6	
I/O119	I/O179	I/O359	F6	135
I/O120	I/O180	I/O360	B6	136
		I/O361		
		I/O362		
NC	I/O181	I/O363	D6	
NC	I/O182	I/O364	E6	
		I/O365		
		I/O366		
		I/O367		
		I/O368		
I/O121	I/O183	I/O369	A5	
I/O122	I/O184	I/O370	B5	
I/O123 (A12)	I/O185 (A12)	I/O371 (A12)	E5	138
I/O124 (A13)	I/O186 (A13)	I/O372 (A13)	C5	139
		I/O373		
		I/O374		
		I/O375		
		I/O376		
		I/O377		
		I/O378		
NC	I/O187	I/O379	A4	
NC	I/O188	I/O380	B4	
I/O125	I/O189	I/O381	A3	140
I/O126	I/O190	I/O382	C4	141
I/O127 (A14)	I/O191 (A14)	I/O383 (A14)	B3	142
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O384, GCK8 (A15)	A2	143

Note: 1. LQ144 is only offered in the AT94S10 and AT94S40.

Table 5-4. 256 CABGA and LQ144 V_{DD}, V_{CC} and GND Pins(1)

Package	V_{DD} (core)	V_{CC} (I/O)	GND
256 CABGA	D14, E7, F12, G3, H9, K10, L13, M13, P4, T9	B2, G8, G13, H10, K13, L3, M10, R14, T3, T7	B11, B13, B16, B7, C3, C6, D5, D9, F11, F13, T15, F16, F2, F5, G16, H11, H16, J15, J2, K16, K3, T2, L14, L16, L7, M4, N15, N4, N6, P11, R9, R10, R15, T8
LQ144	18, 54, 90, 128	37, 73, 108, 144	1, 8, 17, 27, 35, 45, 55, 64, 71, 91, 100, 110, 118, 127, 137

Note: 1. For power rail support for product migration to lower-power devices, refer to the "Designing in Split Power Supply Support for AT94KAL/AX and AT94SAL/AX Devices" application note (doc2308.pdf), available on the Atmel web site, at http://www.atmel.com/dyn/products/app_notes.asp?family_id=627.

6. Thermal Coefficient Table

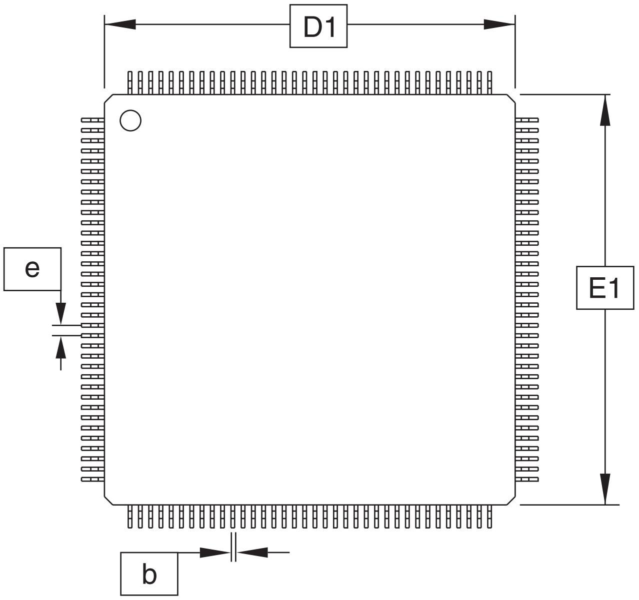
Package Style	Lead Count	Theta J-A [°C/W] 0 LFPM	Theta J-A [°C/W] 225 LFPM	Theta J-A [°C/W] 500 LPFM
CABGA	256	27	23	20
LQFP	144	35	—	—

7. Ordering Information

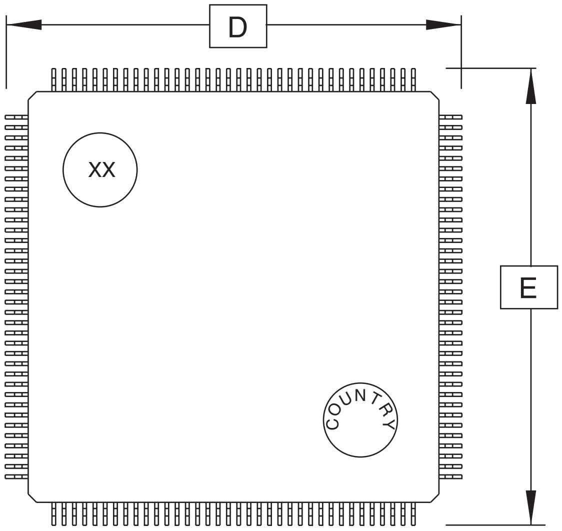
Usable Gates	Speed Grade	Ordering Code	Package	Operation Range
5,000	25 MHz	AT94S05AL-25DGC AT94S05AL-25BQC	256ZA 144L1	Commercial (0°C - 70°C)
		AT94S05AL-25DGI AT94S05AL-25BQI	256ZA 144L1	Industrial (-40°C - 85°C)
10,000	25 MHz	AT94S10AL-25DGC	256ZA	Commercial (0°C - 70°C)
		AT94S10AL-25BQC	144L1	
		AT94S10AL-25DGI	256ZA	Industrial (-40°C - 85°C)
		AT94S10AL-25BQI	144L1	
40,000	16 MHz	AT94S40AL-25DGC	256ZA	Commercial (0°C - 70°C)
		AT94S40AL-25DGI	256ZA	Industrial (-40°C - 85°C)

Package Type	
256ZA	256-ball, Chip Array Ball Grid Array Package (CABGA)
144L1	144-lead, Low Profile Plastic Gull Wing Quad Flat Package (LQFP)

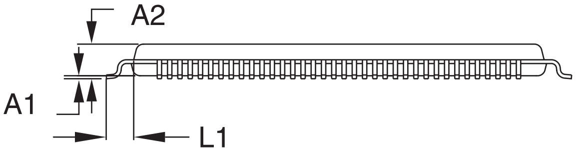
8.2 144L1 – LQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D		22.00 BSC		
D1		20.00 BSC		2, 3
E		22.00 BSC		
E1		20.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**144L1**, 144-lead (20 x 20 x 1.4 mm Body), Low Profile Plastic Quad Flat Pack (LQFP)	144L1	A

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