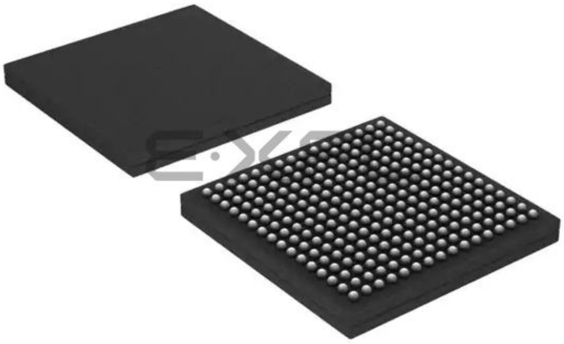
Microchip Technology - AT94S10AL-25DGI Datasheet



Embedded - FPGAs (Field Programmable Gate Array) with Microcontrollers: Enhancing Flexibility and Performance

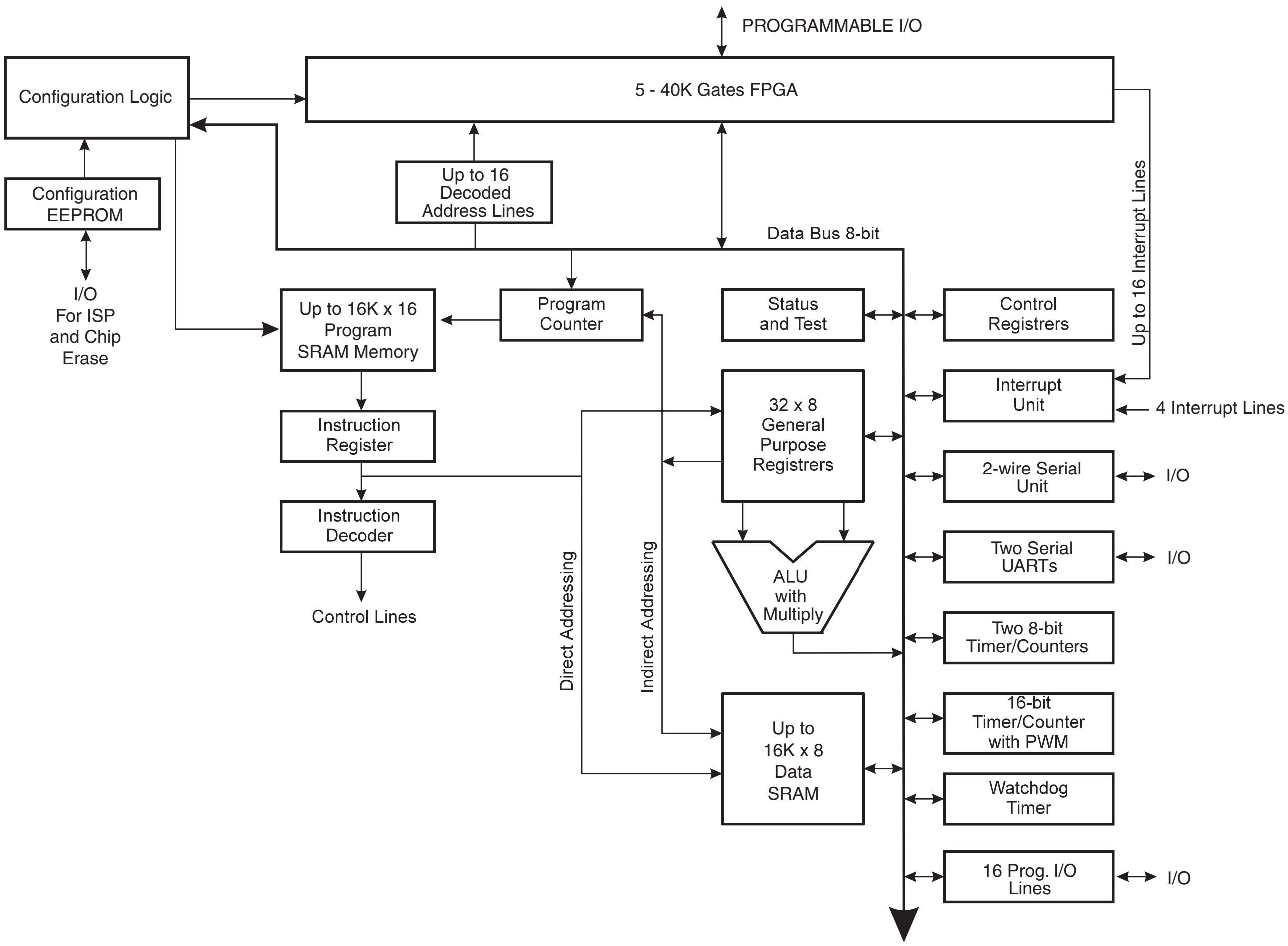
Embedded - FPGAs (Field Programmable Gate Arrays) with Microcontrollers represent a cutting-edge category of electronic components that combine the flexibility of FPGA technology with the processing power of integrated microcontrollers. This hybrid approach offers a versatile solution for designing and implementing complex digital systems that require both programmable logic and embedded processing capabilities.

What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	20K-32K
FPGA SRAM	4kb
EEPROM Size	512K x 8
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	576
FPGA Gates	10K
FPGA Registers	846
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C
Package / Case	256-LBGA, CABGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94s10al-25dgi

Figure 1-1. AT94S Architecture



The embedded AVR core achieves throughputs approaching 1 MIPS per MHz by executing powerful instructions in a single-clock-cycle, and allows system designers to optimize power consumption versus processing speed. The AVR core is based on an enhanced RISC architecture that combines a rich instruction set with 32 general-purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code-efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers at the same clock frequency. The AVR executes out of on-chip SRAM. Both the FPGA configuration SRAM and AVR instruction code SRAM are automatically loaded at system power-up using Atmel's in-system programmable AT17 Series EEPROM configuration memories, which are part of the AT94S Multi-chip Module (MCM).

State-of-the-art FPSLIC design tools, System Designer, were developed in conjunction with the FPSLIC architecture to help reduce overall time-to-market by integrating microcontroller development and debugging, FPGA development, place and route, and complete system co-verification in one easy-to-use software tool.

2. Internal Architecture

For details of the AT94S Secure FPSLIC architecture, please refer to the AT94K FPSLIC datasheet and the AT17 Series Configuration Memory datasheet, available on the Atmel web site at http://www.atmel.com. This document only describes the differences between the AT94S Secure FPSLIC and the AT94K FPSLIC.

3. FPSLIC and Configurator Interface

- Fully In-System Programmable and Re-programmable
- When Security Bit Set:
  - Data Verification Disabled
  - Data Transfer to FPSLIC not Externally Visible
  - Secured EEPROM Will Only Boot the FPSLIC Device or Respond to a Chip Erase
- When Security Bit Cleared:
  - Entire Chip Erase Performed
  - In-System Programming Enabled
  - Data Verification Enabled

External Data pins allow for In-System Programming of the device and setting of the EEPROM-based security bit. When the security bit is set (active) this programming connection will only respond to a device erase command. Data cannot be read out of the external programming/data pins when the security bit is set. The part can be re-programmed, but only after first being erased.

4. Programming and Configuration Timing Characteristics

Atmel's Configurator Programming Software (CPS), available from the Atmel web site (http://www.atmel.com/dyn/products/tools_card.asp?tool_id=3191), creates the programming algorithm for the embedded configurator; however, if you are planning to write your own software or use other means to program the embedded configurator, the section below includes the algorithm and other details.

4.1 The FPSLIC Configurator

The FPSLIC Configurator is a serial EEPROM memory which is used to load programmable devices. This document describes the features needed to program the Configurator from within its programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low).

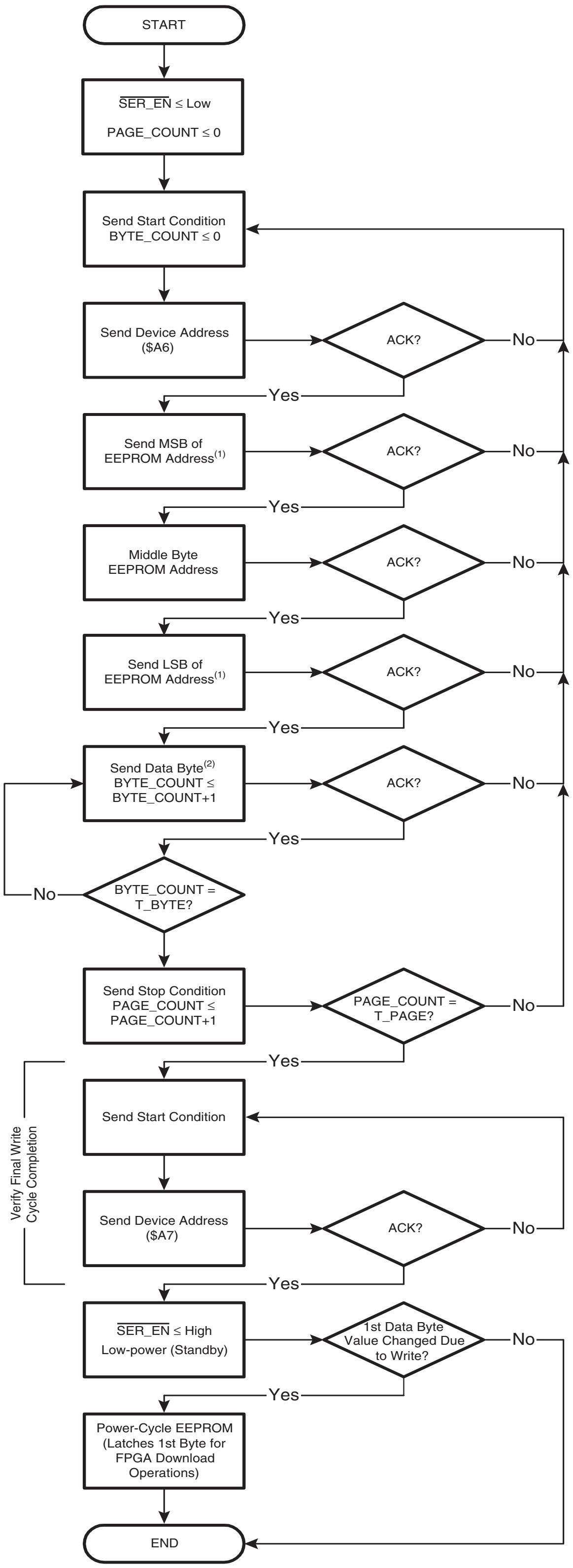
Reference schematics are supplied for ISP applications.

4.2 Serial Bus Overview

The serial bus is a two-wire bus; one wire (cSCK) functions as a clock and is provided by the programmer, the second wire (cSDA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a Start Condition and ends with a Stop Condition. The message consists of an integer number of bytes, each byte consisting of 8 bits of data, followed by a ninth Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted byte. This is possible because devices

4.8 Programming Summary: Write to Whole Device



Notes: 1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.

2. Data byte received/sent LSB to MSB.

4.8.1 EEPROM Address is Defined as:

AT17LV010 0000 $000x_9$ $x_8x_7x_6x_5$ $x_4x_3x_2x_1$ x_0000 0000

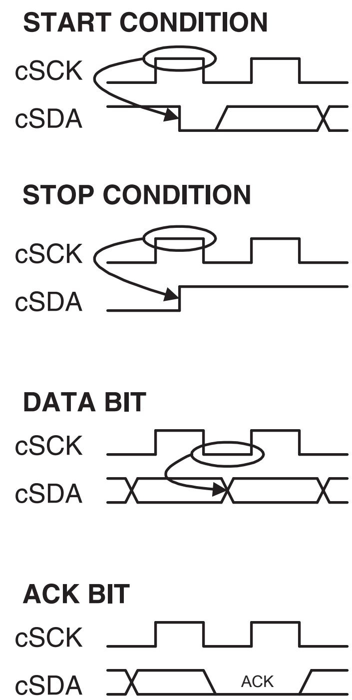
Note: where X_n ... X_0 is (PAGE_COUNT)\b

4.8.2 T_BYTE

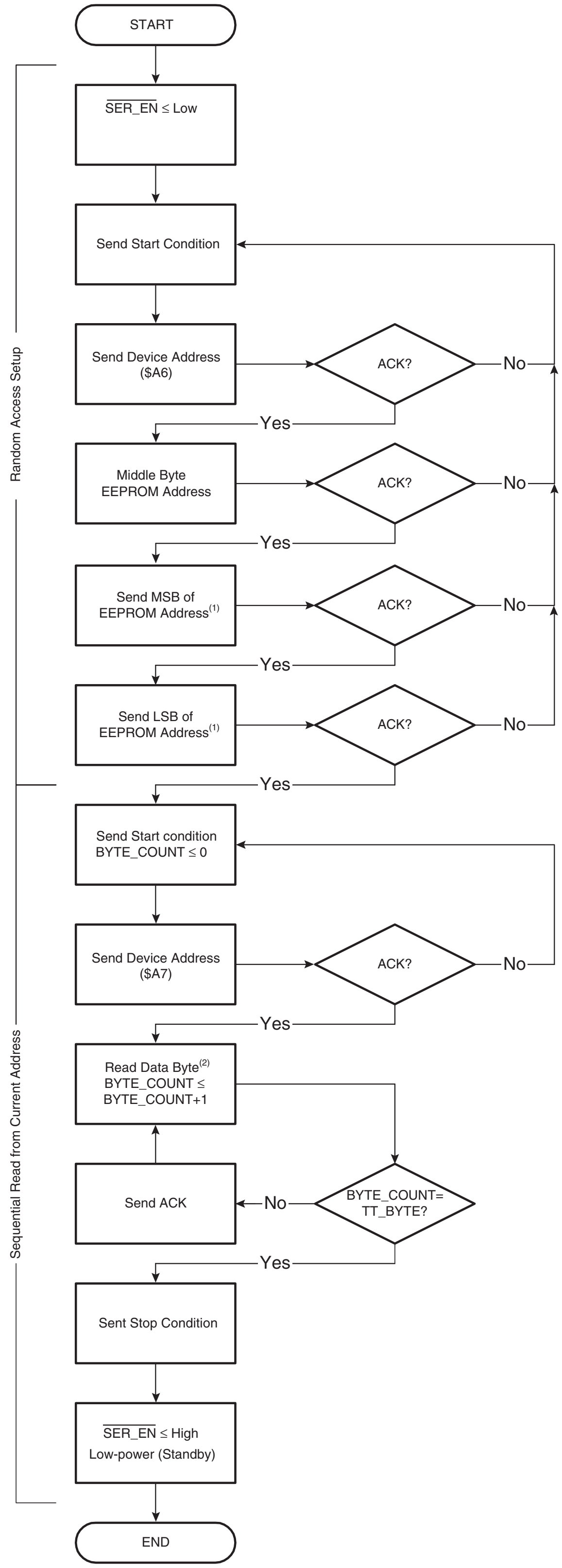
AT17LV010 128

4.8.3 T_PAGE

AT17LV010 1024



4.9 Programming Summary: Read from Whole Device



Notes: 1. The 1-Mbit part requires three EEPROM address bytes; all three bytes must be individually ACK'd by the EEPROM.

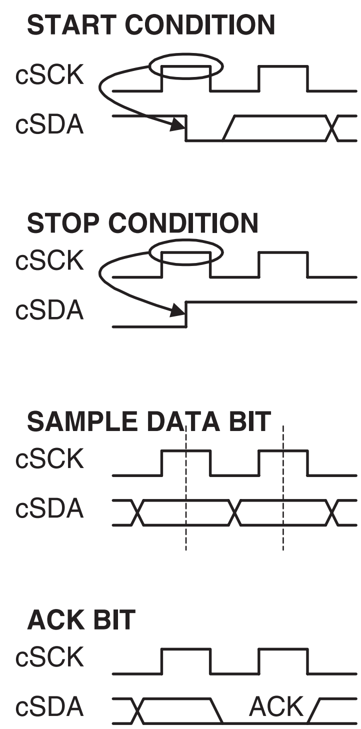
2. Data byte received/sent LSB to MSB

4.9.1 EEPROM Address is Defined as:

AT17LV010	00 00 00 \h

4.9.2 TT_BYTE

AT17LV010	131072 \d



4.9.3 Data Byte

LSB							MSB
D0	D1	D2	D3	D4	D5	D6	D7
1st	2nd	3rd	4th	5th	6th	7th	8th

The organization of the Data Byte is shown above. Note that in this case, the Data Byte is clocked into the device LSB first and MSB last.

4.9.4 Writing

Writing to the normal address space takes place in pages. A page is 128-bytes long in the 1-Mbit part. The page boundaries are, respectively, addresses where A_{E0} down to A_{EOS} are all zero, and A_{E6} down to A_{E0} are all zero. Writing can start at any address within a page and the number of bytes written must be 128 for the 1-Mbit part. The first byte is written at the transmitted address. The address is incremented in the Configurator following the receipt of each Data Byte. Only the lower 7 bits of the address are incremented. Thus, after writing to the last byte address within the given page, the address will roll over to the first byte address of the same page. A Write Instruction consists of:

```
a Start Condition
a Device Address Byte with R/W̅ = 0
  An Acknowledge Bit from the Configurator
MS Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
Next Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
LS Byte of EEPROM Address
  An Acknowledge Bit from the Configurator
One or more Data Bytes (sent to the
Configurator)
  Each followed by an Acknowledge Bit from the
  Configurator
a Stop Condition
```

4.9.4.1 Write Polling

On receipt of the Stop Condition, the Configurator enters an internally-timed write cycle. While the Configurator is busy with this write cycle, it will not acknowledge any transfers. The programmer can start the next page write by sending the Start Condition followed by the Device Address, in effect polling the Configurator. If this is not acknowledged, then the programmer should abandon the transfer without asserting a Stop Condition. The programmer can then repeatedly initiate a write instruction as above, until an acknowledge is received. When the Acknowledge Bit is received, the write instruction should continue by sending the first EEPROM Address Byte to the Configurator.

An alternative to write polling would be to wait a period of t_{WR} before sending the next page of data or exiting the programming mode. All signals must be maintained during the entire write cycle.

4.9.5 Reading

Read instructions are initiated similarly to write instructions. However, with the $R/\overline{W}$ bit in the Device Address set to one. There are three variants of the read instruction: current address read, random read and sequential read.

For all reads, it is important to understand that the internal Data Byte address counter maintains the last address accessed during the previous read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode (i.e., $\overline{\text{SER\_EN}}$ is driven Low). If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the last byte address in the page, the incremented address n + 1 would “roll over” to the first byte address on the next page.

4.9.5.1 Current Address Read

Once the Device Address (with the $R/\overline{W}$ select bit set to High) is clocked in and acknowledged by the Configurator, the Data Byte at the current address is serially clocked out by the Configurator in response to the clock from the programmer. The programmer generates a Stop Condition to accept the single byte of data and terminate the read instruction.

```
A Current Address Read instruction consists of
    a Start Condition
    a Device Address with R/W̄ = 1
      An Acknowledge Bit from the Configurator
    a Data Byte from the Configurator
    a Stop Condition from the programmer.
```

4.9.5.2 Random Read

A Random Read is a Current Address Read preceded by an aborted write instruction. The write instruction is only initiated for the purpose of loading the EEPROM Address Bytes. Once the Device Address Byte and the EEPROM Address Bytes are clocked in and acknowledged by the Configurator, the programmer immediately initiates a Current Address Read.

A Random Address Read instruction consists of :

```
a Start Condition
a Device Address with R/W̄ = 0
  An Acknowledge Bit from the Configurator
MS Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
Next Byte of the EEPROM Address
  An Acknowledge Bit from the Configurator
LS Byte of EEPROM Address
  An Acknowledge bit from the Configurator
a Start Condition
a Device Address with R/W̄ = 1
  An Acknowledge Bit from the Configurator
a Data Byte from the Configurator
a Stop Condition from the programmer.
```

4.9.5.3 *Sequential Read*

Sequential Reads follow either a Current Address Read or a Random Address Read. After the programmer receives a Data Byte, it may respond with an Acknowledge Bit. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached.[1] The Sequential Read instruction is terminated when the programmer does not respond with an Acknowledge Bit but instead generates a Stop Condition following the receipt of a Data Byte.

Note: 1. If an ACK is sent by the programmer after the data in the last memory address is sent by the configurator, the internal address counter will "rollover" to the first byte address of the memory array and continue to send data as long as an ACK is sent by the programmer.

4.9.6 Programmer Functions

The following programmer functions are supported while the Configurator is in programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low):

1. Read the Manufacturer's Code and the Device Code (optional for ISP).
2. Program the device.
3. Verify the device.

In the order given above, they are performed in the following manner.

4.9.7 Reading Manufacturer's and Device Codes

On AT17LV010 Configurator, the sequential reading of these bytes are accomplished by performing a Random Read at EEPROM Address 040000H.

The correct codes are:

```
Manufacturers Code -Byte 0     1E
Device Code       - Byte 1 F7   AT17LV010
```

Note: The Manufacturer's Code and Device Code are read using the byte ordering specified for Data Bytes; i.e., LSB first, MSB last.

4.9.8 Programming the Device

All the bytes in a given page must be written. The page access order is not important but it is suggested that the Configurator be written sequentially from address 0. Writing is accomplished by using the cSDA and cSCK pins.

4.9.8.1 *Important Note on AT94S Series Configurators Programming*

The first byte of data will not be cached for read back during FPGA Configuration (i.e., when $\overline{\text{SER\_EN}}$ is driven High) until the Configurator is power-cycled.

4.9.9 Verifying the Device

All bytes in the Configurator should be read and compared to their intended values. Reading is done using the cSDA and cSCK pins.

4.10 In-System Programming Applications

The AT94S Series Configurators are in-system (re)programmable (ISP). The example shown on the following page supports the following programmer functions:

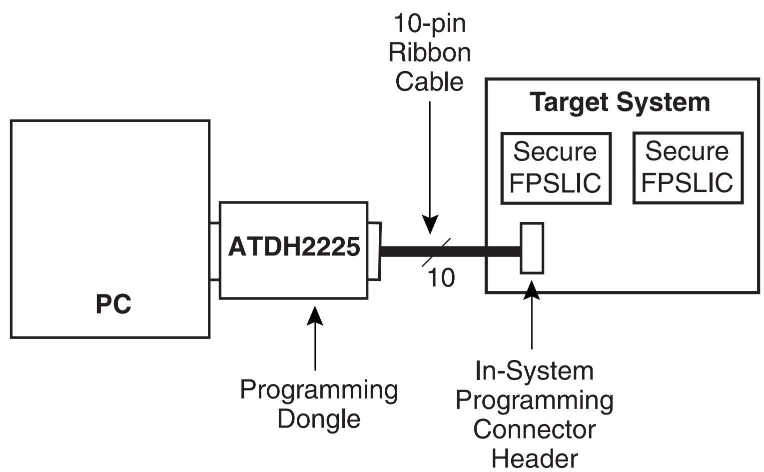
1. Read the Manufacturer's Code and the Device Code.
2. Program the device.
3. Verify the device data.

While Atmel's Secure FPSLIC Configurators can be programmed from various sources (e.g., on-board microcontrollers or PLDs), the applications shown here are designed to facilitate users of our ATDH2225 Configurator Programming Cable. The typical system setup is shown in Figure 4-2.

The pages within the configuration EEPROM can be selectively rewritten.

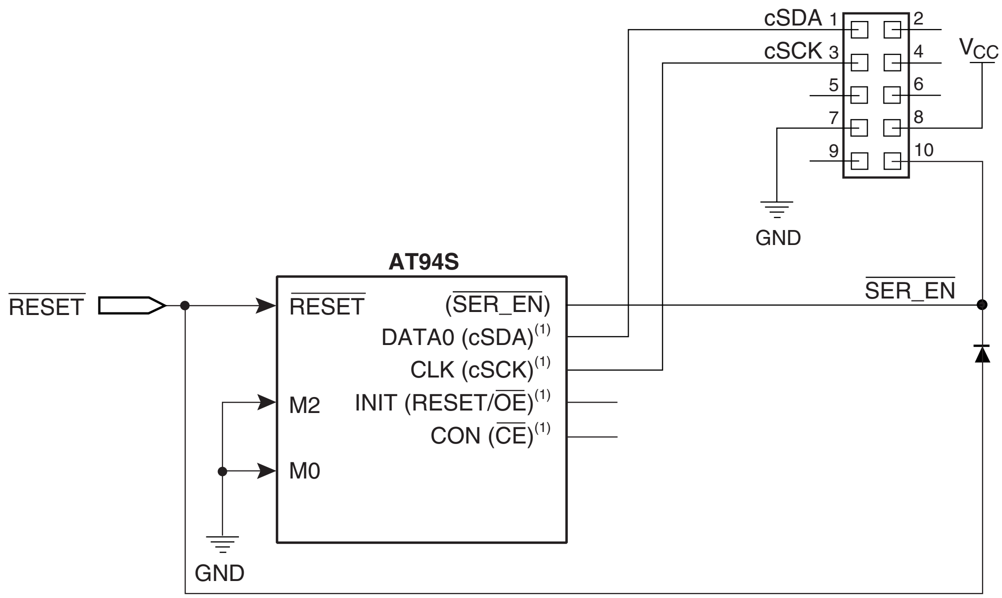
This document is limited to example implementations for Atmel's AT94S application.

Figure 4-2. Typical System Setup



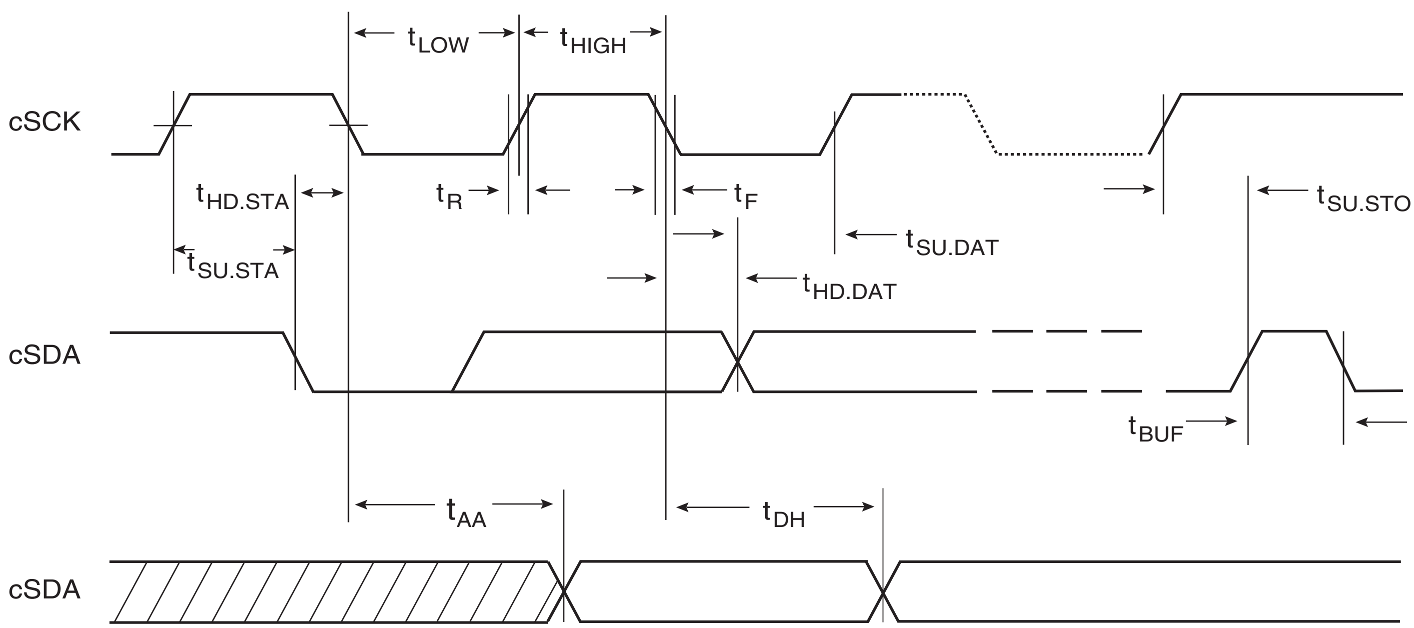
The diode connection between the AT94S' $\overline{\text{RESET}}$ pin and the $\overline{\text{SER\_EN}}$ signal allows the external programmer to force the FPGA into a reset state during ISP. This eliminates the potential for contention on the cSCK line. The pull-up resistors required on the lines to $\overline{\text{RESET}}$, CON and INIT are present on the inputs (internally) to the AT94S FPSLIC, see Figure 4-3.

Figure 4-3. ISP of the AT17LV512/010 in an AT94S FPSLIC Application



Note: 1. Configurator signal names are shown in parenthesis.

Figure 4-4. Serial Data Timing Diagram



4.11 DC Characteristics[1]

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C[2][3][4]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Supply Current	V_{CC} = 3.6		2	3	mA
I_{LL}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	10	µA
V_{IH}	High-level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage		-0.5		0.2	V
V_{OL}	Output Low-level Voltage	I_{OL} = 2.1 mA			0.4	V

Notes:
1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

4.12 AC Characteristics[1]

V_{CC} = 3.3V ± 10%, T_A = -40°C - 85°C[2][3][4]

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		100	KHz
t_{LOW}	Clock Pulse Width Low	4		µs
t_{HIGH}	Clock Pulse Width High	4		µs
t_{AA}	Clock Low to Data Out Valid	0.1	1	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.5		µs
$t_{HD;STA}$	Start Hold Time	2		µs
$t_{SU;STA}$	Start Setup Time	2		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Setup Time	0.2		µs
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		0.3	µs
$t_{SU\ STO}$	Stop Setup Time	2		µs
t_{DH}	Data Out Hold Time	0.1		µs
t_{WR}	Write Cycle Time		20	ms

Notes:
1. Specific to programming mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low)
2. Commercial temperature range 0°C - 70°C
3. Industrial temperature range -40°C - 85°C
4. This parameter is characterized and is not 100% tested.

4.13 Secure FPSLIC Configurator Pin Configurations

144-pin LQFP	256-pin CABGA	Name	I/O	Description
105	D16	cSDA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
107	C16	cSCK	O	CLOCK output. Used to increment the internal address and bit counter for reading and programming.
53	K9	RESET/$\overline{\text{OE}}$	I	RESET/$\overline{\text{OE}}$ input (when $\overline{\text{SER\_EN}}$ is High). A Low level on both the $\overline{\text{CE}}$ and RESET/$\overline{\text{OE}}$ inputs enables the data output driver. A High level on RESET/$\overline{\text{OE}}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{\text{OE}}$ or $\overline{\text{RESET}}$/OE. This document describes the pin as RESET/$\overline{\text{OE}}$.
72	N16	$\overline{\text{CE}}$	I	Chip Enable input. Used for device selection only when $\overline{\text{SER\_EN}}$ is High. A Low level on both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power mode. Note this pin will not enable/disable the device in the 2-wire Serial mode (i.e., when $\overline{\text{SER\_EN}}$ is driven Low).
81	M5	$\overline{\text{SER\_EN}}$	I	Serial enable is normally High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the programming mode.

4.14 Security Bit

Once the security bit is programmed, data will no longer output from the normal data pad. Once the fuse is set, any attempt to erase the fuse will cause the configurator to erase all of it contents.

4.14.1 AT17LV512/010 Security Bit Programming

4.14.1.1 Disabling the Security Bit

Write 4 bytes "00 00 00 00" to addresses 800000-800003 two consecutive times, using the previously defined 2-wire write algorithm. Thereafter, either cycle the power or toggle (HI-LO-HI) the $\overline{\text{SER\_EN}}$ pin in order to disable the security.

4.14.1.2 Enabling the Security Bit

Write 4 bytes "FF FF FF FF" to addresses 800000-800003 using the previously defined 2-wire write algorithm.

4.14.1.3 Verifying the Security Bit

Read 4 bytes of data from addresses 800000-800003 using the previously defined 2-wire Random Read algorithm. If the data is "FF FF FF FF", the security bit has been enabled. If the data is "00 00 00 00", the security bit has been disabled.

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[(1)]
NC	I/O31	I/O67	L2	
NC	I/O32	I/O68	L5	
I/O21 (A26)	I/O33 (A26)	I/O69 (A26)	L4	23
I/O22 (A27)	I/O34 (A27)	I/O70 (A27)	M1	24
I/O23	I/O35	I/O71	M2	25
I/O24, FCK2	I/O36, FCK2	I/O72, FCK2	N1	26
		I/O73		
		I/O74		
	I/O37	I/O75		
	I/O38	I/O76		
		I/O77		
		I/O78		
		I/O79		
		I/O80		
I/O25	I/O39	I/O81	M3	
I/O26	I/O40	I/O82	N2	
	I/O41	I/O83		
	I/O42	I/O84		
		I/O85		
		I/O86		
		I/O87		
		I/O88		
I/O27 (A28)	I/O43 (A28)	I/O89 (A28)	P1	28
I/O28	I/O44	I/O90	P2	29
		I/O91		
		I/O92		
I/O29	I/O45	I/O93	R1	30
I/O30	I/O46	I/O94	N3	31
I/O31 ($\overline{\text{OTS}}$)	I/O47 ($\overline{\text{OTS}}$)	I/O95 ($\overline{\text{OTS}}$)	T1	32
I/O32, GCK2 (A29)	I/O48, GCK2 (A29)	I/O96, GCK2 (A29)	P3	33
AVRRESET	$\overline{\text{AVRRESET}}$	$\overline{\text{AVRRESET}}$	R2	34
M0	M0	M0	R3	36
FPSLIC Array				
M2	M2	M2	T3	38

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144(1)
I/O33, GCK3	I/O49, GCK3	I/O97, GCK3	R4	39
I/O34 (HDC/TDI)	I/O50 (HDC/TDI)	I/O98 (HDC/TDI)	T4	40
I/O35	I/O51	I/O99	N5	41
I/O36	I/O52	I/O100	P5	42
	I/O53	I/O101		43
SER_EN	SER_EN	SER_EN	M5	81
I/O38 (LDC/TDO)	I/O54 (LDC/TDO)	I/O102 (LDC/TDO)	R5	44
		I/O103		
		I/O104		
		I/O105		
		I/O106		
NC	NC	I/O107	T5	
NC	NC	I/O108	M6	
I/O39	I/O55	I/O109	P6	
I/O40	I/O56	I/O110	R6	
NC	I/O57	I/O111	L6	
NC	I/O58	I/O112	T6	
		I/O113		
		I/O114		
		I/O115		
		I/O116		
	I/O59	I/O117		
	I/O60	I/O118		
		I/O119		
		I/O120		
I/O41	I/O61	I/O121	M7	46
I/O42	I/O62	I/O122	N7	47
I/O43 (TMS)	I/O63 (TMS)	I/O123 (TMS)	P7	48
I/O44 (TCK)	I/O64 (TCK)	I/O124 (TCK)	R7	49
NC	I/O65	I/O125	K7	
NC	I/O66	I/O126	K8	
		I/O127		
		I/O128		
		I/O129		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[(1)]
		I/O130		
		I/O131		
		I/O132		
		I/O133		
		I/O134		
NC	I/O67	I/O135	M8	
NC	I/O68	I/O136	R8	
I/O45	I/O69	I/O137	P8	50
I/O46	I/O70	I/O138	N8	51
		I/O139		
		I/O140		
		I/O141		
		I/O142		
I/O47 (TD7)	I/O71 (TD7)	I/O143 (TD7)	L8	52
I/O48 (InitErr) RESET/$\overline{OE}$	I/O72 (InitErr) RESET/$\overline{OE}$	I/O144 (InitErr) RESET/$\overline{OE}$	K9	53
I/O49 (TD6)	I/O73 (TD6)	I/O145 (TD6)	P9	56
I/O50 (TD5)	I/O74 (TD5)	I/O146 (TD5)	N9	57
		I/O147		
		I/O148		
		I/O149		
		I/O150		
I/O51	I/O75	I/O151	M9	58
I/O52	I/O76	I/O152	L9	59
NC	I/O77	I/O153	J9	
NC	I/O78	I/O154	T10	
		I/O155		
		I/O156		
		I/O157		
		I/O158		
		I/O159		
		I/O160		
		I/O161		
		I/O162		
NC	I/O79	I/O163	P10	

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144(1)
NC	I/O80	I/O164	N10	
I/O53 (TD4)	I/O81 (TD4)	I/O165 (TD4)	L10	60
I/O54 (TD3)	I/O82 (TD3)	I/O166 (TD3)	T11	61
I/O55	I/O83	I/O167	R11	62
I/O56	I/O84	I/O168	M11	63
NC	NC	I/O169	N11	
NC	NC	I/O170	T12	
NC	I/O85	I/O171	R12	
NC	I/O86	I/O172	T13	
		I/O173		
		I/O174		
		I/O175		
		I/O176		
NC	I/O87	I/O177	N12	
NC	I/O88	I/O178	P12	
I/O57	I/O89	I/O179	R13	
I/O58	I/O90	I/O180	T14	
NC	NC	I/O181	N13	
NC	NC	I/O182	P13	
I/O59 (TD2)	I/O91 (TD2)	I/O183 (TD2)	T16	65
I/O60 (TD1)	I/O92 (TD1)	I/O184 (TD1)	P14	66
		I/O185		
		I/O186		
		I/O187		
		I/O188		
I/O61	I/O93	I/O189	R16	67
I/O62	I/O94	I/O190	P15	68
I/O63 (TD0)	I/O95 (TD0)	I/O191 (TD0)	N14	69
I/O64, GCK4	I/O96, GCK4	I/O192, GCK4	P16	70
$\overline{\text{CON}}$/CE	$\overline{\text{CON}}$/CE	$\overline{\text{CON}}$/CE	N16	72
FPSLIC Array				
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	M14	74
PE0	PE0	PE0	M12	75
PE1	PE1	PE1	M15	76

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[1]
		I/O321		
		I/O322		
		I/O323		
		I/O324		
I/O107 (A4)	I/O161 (A4)	I/O325 (A4)	A10	121
I/O108 (A5)	I/O162 (A5)	I/O326 (A5)	G10	122
NC	I/O163	I/O327	G9	
NC	I/O164	I/O328	F9	
I/O109	I/O165	I/O329	E9	123
I/O110	I/O166	I/O330	C9	124
		I/O331		
		I/O332		
		I/O333		
		I/O334		
I/O111 (A6)	I/O167 (A6)	I/O335 (A6)	B9	125
I/O112 (A7)	I/O168 (A7)	I/O336 (A7)	A9	126
I/O113 (A8)	I/O169 (A8)	I/O337 (A8)	A8	129
I/O114 (A9)	I/O170 (A9)	I/O338 (A9)	B8	130
		I/O339		
		I/O340		
		I/O341		
		I/O342		
I/O115	I/O171	I/O343	C8	131
I/O116	I/O172	I/O344	D8	132
NC	I/O173	I/O345	E8	
NC	I/O174	I/O346	F8	
I/O117 (A10)	I/O175 (A10)	I/O347 (A10)	H8	133
I/O118 (A11)	I/O176 (A11)	I/O348 (A11)	A7	134
NC	NC	I/O349	C7	
NC	NC	I/O350	D7	
		I/O351		
		I/O352		
		I/O353		
		I/O354		

Table 5-3. AT94S Pin List (Continued)

AT94S05 96 FPGA I/O	AT94S10 144 FPGA I/O	AT94S40 288 FPGA I/O	Package	
			Chip Array 256 CABGA	LQ144[(1)]
		I/O355		
		I/O356		
NC	I/O177	I/O357	F7	
NC	I/O178	I/O358	A6	
I/O119	I/O179	I/O359	F6	135
I/O120	I/O180	I/O360	B6	136
		I/O361		
		I/O362		
NC	I/O181	I/O363	D6	
NC	I/O182	I/O364	E6	
		I/O365		
		I/O366		
		I/O367		
		I/O368		
I/O121	I/O183	I/O369	A5	
I/O122	I/O184	I/O370	B5	
I/O123 (A12)	I/O185 (A12)	I/O371 (A12)	E5	138
I/O124 (A13)	I/O186 (A13)	I/O372 (A13)	C5	139
		I/O373		
		I/O374		
		I/O375		
		I/O376		
		I/O377		
		I/O378		
NC	I/O187	I/O379	A4	
NC	I/O188	I/O380	B4	
I/O125	I/O189	I/O381	A3	140
I/O126	I/O190	I/O382	C4	141
I/O127 (A14)	I/O191 (A14)	I/O383 (A14)	B3	142
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O384, GCK8 (A15)	A2	143

Note: 1. LQ144 is only offered in the AT94S10 and AT94S40.

Table 5-4. 256 CABGA and LQ144 V_{DD}, V_{CC} and GND Pins(1)

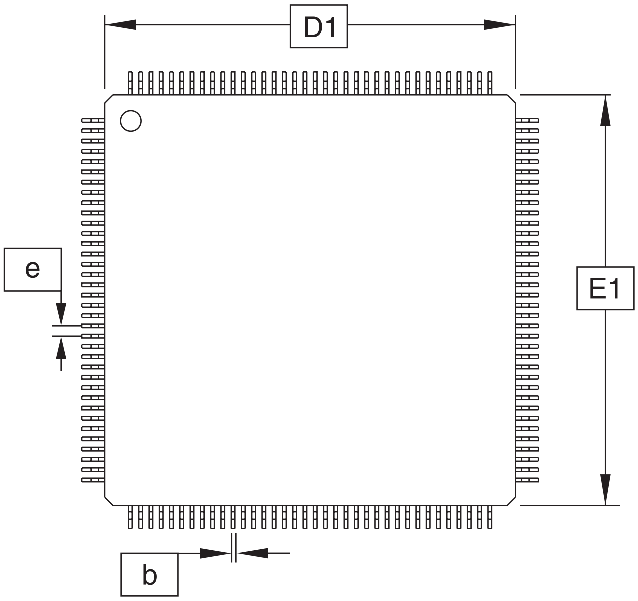
Package	V_{DD} (core)	V_{CC} (I/O)	GND
256 CABGA	D14, E7, F12, G3, H9, K10, L13, M13, P4, T9	B2, G8, G13, H10, K13, L3, M10, R14, T3, T7	B11, B13, B16, B7, C3, C6, D5, D9, F11, F13, T15, F16, F2, F5, G16, H11, H16, J15, J2, K16, K3, T2, L14, L16, L7, M4, N15, N4, N6, P11, R9, R10, R15, T8
LQ144	18, 54, 90, 128	37, 73, 108, 144	1, 8, 17, 27, 35, 45, 55, 64, 71, 91, 100, 110, 118, 127, 137

Note: 1. For power rail support for product migration to lower-power devices, refer to the "Designing in Split Power Supply Support for AT94KAL/AX and AT94SAL/AX Devices" application note (doc2308.pdf), available on the Atmel web site, at http://www.atmel.com/dyn/products/app_notes.asp?family_id=627.

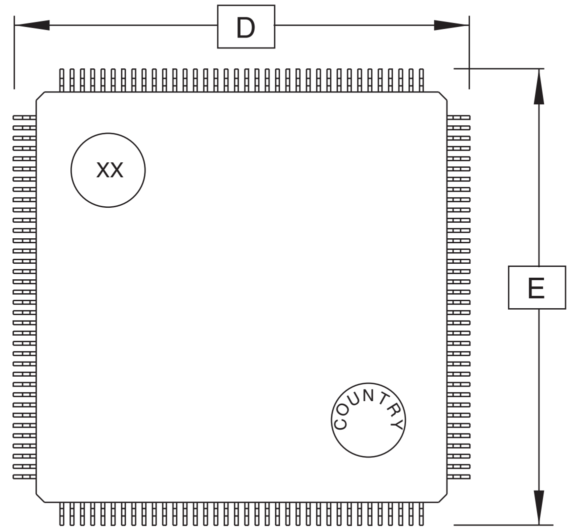
6. Thermal Coefficient Table

Package Style	Lead Count	Theta J-A [°C/W] 0 LFPM	Theta J-A [°C/W] 225 LFPM	Theta J-A [°C/W] 500 LPFM
CABGA	256	27	23	20
LQFP	144	35	—	—

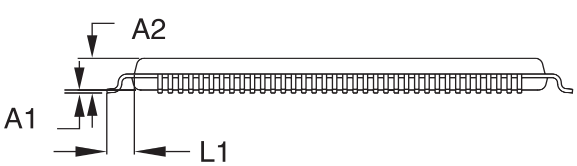
8.2 144L1 – LQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D	22.00 BSC			
D1	20.00 BSC			2, 3
E	22.00 BSC			
E1	20.00 BSC			2, 3
e	0.50 BSC			
b	0.17	0.22	0.27	4, 5
L1	1.00 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

11/30/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**144L1**, 144-lead (20 x 20 x 1.4 mm Body), Low Profile Plastic Quad Flat Pack (LQFP)	144L1	A

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