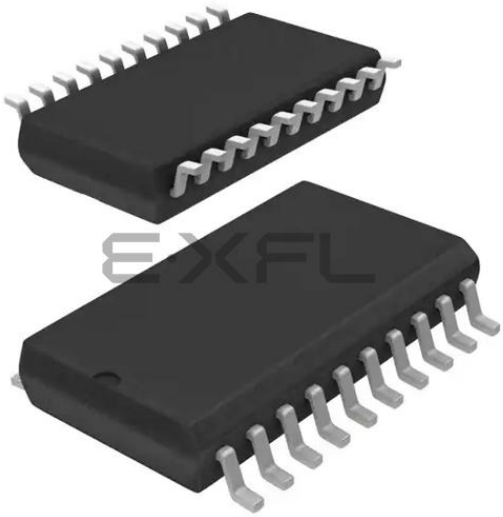


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24223-24si

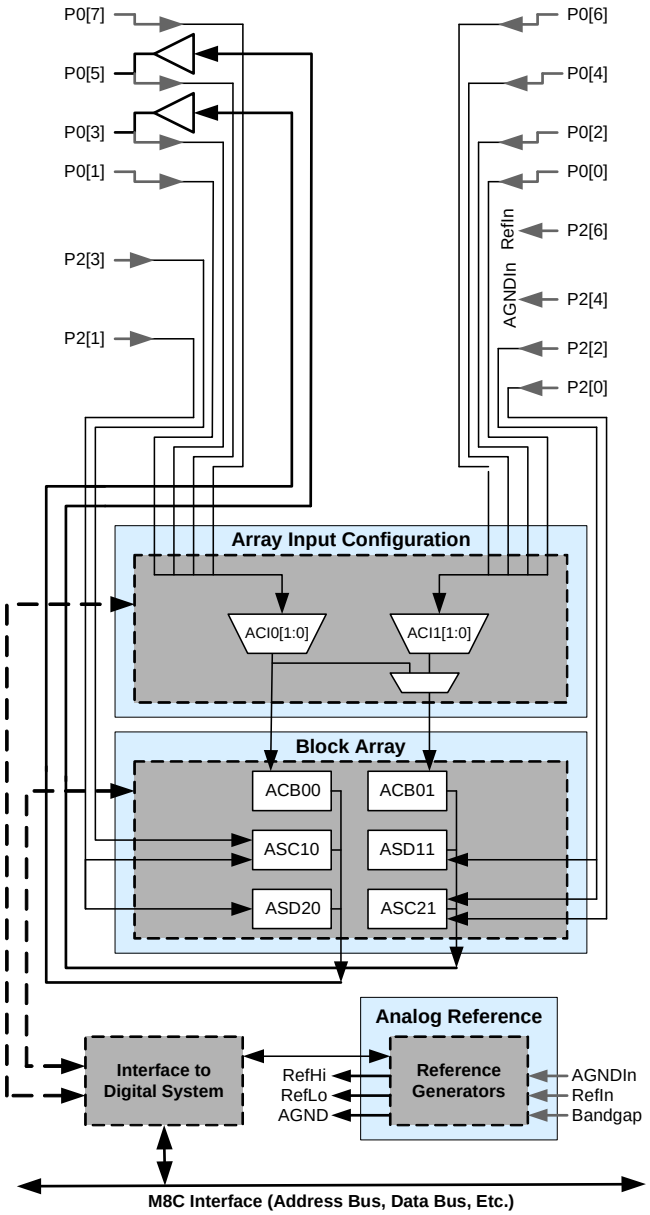
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table PSoC Device Characteristics on page 4.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x66	up to 44	2	8	12	4	4	12
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C24x23	**up to 24**	**1**	**4**	**12**	**2**	**2**	**6**
CY8C22x13	up to 16	1	4	8	1	1	3

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer the PSoC Programmable Sytem-on-Chip Technical Reference Manual.

For up-to-date Ordering, Packaging, and Electrical Specification information, refer the latest PSoC device data sheets on the web at http://www.cypress.com/psoc.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training

Free PSoC technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, and application-specific classes covering topics, such as PSoC and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select Technical Training for more details.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes can assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date as default.

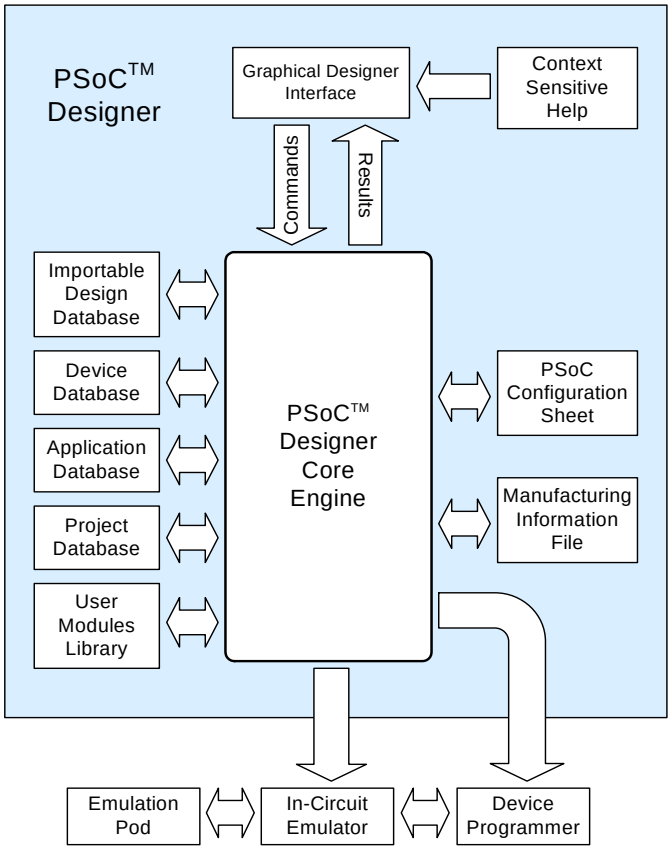
Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (refer Figure 3).

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 3. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. After the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

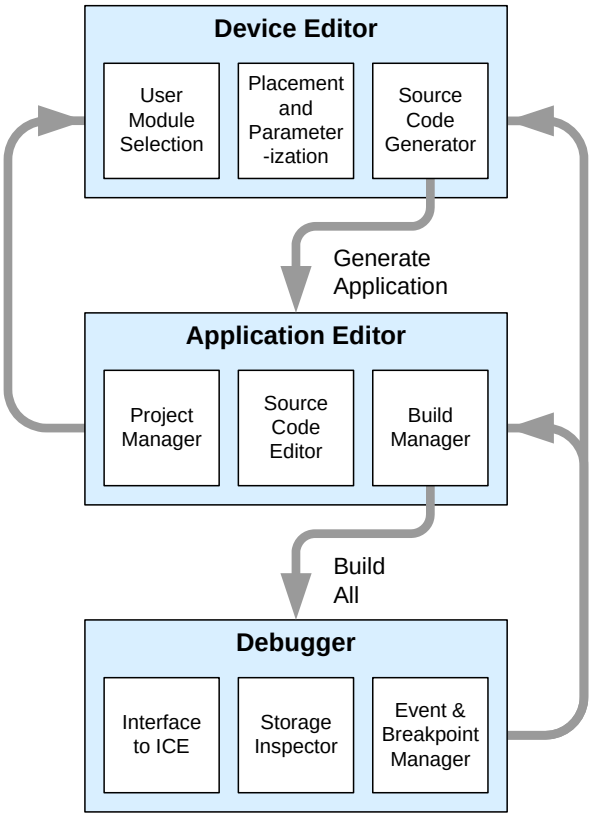
In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Figure 5. User Module and Source Code Development Flows



The next step is to write your main program, and any sub-routines using PSoC Designer's Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive "grep-style" patterns. A single mouse click invokes the Build Manager. It employs a professional-strength "makefile" system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a ROM file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the ROM image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
RAM	random access memory
ROM	read only memory
SC	switched capacitor
SMP	switch mode pump

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 11 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

32-Pin Part Pinout

Table 6. 32-Pin Part Pinout (MLF*)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[7]	
2	IO		P2[5]	
3	IO	I	P2[3]	Direct switched capacitor block input
4	IO	I	P2[1]	Direct switched capacitor block input
5	Power		Vss	Ground connection
6	Power		SMP	Switch Mode Pump (SMP) connection to external components required
7	IO		P1[7]	I2C Serial Clock (SCL)
8	IO		P1[5]	I2C Serial Data (SDA)
9			NC	No connection. Do not use.
10	IO		P1[3]	
11	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
12	Power		Vss	Ground connection
13	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
14	IO		P1[2]	
15	IO		P1[4]	Optional External Clock Input (EXTCLK)
16			NC	No connection. Do not use.
17	IO		P1[6]	
18	Input		XRES	Active high external reset with internal pull down
19	IO	I	P2[0]	Direct switched capacitor block input
20	IO	I	P2[2]	Direct switched capacitor block input
21	IO		P2[4]	External Analog Ground (AGND)
22	IO		P2[6]	External Voltage Reference (VRef)
23	IO	I	P0[0]	Analog column mux input
24	IO	I	P0[2]	Analog column mux input
25			NC	No connection. Do not use.
26	IO	I	P0[4]	Analog column mux input
27	IO	I	P0[6]	Analog column mux input
28	Power		Vdd	Supply voltage
29	IO	I	P0[7]	Analog column mux input
30	IO	IO	P0[5]	Analog column mux input and column output
31	IO	IO	P0[3]	Analog column mux input and column output
32	IO	I	P0[1]	Analog column mux input

LEGEND: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to the same ground as the Vss pin.

Figure 9. CY8C24423 32-Pin PSoC Device

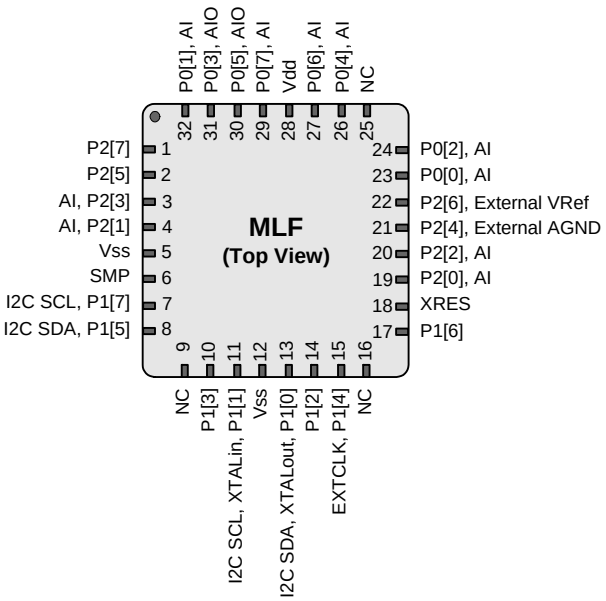


Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

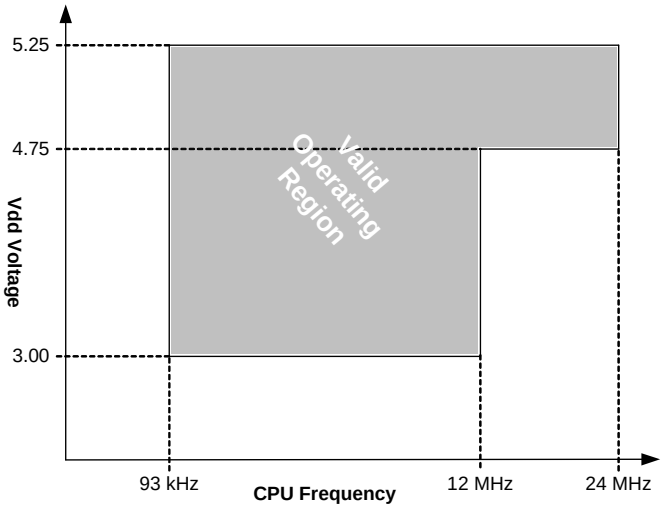
Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23 PSoC device. For latest electrical specifications, http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 10. Voltage versus Operating Frequency



The following table lists the units of measure that are used in this section.

Table 10. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
µA	micro ampere	pp	peak-to-peak
µF	micro farad	ppm	parts per million
µH	micro henry	ps	picosecond
µs	microsecond	sps	samples per second
µV	micro volts	s	sigma: one standard deviation
µVrms	micro volts root-mean-square	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+100	°C	Higher storage temperatures reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
–	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
–	Static Discharge Voltage	2000	–	–	V	
–	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 41. The user must limit the power consumption to comply with this requirement.

Table 16. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power Input Offset Voltage (absolute value) Mid Power High Power is 5 Volt Only	– –	1.65 1.32	10 8	mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	–	–	dB	

DC Switch Mode Pump Specifications

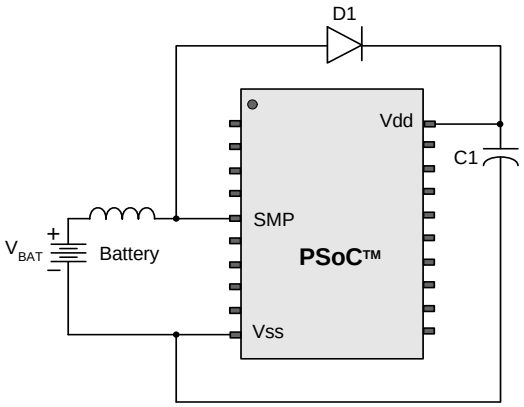
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 19. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output voltage	4.75	5.0	5.25	V	Average, neglecting ripple
V_{PUMP} 3V	3V Output voltage	3.00	3.25	3.60	V	Average, neglecting ripple
I_{PUMP}	Available Output Current V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.8V, V_{PUMP} = 5.0V	 8 5	 – –	 – –	 mA mA	For implementation, which includes 2 uH inductor, 1 uF cap, and Schottky diode
V_{BAT}5V	Input Voltage Range from Battery	1.8	–	5.0	V	
V_{BAT}3V	Input Voltage Range from Battery	1.0	–	3.3	V	
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.1	–	–	V	
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	$\%V_O$[a]	
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$[a]	
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on cap/load)	–	25	–	mVpp	Configuration of note 2, load is 5mA
–	Efficiency	35	50	–	%	Configuration of note 2, load is 5mA, Vout is 3.25V.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

a. V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 23 on page 25.

Figure 11. Basic Switch Mode Pump Circuit



DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 22. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

Table 23. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
	Vdd Value for PPOR Trip (positive ramp)				
V_{PPOR0R}	PORLEV[1:0] = 00b		2.908		V
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.394	–	V
V_{PPOR2R}	PORLEV[1:0] = 10b		4.548		V
	Vdd Value for PPOR Trip (negative ramp)				
V_{PPOR0}	PORLEV[1:0] = 00b		2.816		V
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.394	–	V
V_{PPOR2}	PORLEV[1:0] = 10b		4.548		V
	PPOR Hysteresis				
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b	2.863	2.921	2.979[a]	V
V_{LVD1}	VM[2:0] = 001b	2.963	3.023	3.083	V
V_{LVD2}	VM[2:0] = 010b	3.070	3.133	3.196	V
V_{LVD3}	VM[2:0] = 011b	3.920	4.00	4.080	V
V_{LVD4}	VM[2:0] = 100b	4.393	4.483	4.573	V
V_{LVD5}	VM[2:0] = 101b	4.550	4.643	4.736[b]	V
V_{LVD6}	VM[2:0] = 110b	4.632	4.727	4.822	V
V_{LVD7}	VM[2:0] = 111b	4.718	4.814	4.910	V
					V
	Vdd Value for PUMP Trip				
V_{PUMP0}	VM[2:0] = 000b	2.963	3.023	3.083	V
V_{PUMP1}	VM[2:0] = 001b	3.033	3.095	3.157	V
V_{PUMP2}	VM[2:0] = 010b	3.185	3.250	3.315	V
V_{PUMP3}	VM[2:0] = 011b	4.110	4.194	4.278	V
V_{PUMP4}	VM[2:0] = 100b	4.550	4.643	4.736	V
V_{PUMP5}	VM[2:0] = 101b	4.632	4.727	4.822	V
V_{PUMP6}	VM[2:0] = 110b	4.719	4.815	4.911	V
V_{PUMP7}	VM[2:0] = 111b	4.900	5.000	5.100	V
					V

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 24. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 27. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.62	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.92	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.15	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.7	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	6.5	–		V/µs	
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.01	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	0.5	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	4.0	–		V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.75	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	3.1	–		MHz	
	Power = High				MHz	
	Power = High, Opamp Bias = High	5.4	–		MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

Table 28. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 3.92 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 5.41 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.31 2.7 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.24 1.8 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
BW_{OA}	Gain Bandwidth Product Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.67 2.8 – –	 – – – –	 – –	 MHz MHz MHz MHz MHz MHz	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 32. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0	–	24.24	MHz
–	High Period	20.6	–	–	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Table 33. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[a]	0	–	12.12	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[b]	0	–	24.24	MHz
–	High Period with CPU Clock divide by 1	41.7	–	–	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 34. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns
F_{SCLK}	Frequency of SCLK	0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms
T_{WRITE}	Flash Block Write Time	–	30	–	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns

Packaging Information

This section presents the packaging specifications for the CY8C24x23 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Figure 19. 8-Pin (300-Mil) PDIP

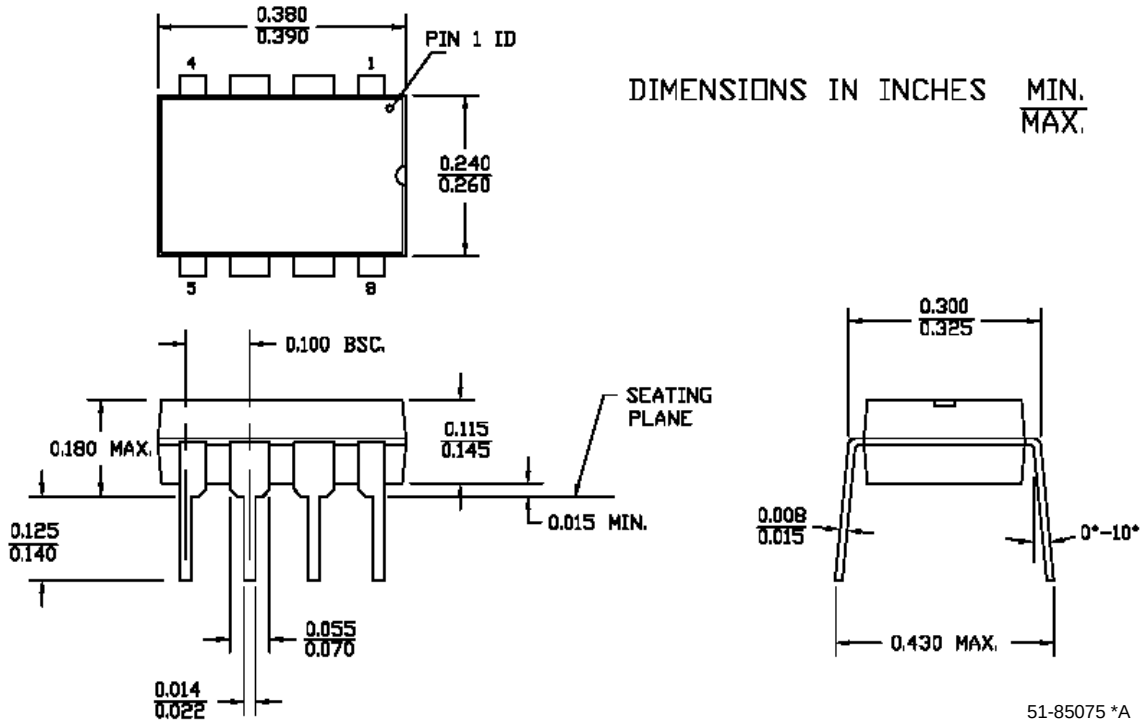


Figure 22. 20-Pin (210-Mil) SSOP

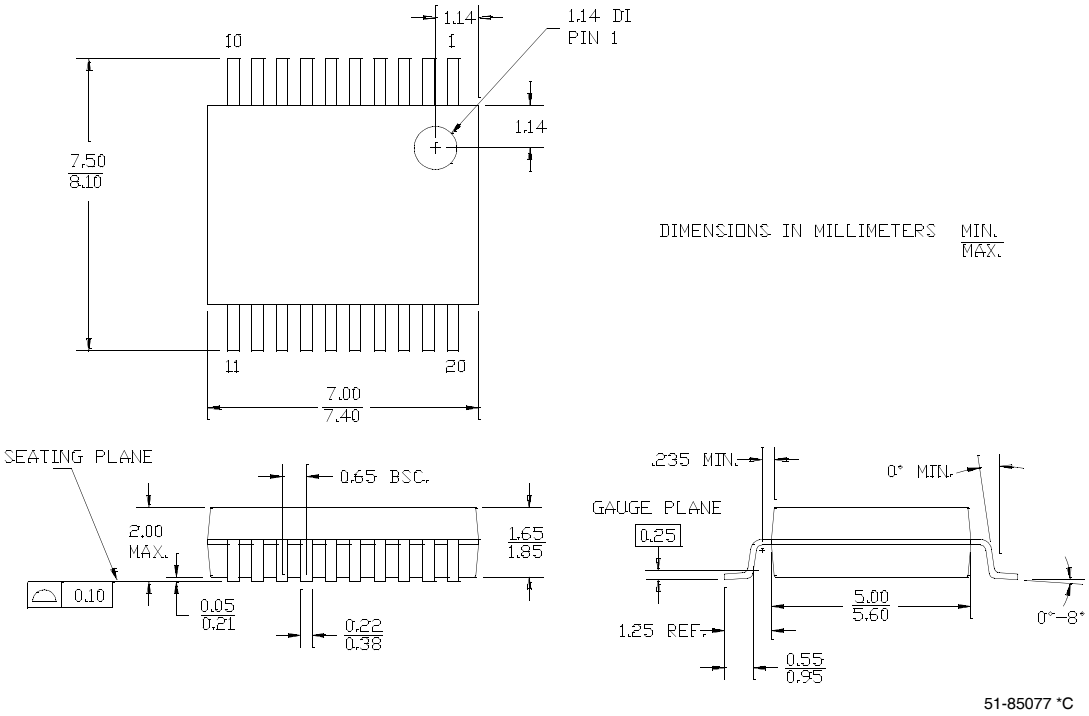


Figure 23. 20-Pin (300-Mil) Molded SOIC

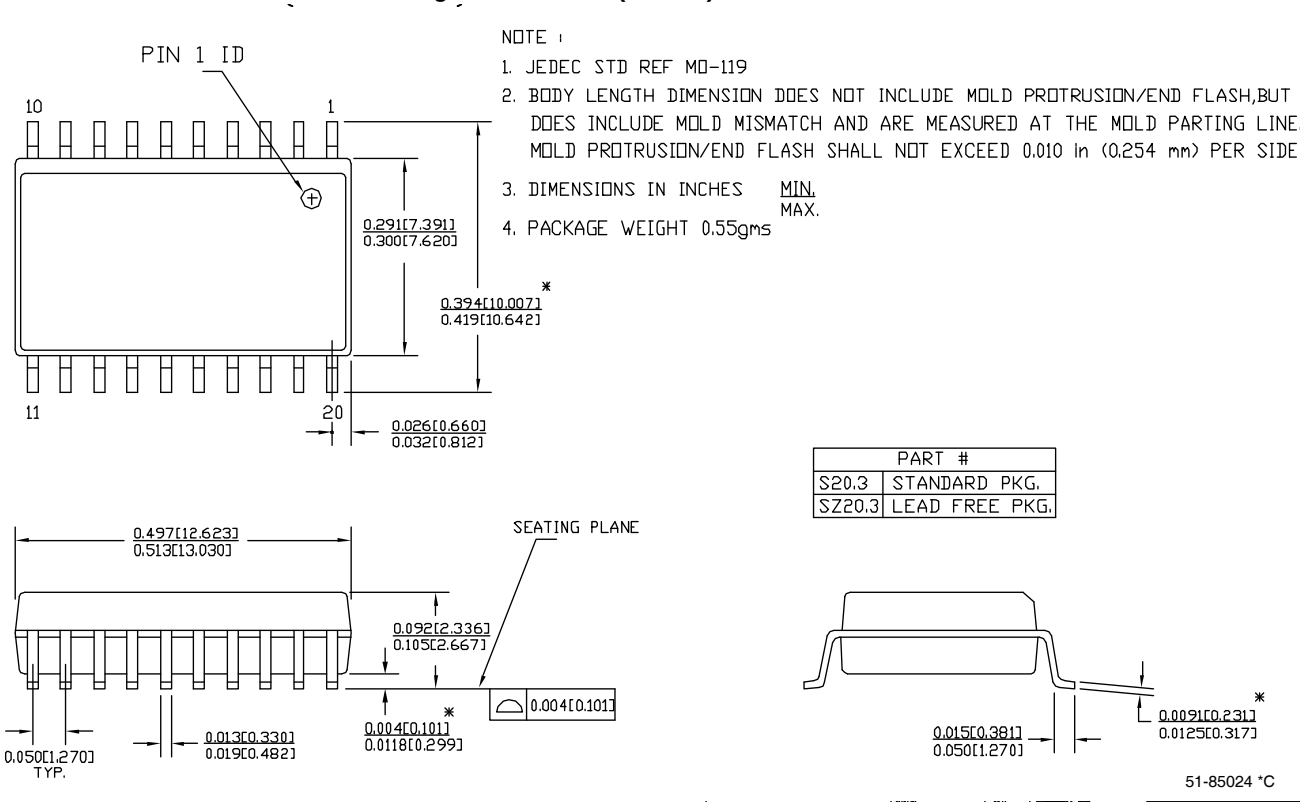


Figure 24. 28-Pin (300-Mil) Molded DIP

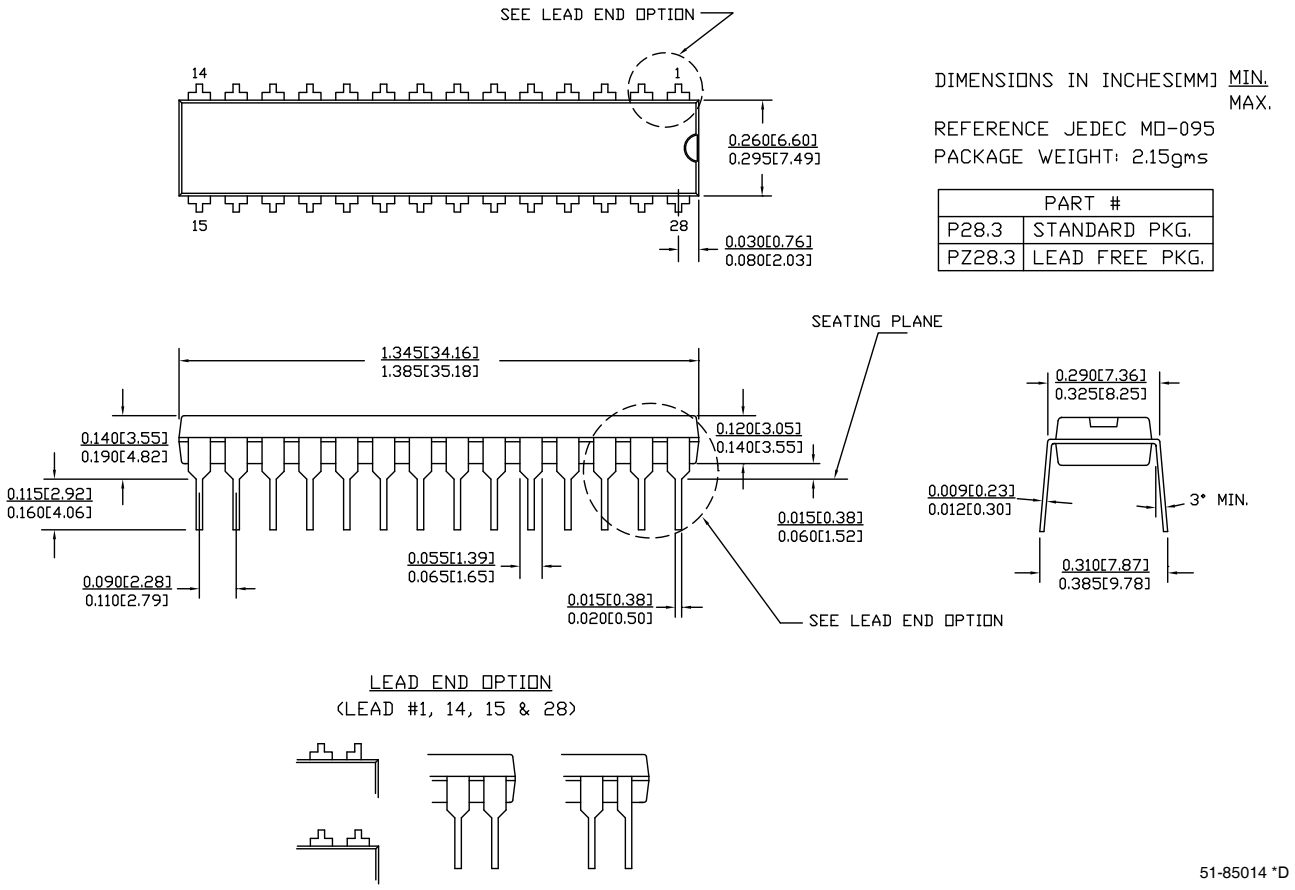


Figure 25. 28-Pin (210-Mil) SSOP

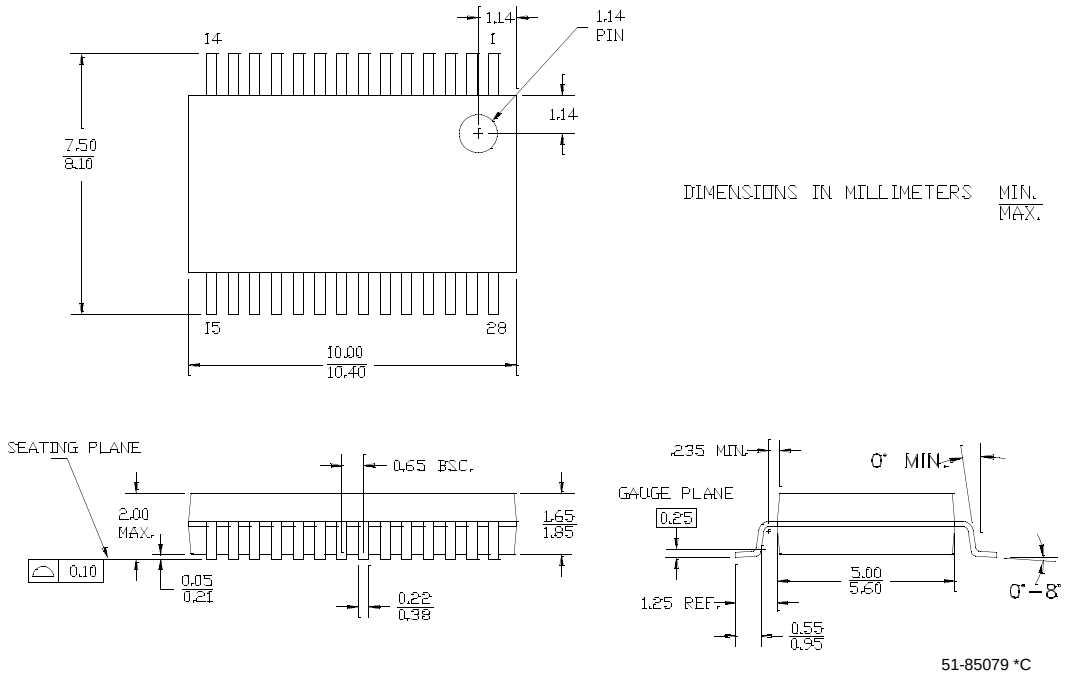


Figure 26. 28-Pin (300-Mil) Molded SOIC