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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24223-24sit

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear break-points, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Figure 4. PSoC Development Tool Kit

User Modules and the PSoC Development Process

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a pictorial environment (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by inter-connecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

32-Pin Part Pinout

Table 6. 32-Pin Part Pinout (MLF*)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[7]	
2	IO		P2[5]	
3	IO	I	P2[3]	Direct switched capacitor block input
4	IO	I	P2[1]	Direct switched capacitor block input
5	Power		Vss	Ground connection
6	Power		SMP	Switch Mode Pump (SMP) connection to external components required
7	IO		P1[7]	I2C Serial Clock (SCL)
8	IO		P1[5]	I2C Serial Data (SDA)
9			NC	No connection. Do not use.
10	IO		P1[3]	
11	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
12	Power		Vss	Ground connection
13	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
14	IO		P1[2]	
15	IO		P1[4]	Optional External Clock Input (EXTCLK)
16			NC	No connection. Do not use.
17	IO		P1[6]	
18	Input		XRES	Active high external reset with internal pull down
19	IO	I	P2[0]	Direct switched capacitor block input
20	IO	I	P2[2]	Direct switched capacitor block input
21	IO		P2[4]	External Analog Ground (AGND)
22	IO		P2[6]	External Voltage Reference (VRef)
23	IO	I	P0[0]	Analog column mux input
24	IO	I	P0[2]	Analog column mux input
25			NC	No connection. Do not use.
26	IO	I	P0[4]	Analog column mux input
27	IO	I	P0[6]	Analog column mux input
28	Power		Vdd	Supply voltage
29	IO	I	P0[7]	Analog column mux input
30	IO	IO	P0[5]	Analog column mux input and column output
31	IO	IO	P0[3]	Analog column mux input and column output
32	IO	I	P0[1]	Analog column mux input

LEGEND: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to the same ground as the Vss pin.

Figure 9. CY8C24423 32-Pin PSoC Device

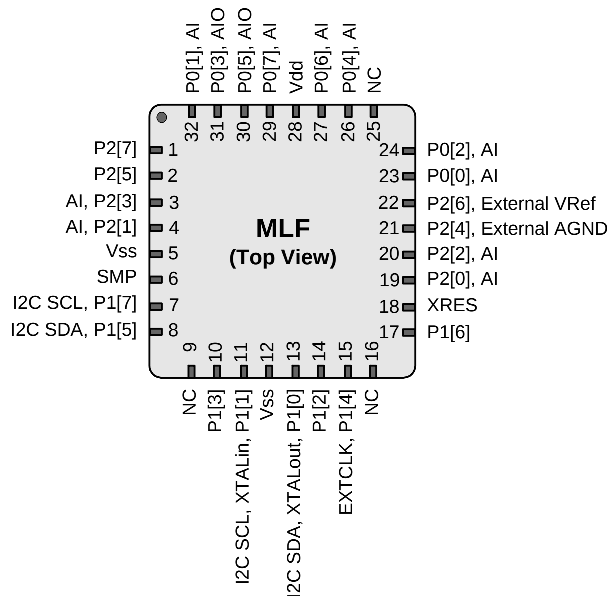


Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 8. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	

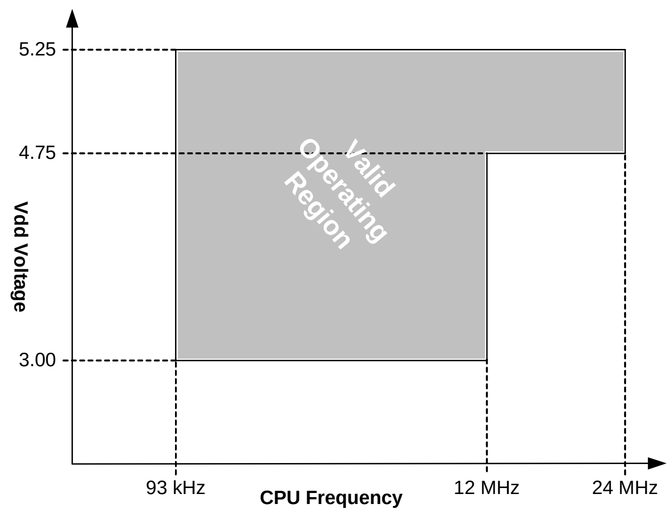
Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23 PSoC device. For latest electrical specifications, http://www.cypress.com.

Specifications are valid for $-40^oC \le T_A \le 85^oC$ and $T_J \le 100^oC$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^oC \le T_A \le 70^oC$ and $T_J \le 82^oC$.

Figure 10. Voltage versus Operating Frequency



The following table lists the units of measure that are used in this section.

Table 10. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
µA	micro ampere	pp	peak-to-peak
µF	micro farad	ppm	parts per million
µH	micro henry	ps	picosecond
µs	microsecond	sps	samples per second
µV	micro volts	s	sigma: one standard deviation
µVrms	micro volts root-mean-square	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+100	^oC	Higher storage temperatures reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+85	^oC	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
–	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
–	Static Discharge Voltage	2000	–	–	V	
–	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	^oC	
T_J	Junction Temperature	-40	–	+100	^oC	The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 41. The user must limit the power consumption to comply with this requirement.

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 14. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (80 mA maximum combined IOH budget)
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (150 mA maximum combined IOL budget)
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25^{o}C
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25^{o}C

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 15. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.6	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.3	8	mV	
	Input Offset Voltage (absolute value) High Power	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/^{o}C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25^{o}C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 17. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	–	–	dB

Table 18. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	50	–	–	dB

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 22. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

Table 23. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
 V_{PPOR0R} V_{PPOR1R} V_{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.908 4.394 4.548	–	 V V V
 V_{PPOR0} V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.816 4.394 4.548	–	 V V V
 V_{PH0} V_{PH1} V_{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – – –	 92 0 0	 – – –	 mV mV mV
 V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.863 2.963 3.070 3.920 4.393 4.550 4.632 4.718	 2.921 3.023 3.133 4.00 4.483 4.643 4.727 4.814	 2.979[a] 3.083 3.196 4.080 4.573 4.736[b] 4.822 4.910	 V V V V V V V V V
 V_{PUMP0} V_{PUMP1} V_{PUMP2} V_{PUMP3} V_{PUMP4} V_{PUMP5} V_{PUMP6} V_{PUMP7}	Vdd Value for PUMP Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.963 3.033 3.185 4.110 4.550 4.632 4.719 4.900	 3.023 3.095 3.250 4.194 4.643 4.727 4.815 5.000	 3.083 3.157 3.315 4.278 4.736 4.822 4.911 5.100	 V V V V V V V V V

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 24. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 25. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a]	MHz	Trimmed. Using factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b,e,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800[f]	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 ^oC ≤ T_A ≤ 85 ^oC.

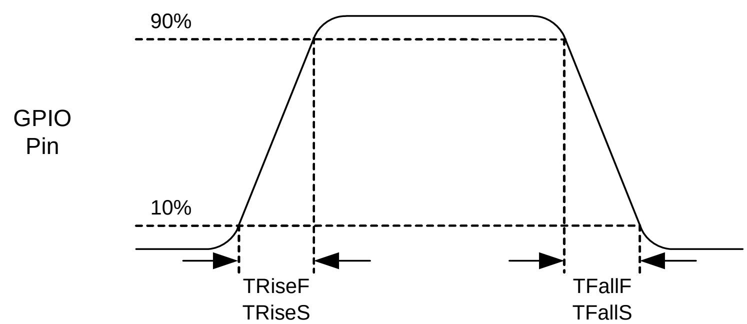
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 26. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 17. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 27. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 – – –	 3.9 0.72 0.62	 μs μs μs μs μs μs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 – – –	 5.9 0.92 0.72	 μs μs μs μs μs μs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –		 V/μs V/μs V/μs V/μs V/μs V/μs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –		 V/μs V/μs V/μs V/μs V/μs V/μs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
BW_{OA}	Gain Bandwidth Product Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –		 MHz MHz MHz MHz MHz MHz	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

Table 28. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.92	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.41	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.31	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	2.7	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.24	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.8	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.67	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	2.8	–		MHz	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	MHz	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 32. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0	–	24.24	MHz
–	High Period	20.6	–	–	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

Table 33. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[a]	0	–	12.12	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[b]	0	–	24.24	MHz
–	High Period with CPU Clock divide by 1	41.7	–	–	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 34. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns
F_{SCLK}	Frequency of SCLK	0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms
T_{WRITE}	Flash Block Write Time	–	30	–	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns

AC I²C Specifications

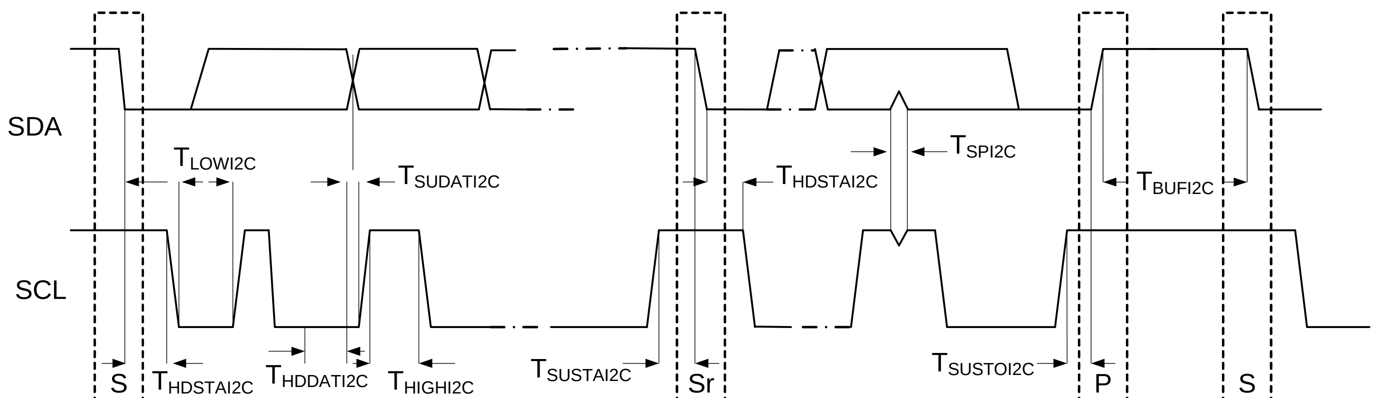
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 35. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[a]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

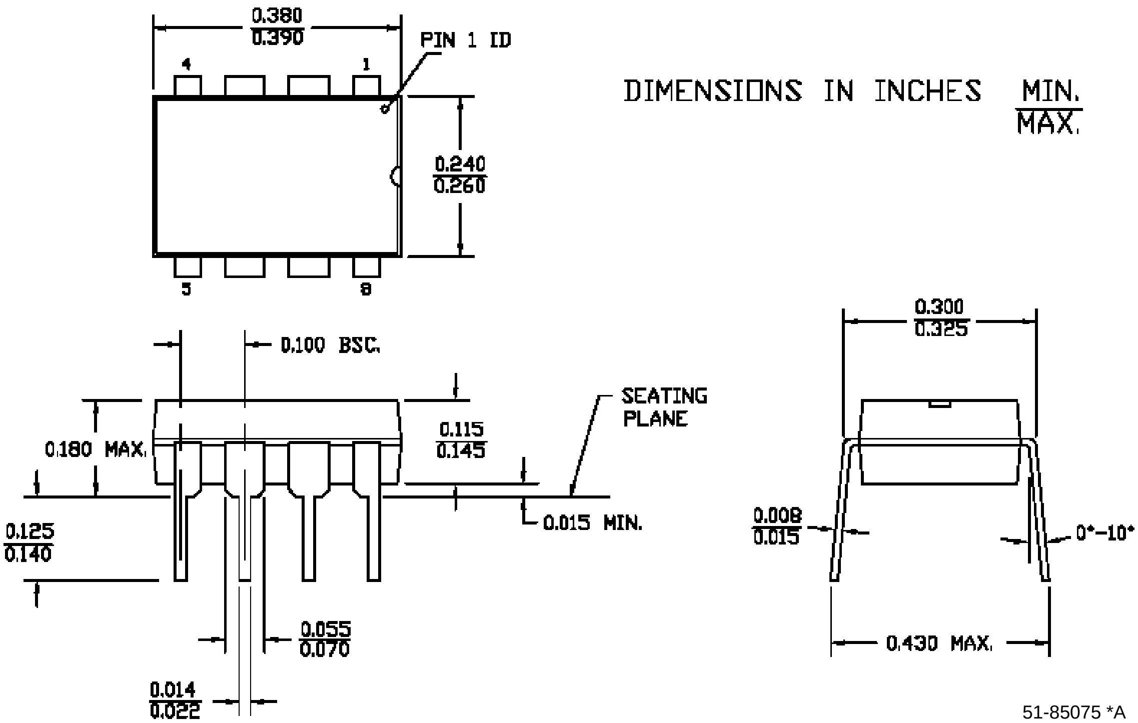
Figure 18. Definition for Timing for Fast/Standard Mode on the I2C Bus



Packaging Information

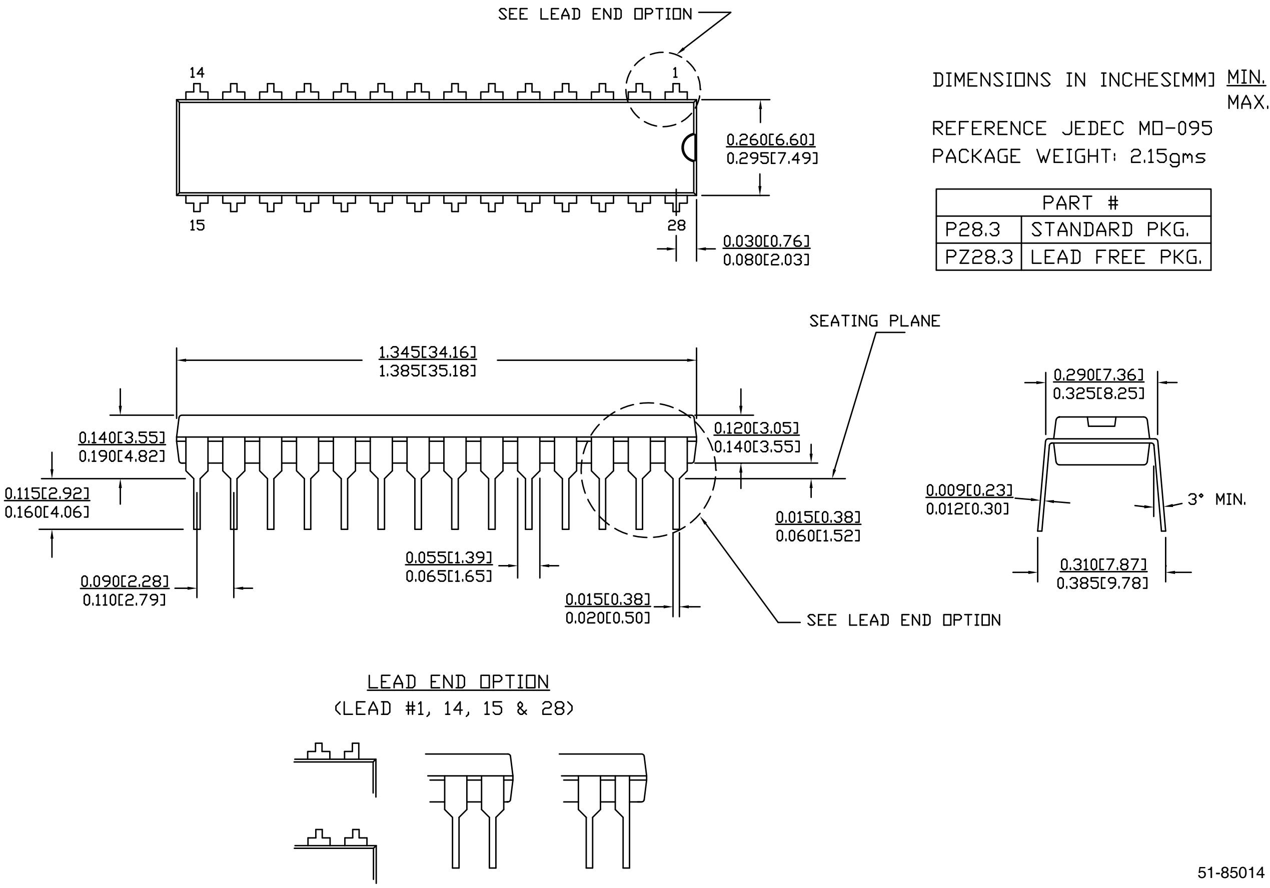
This section presents the packaging specifications for the CY8C24x23 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Figure 19. 8-Pin (300-Mil) PDIP



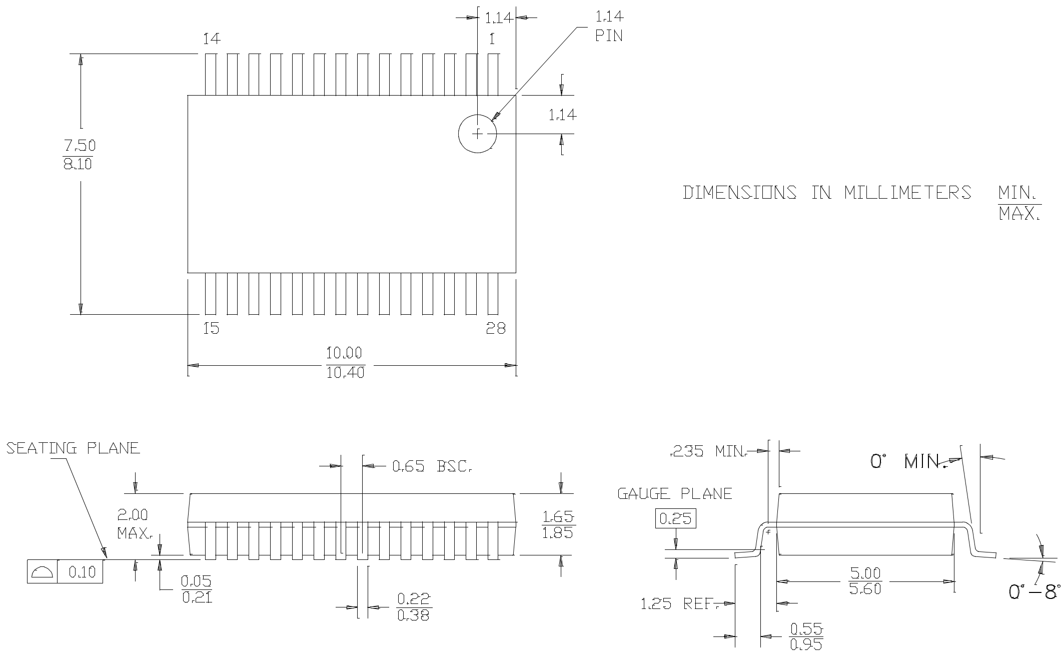
51-85075 *A

Figure 24. 28-Pin (300-Mil) Molded DIP



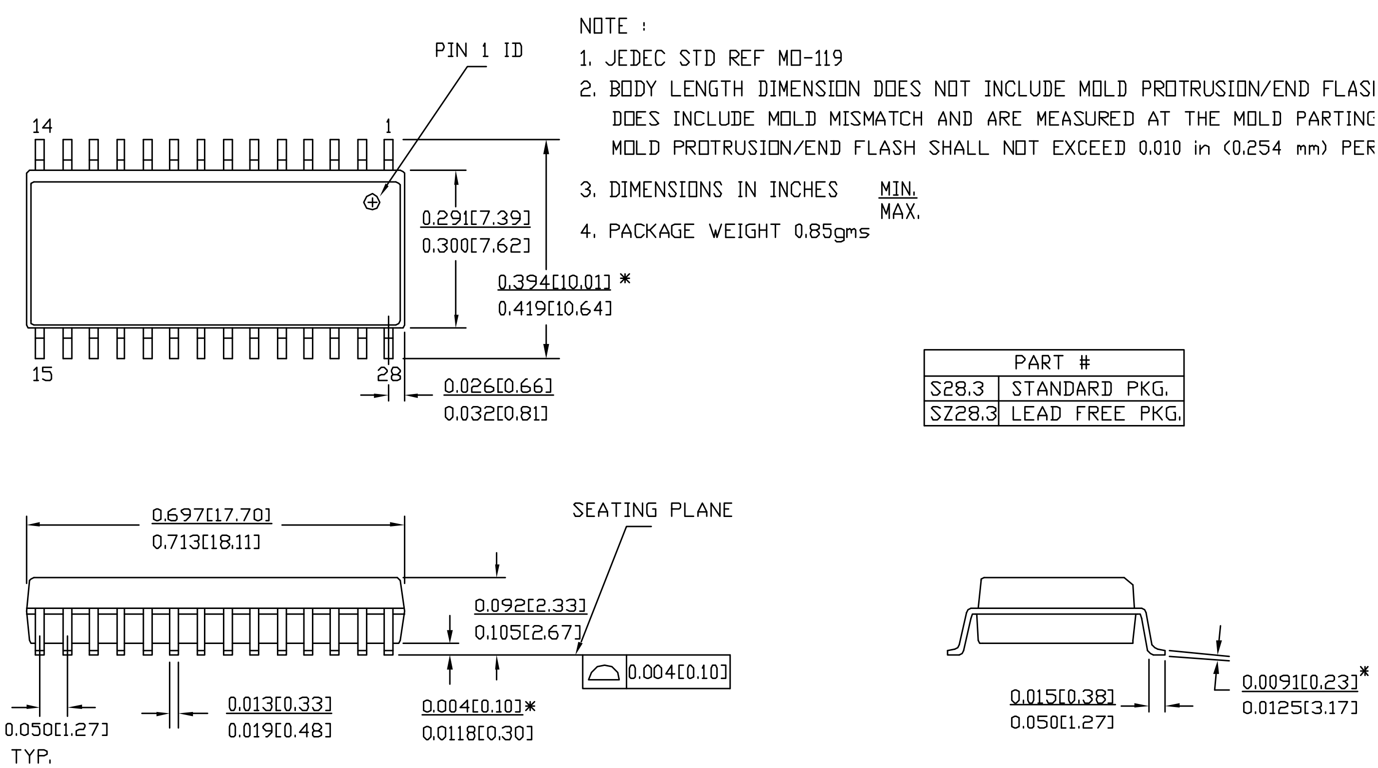
51-85014 *D

Figure 25. 28-Pin (210-Mil) SSOP



51-85079 *C

Figure 26. 28-Pin (300-Mil) Molded SOIC



51-85026 *D

Ordering Information

The following table lists the CY8C24x23 PSoC Device family's key package features and ordering codes.

Table 38. CY8C24x23 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C24123-24PI	4	256	No	-40°C to +85°C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC	CY8C24123-24SI	4	256	Yes	-40°C to +85°C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C24123-24SIT	4	256	Yes	-40°C to +85°C	4	6	6	4	2	No
20 Pin (300 Mil) DIP	CY8C24223-24PI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP	CY8C24223-24PVI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223-24PVIT	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC	CY8C24223-24SI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24223-24SIT	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
28 Pin (300 Mil) DIP	CY8C24423-24PI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423-24PVI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423-24PVIT	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC	CY8C24423-24SI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24423-24SIT	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
32 Pin (5x5 mm) MLF	CY8C24423-24LFI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 24 xxx-SPxx

Package Type:
- P = PDIP
- S = SOIC
- PV = SSOP
- LF = MLF
- A = TQFP

Thermal Rating:
- C = Commercial
- I = Industrial
- E = Extended

Speed: 24 MHz

Part Number

Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress MicroSystems

Company ID: CY = Cypress