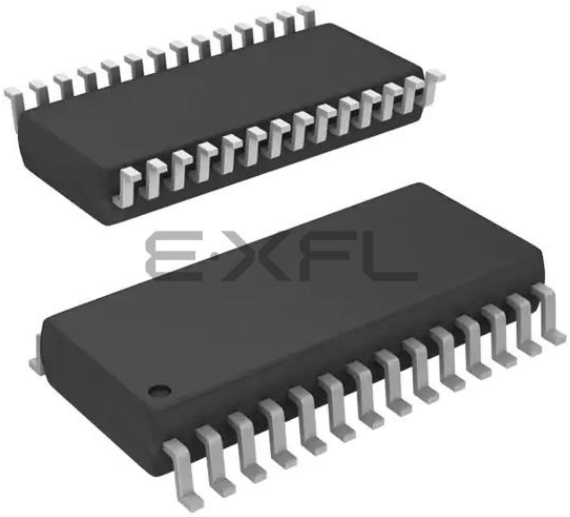

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423-24si

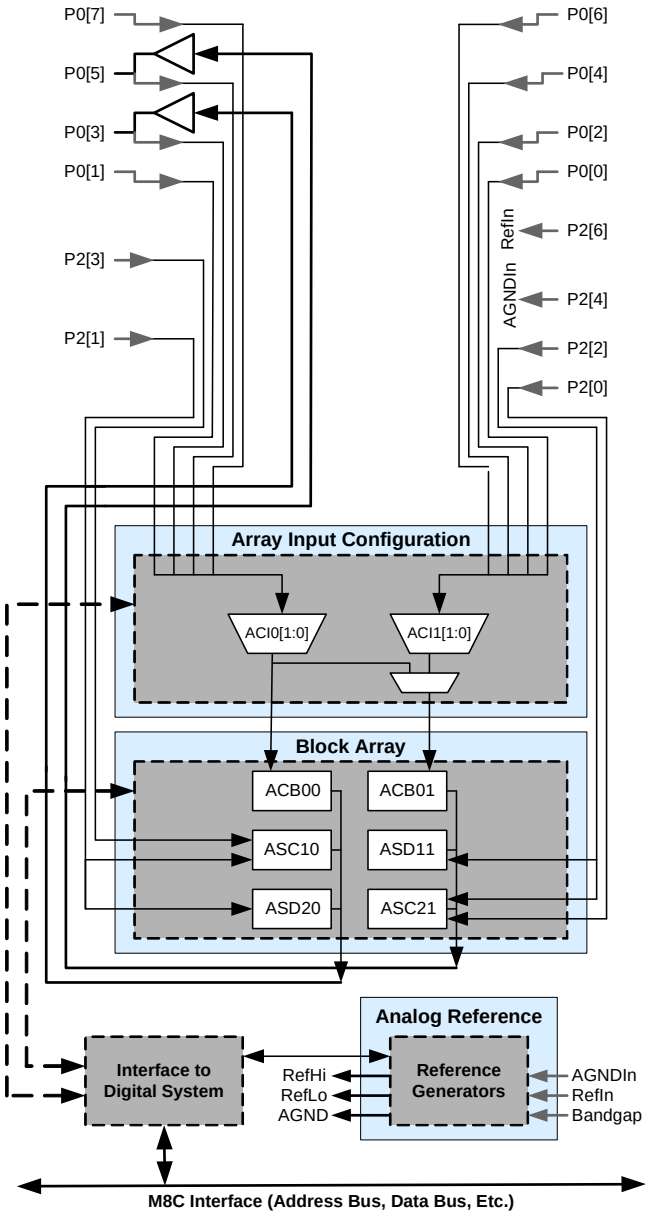
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table PSoC Device Characteristics on page 4.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x66	up to 44	2	8	12	4	4	12
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C24x23	**up to 24**	**1**	**4**	**12**	**2**	**2**	**6**
CY8C22x13	up to 16	1	4	8	1	1	3

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer the PSoC Programmable Sytem-on-Chip Technical Reference Manual.

For up-to-date Ordering, Packaging, and Electrical Specification information, refer the latest PSoC device data sheets on the web at http://www.cypress.com/psoc.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training

Free PSoC technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, and application-specific classes covering topics, such as PSoC and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select Technical Training for more details.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes can assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date as default.

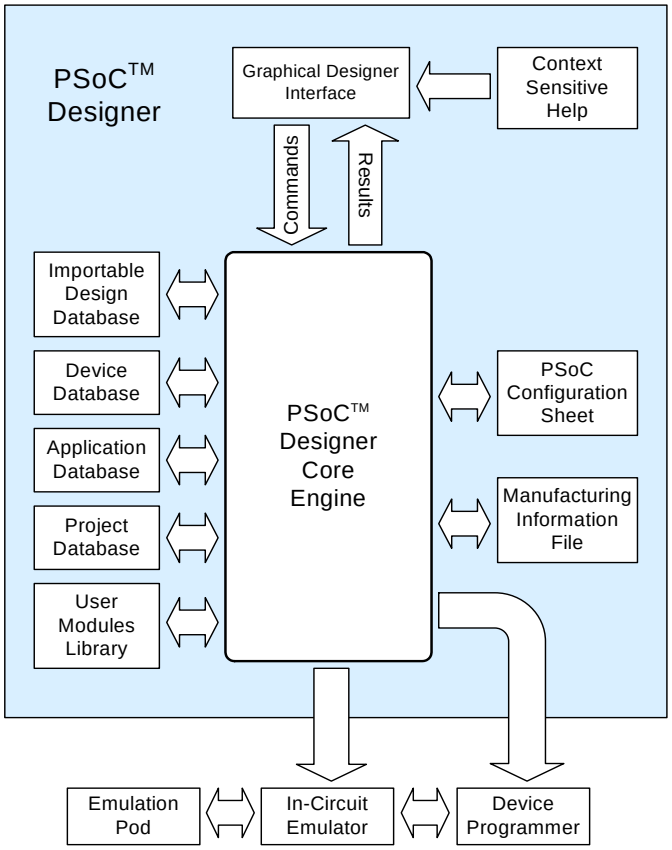
Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (refer Figure 3).

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 3. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. After the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 14. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (80 mA maximum combined IOH budget)
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (150 mA maximum combined IOL budget)
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 15. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.6	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.3	8	mV	
	Input Offset Voltage (absolute value) High Power	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.

Table 16. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power Input Offset Voltage (absolute value) Mid Power High Power is 5 Volt Only	– –	1.65 1.32	10 8	mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	–	–	dB	

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 17. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	–	–	dB

Table 18. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	50	–	–	dB

DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 19. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output voltage	4.75	5.0	5.25	V	Average, neglecting ripple
V_{PUMP} 3V	3V Output voltage	3.00	3.25	3.60	V	Average, neglecting ripple
I_{PUMP}	Available Output Current V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.8V, V_{PUMP} = 5.0V	 8 5	 – –	 – –	 mA mA	For implementation, which includes 2 uH inductor, 1 uF cap, and Schottky diode
V_{BAT}5V	Input Voltage Range from Battery	1.8	–	5.0	V	
V_{BAT}3V	Input Voltage Range from Battery	1.0	–	3.3	V	
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.1	–	–	V	
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	$\%V_O$[a]	
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$[a]	
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on cap/load)	–	25	–	mVpp	Configuration of note 2, load is 5mA
–	Efficiency	35	50	–	%	Configuration of note 2, load is 5mA, Vout is 3.25V.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

a. V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 23 on page 25.

Figure 11. Basic Switch Mode Pump Circuit

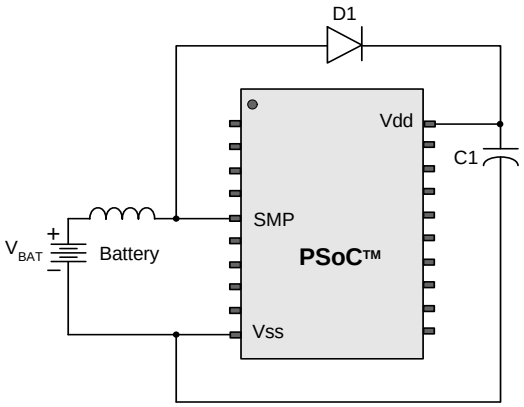


Table 21. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.274	1.30	1.326	V
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.037	Vdd/2 - 0.020	Vdd/2 + 0.002	V
–	AGND = 2 x BandGap[a] CT Block Power = High	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2) CT Block Power = High	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[a] CT Block Power = High	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[a] CT Block Power = High	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 3 x BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap Ref Control Power = High	Not Allowed			
–	RefLo = Vdd/2 - BandGap Ref Control Power = High	Not Allowed			
–	RefLo = BandGap Ref Control Power = High	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 24. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 25. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a]	MHz	Trimmed. Using factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b,e,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800[f]	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ T_A ≤ 85 °C.

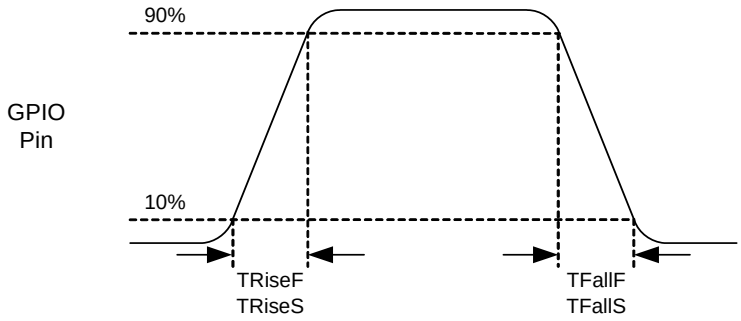
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 26. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 17. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 27. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.62	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.92	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.15	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.7	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	6.5	–		V/µs	
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.01	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	0.5	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	4.0	–		V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.75	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	3.1	–		MHz	
	Power = High				MHz	
	Power = High, Opamp Bias = High	5.4	–		MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

Table 28. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 3.92 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 5.41 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.31 2.7 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.24 1.8 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
BW_{OA}	Gain Bandwidth Product Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.67 2.8 – –	 – – – –	 – –	 MHz MHz MHz MHz MHz MHz	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 29. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	16.4	MHz	
Receiver	Maximum Input Clock Frequency	–	16	49.2	MHz	4.75V < Vdd < 5.25V

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Packaging Information

This section presents the packaging specifications for the CY8C24x23 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Figure 19. 8-Pin (300-Mil) PDIP

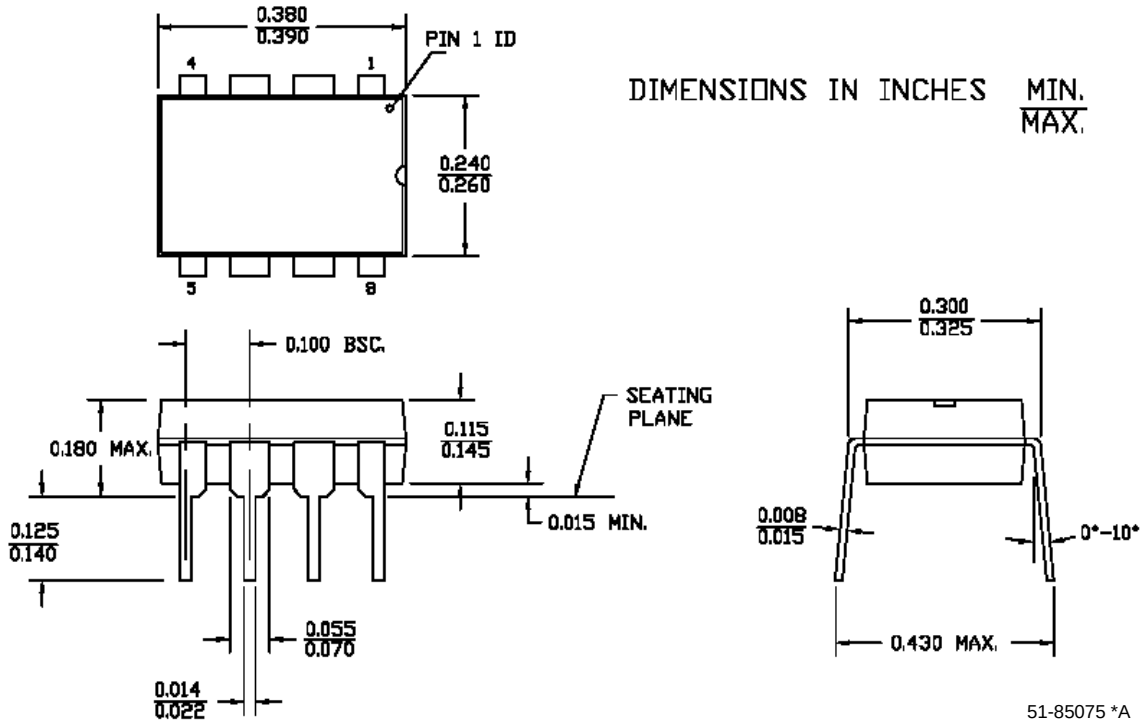


Figure 20. 8-Pin (150-Mil) SOIC

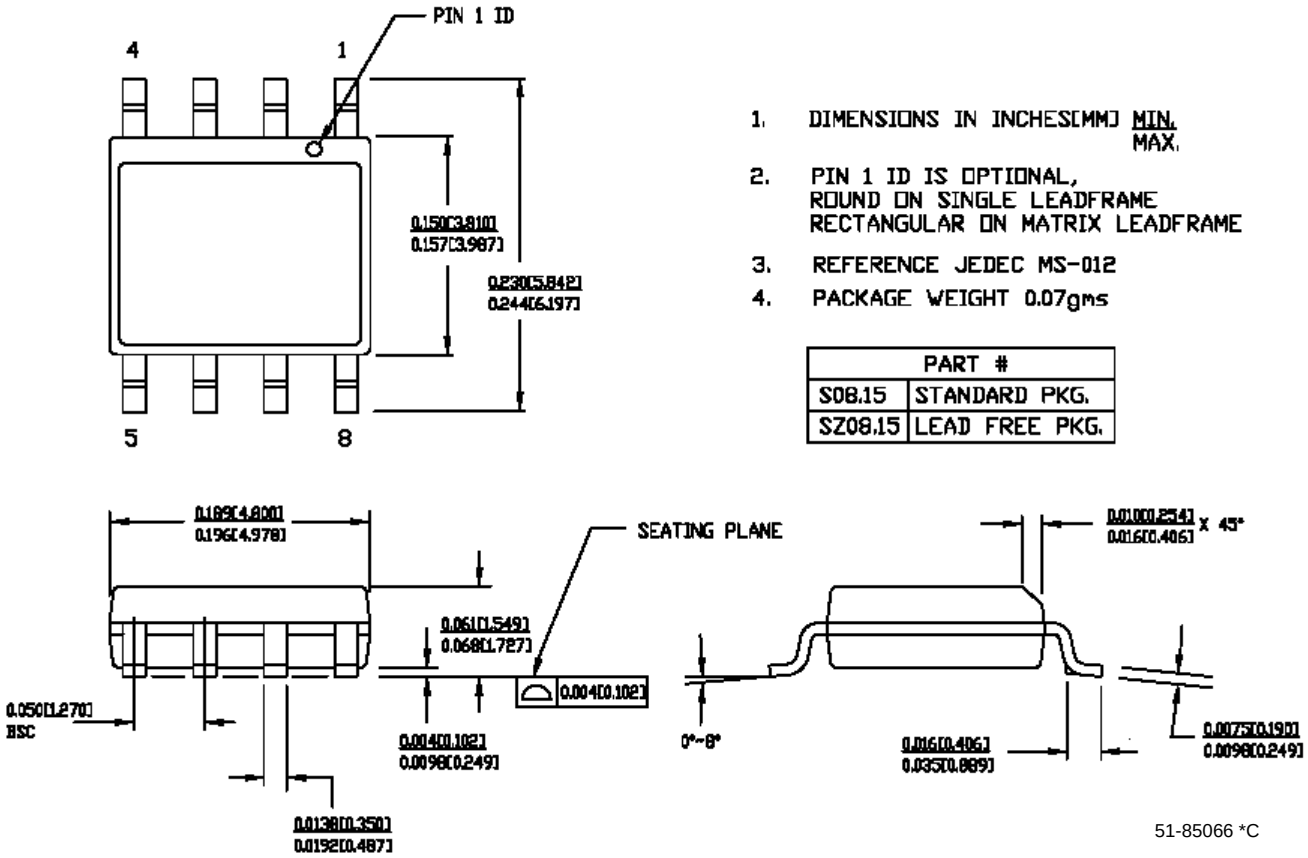


Figure 21. 20-Pin (300-Mil) Molded DIP

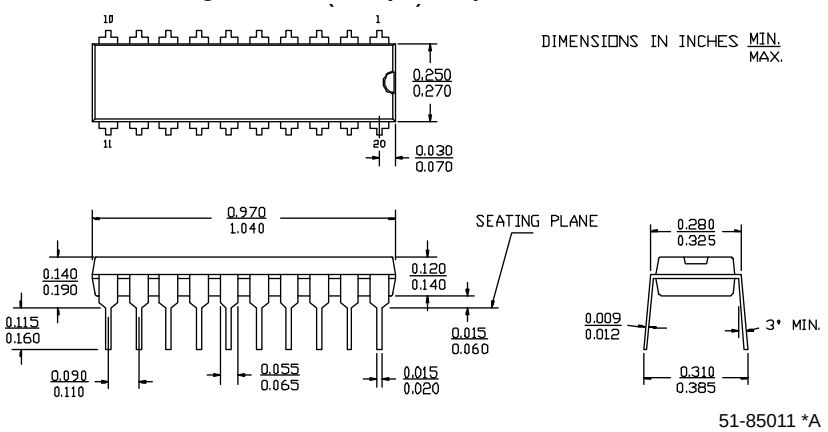
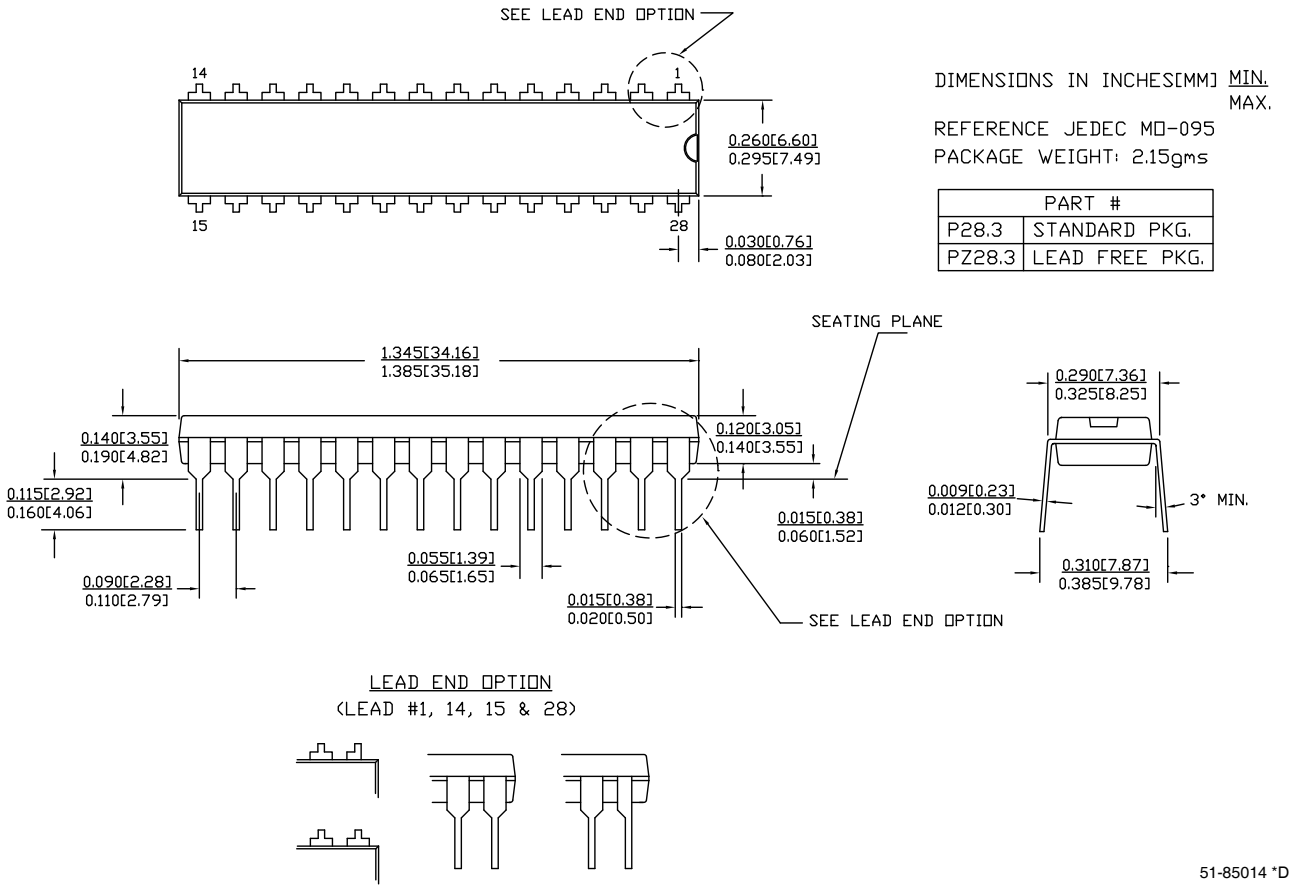


Figure 24. 28-Pin (300-Mil) Molded DIP



Ordering Information

The following table lists the CY8C24x23 PSoC Device family's key package features and ordering codes.

Table 38. CY8C24x23 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C24123-24PI	4	256	No	-40°C to +85°C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC	CY8C24123-24SI	4	256	Yes	-40°C to +85°C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C24123-24SIT	4	256	Yes	-40°C to +85°C	4	6	6	4	2	No
20 Pin (300 Mil) DIP	CY8C24223-24PI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP	CY8C24223-24PVI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223-24PVIT	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC	CY8C24223-24SI	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24223-24SIT	4	256	Yes	-40°C to +85°C	4	6	16	8	2	Yes
28 Pin (300 Mil) DIP	CY8C24423-24PI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423-24PVI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423-24PVIT	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC	CY8C24423-24SI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24423-24SIT	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes
32 Pin (5x5 mm) MLF	CY8C24423-24LFI	4	256	Yes	-40°C to +85°C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions