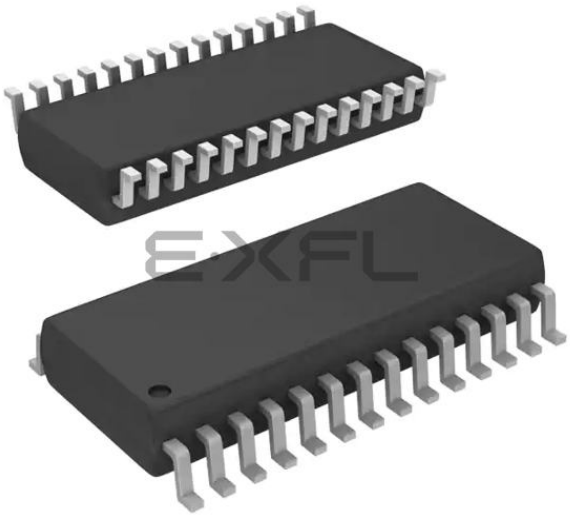

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423-24sit

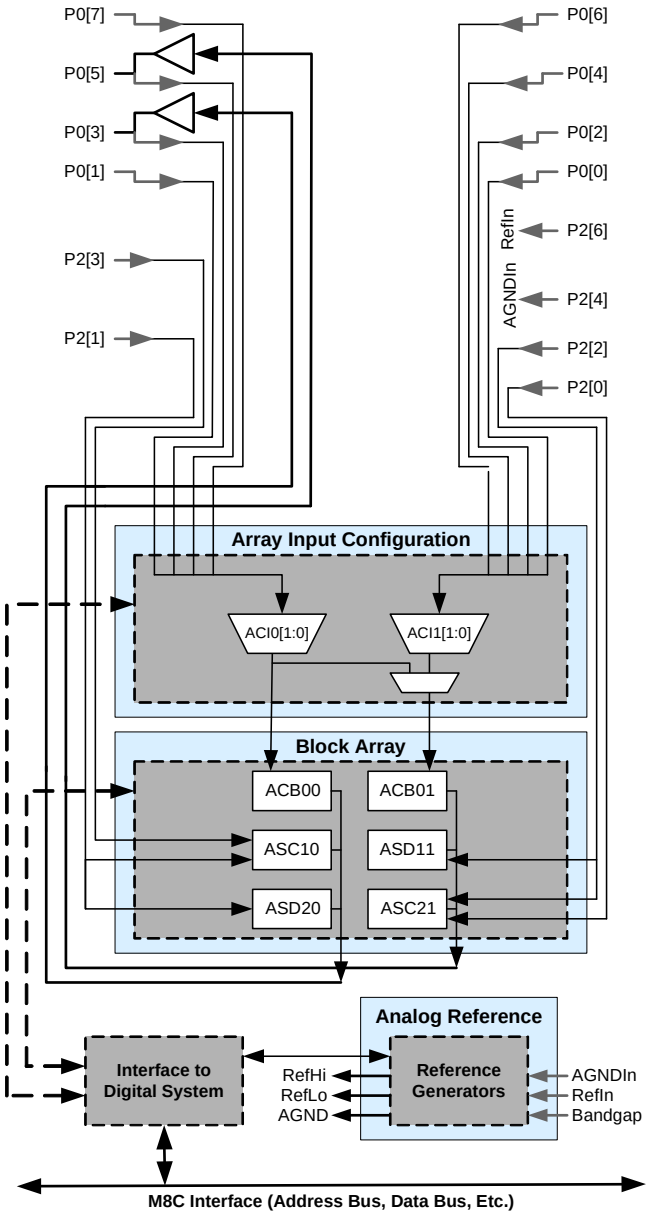
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table PSoC Device Characteristics on page 4.

Figure 2. Analog System Block Diagram



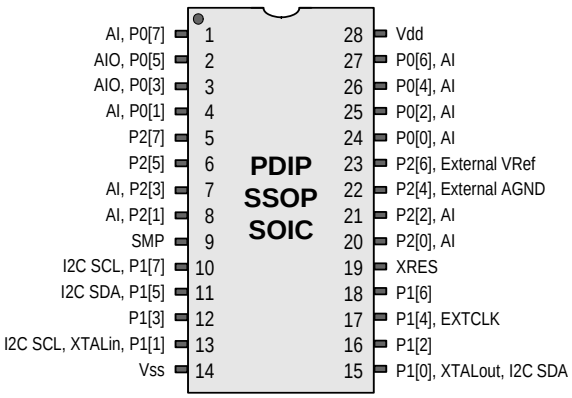
28-Pin Part Pinout

Table 5. 28-Pin Part Pinout (PDIP, SSOP, SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input
2	IO	IO	P0[5]	Analog column mux input and column output
3	IO	IO	P0[3]	Analog column mux input and column output
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input
8	IO	I	P2[1]	Direct switched capacitor block input
9	Power		SMP	Switch Mode Pump (SMP) connection to external components required
10	IO		P1[7]	I2C Serial Clock (SCL)
11	IO		P1[5]	I2C Serial Data (SDA)
12	IO		P1[3]	
13	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
14	Power		Vss	Ground connection
15	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK)
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20	IO	I	P2[0]	Direct switched capacitor block input
21	IO	I	P2[2]	Direct switched capacitor block input
22	IO		P2[4]	External Analog Ground (AGND)
23	IO		P2[6]	External Voltage Reference (VRef)
24	IO	I	P0[0]	Analog column mux input
25	IO	I	P0[2]	Analog column mux input
26	IO	I	P0[4]	Analog column mux input
27	IO	I	P0[6]	Analog column mux input
28	Power		Vdd	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 8. CY8C24423 28-Pin PSoC Device



Register Reference

This section lists the registers of the CY8C27xxx PSoC device by way of mapping tables, in offset order. For detailed register information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 7. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 8. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

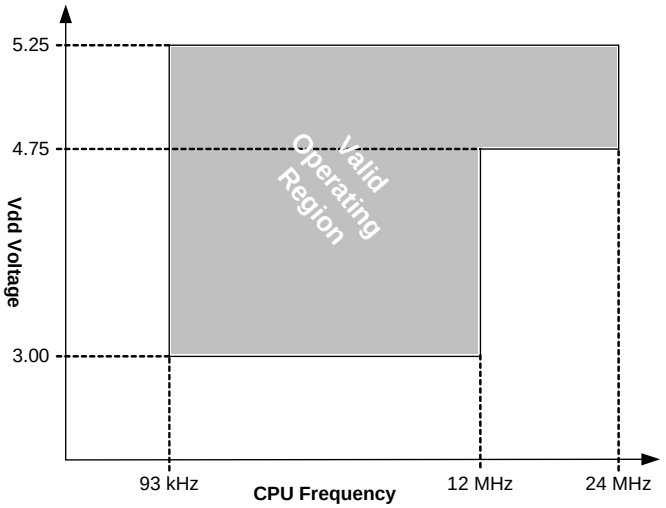
Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23 PSoC device. For latest electrical specifications, http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 10. Voltage versus Operating Frequency



The following table lists the units of measure that are used in this section.

Table 10. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
µA	micro ampere	pp	peak-to-peak
µF	micro farad	ppm	parts per million
µH	micro henry	ps	picosecond
µs	microsecond	sps	samples per second
µV	micro volts	s	sigma: one standard deviation
µVrms	micro volts root-mean-square	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+100	°C	Higher storage temperatures reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
–	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
–	Static Discharge Voltage	2000	–	–	V	
–	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 41. The user must limit the power consumption to comply with this requirement.

Table 15. 5V DC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	

Table 16. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power Input Offset Voltage (absolute value) Mid Power High Power is 5 Volt Only	– –	1.65 1.32	10 8	mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	–	–	dB	

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 17. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	–	–	dB

Table 18. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	50	–	–	dB

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 20. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.274	1.30	1.326	V
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.043	Vdd/2 - 0.025	Vdd/2 + 0.003	V
–	AGND = 2 x BandGap[a] CT Block Power = High	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a] CT Block Power = High	P2[4] - 0.013	P2[4]	P2[4] + 0.014	V
–	AGND = BandGap[a] CT Block Power = High	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[a] CT Block Power = High	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Vdd/2 + BG - 0.140	Vdd/2 + BG - 0.018	Vdd/2 + BG + 0.103	V
–	RefHi = 3 x BandGap Ref Control Power = High	3 x BG - 0.112	3 x BG - 0.018	3 x BG + 0.076	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V) Ref Control Power = High	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap Ref Control Power = High	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap Ref Control Power = High	Vdd/2 - BG - 0.051	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.098	V
–	RefLo = BandGap Ref Control Power = High	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V) Ref Control Power = High	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%.

Table 21. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.274	1.30	1.326	V
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.037	Vdd/2 - 0.020	Vdd/2 + 0.002	V
–	AGND = 2 x BandGap[a] CT Block Power = High	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2) CT Block Power = High	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[a] CT Block Power = High	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[a] CT Block Power = High	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 3 x BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap Ref Control Power = High	Not Allowed			
–	RefLo = Vdd/2 - BandGap Ref Control Power = High	Not Allowed			
–	RefLo = BandGap Ref Control Power = High	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 25. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a]	MHz	Trimmed. Using factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b,e,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800[f]	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ T_A ≤ 85 °C.

AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 26. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 17. GPIO Timing Diagram

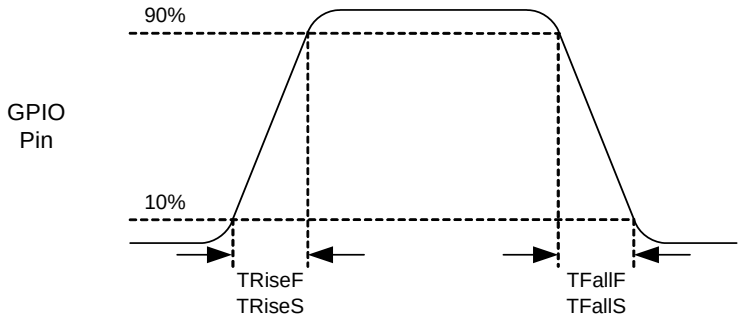


Table 28. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 3.92 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 – – – – –	 – – –	 5.41 0.72 –	 µs µs µs µs µs	Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.31 2.7 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
SR_{FOA}	Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.24 1.8 – –	 – – – –	 – –	 V/µs V/µs V/µs V/µs V/µs V/µs	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
BW_{OA}	Gain Bandwidth Product Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High (3.3 Volt High Bias Operation not supported) Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	 0.67 2.8 – –	 – – – –	 – –	 MHz MHz MHz MHz MHz MHz	Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	200	–	nV/rt-Hz	

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 29. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	16.4	MHz	
Receiver	Maximum Input Clock Frequency	–	16	49.2	MHz	4.75V < Vdd < 5.25V

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Figure 20. 8-Pin (150-Mil) SOIC

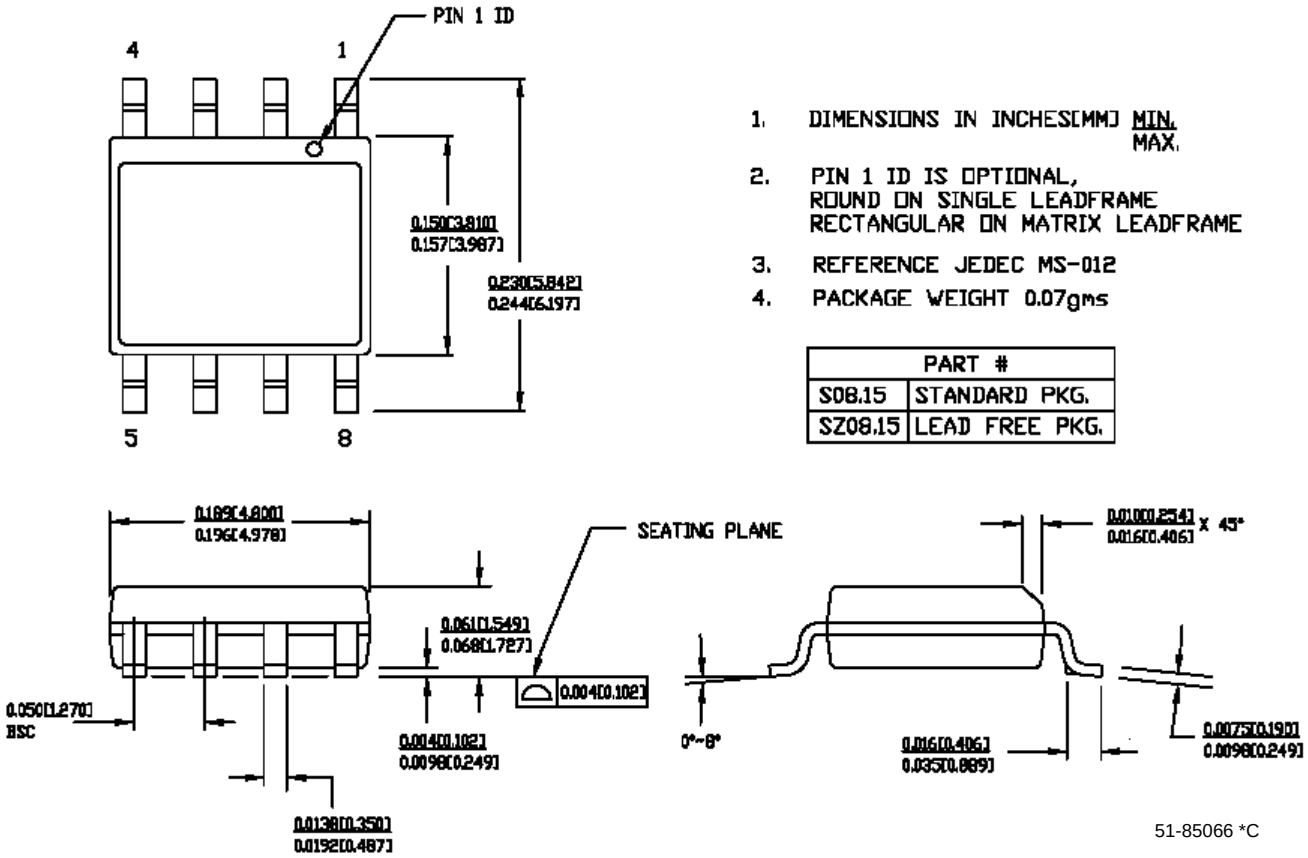


Figure 21. 20-Pin (300-Mil) Molded DIP

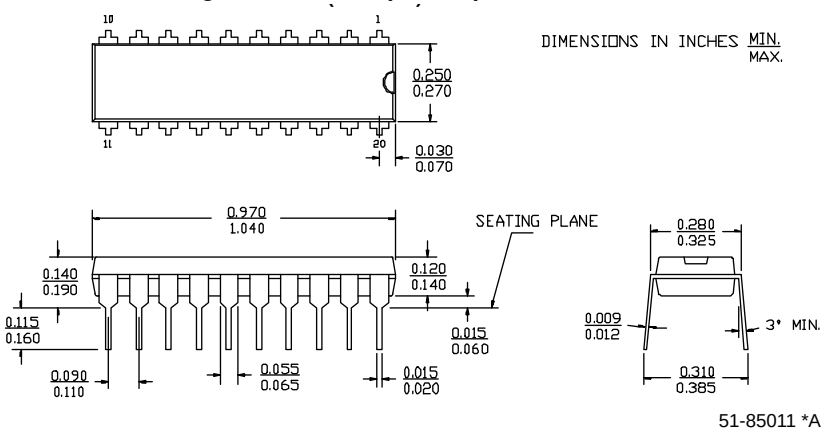


Figure 24. 28-Pin (300-Mil) Molded DIP

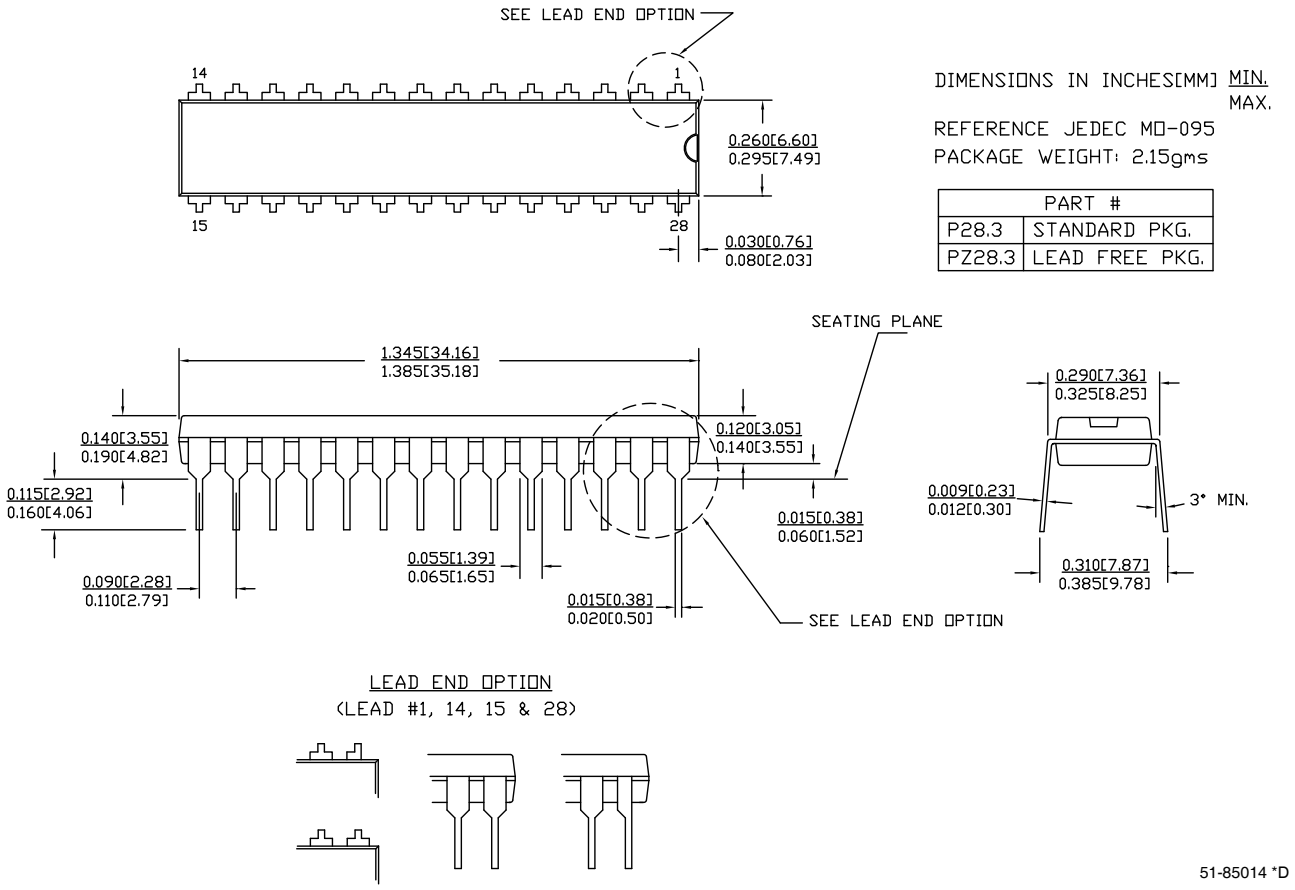


Figure 25. 28-Pin (210-Mil) SSOP

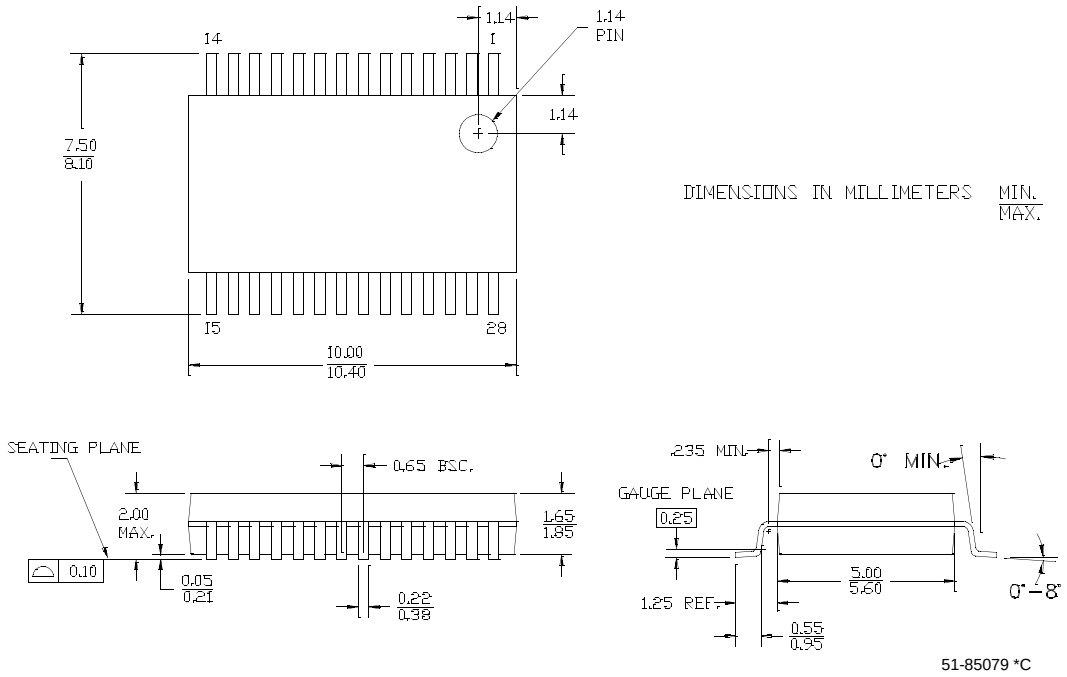
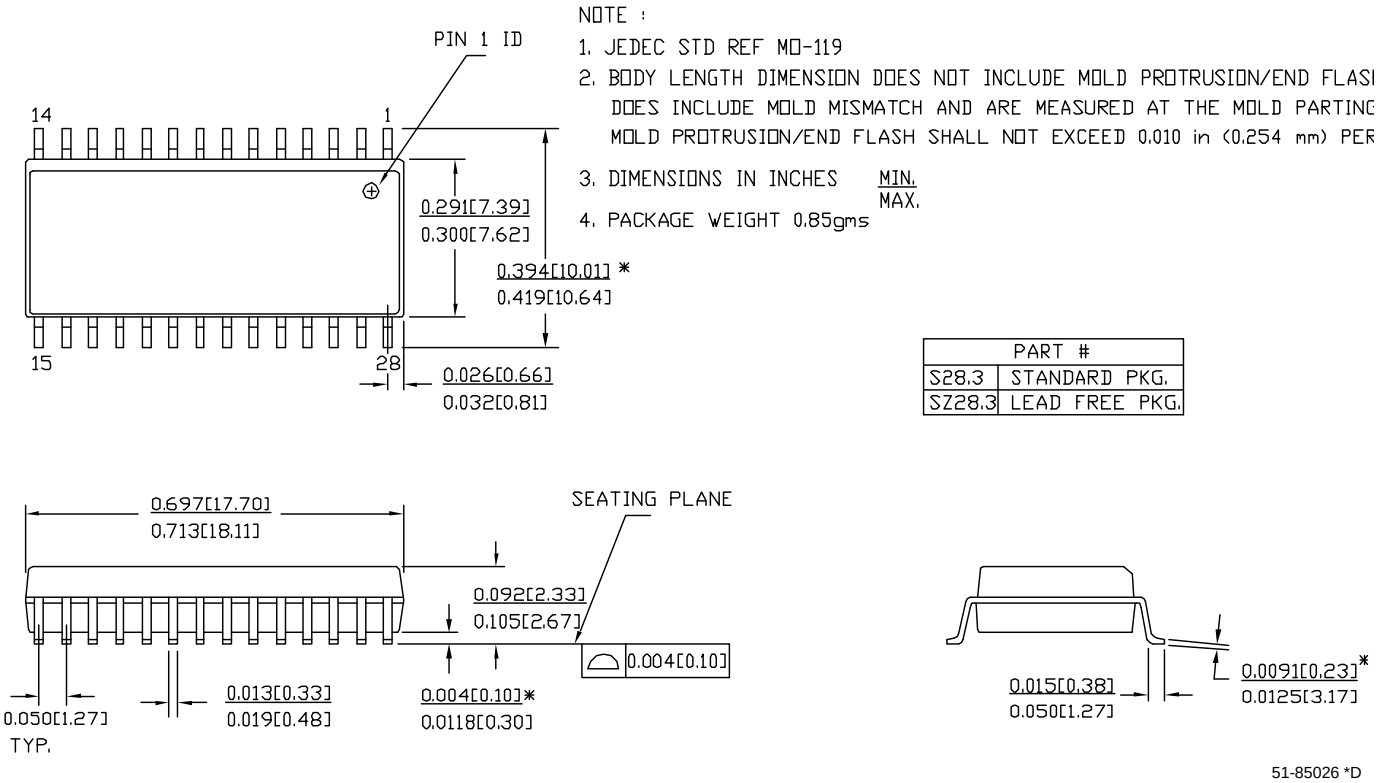


Figure 26. 28-Pin (300-Mil) Molded SOIC



Document History Page

Document Title: CY8C24123, CY8C24223, CY8C24423 PSoC® Programmable System-on-Chip™ Document Number: 38-12011				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	127043	New Silicon and NWJ	05/15/2003	New document – Advanced Data Sheet (two page product brief).
*A	128779	NWJ	08/13/2003	New document – Preliminary Data Sheet (300 page product detail).
*B	129775	MWR/NWJ	09/26/2003	Changes to Electrical Specifications section, Register Details chapter, and chapter changes in the Analog System section.
*C	130128	NWJ	10/14/2003	Revised document for Silicon Revision A.
*D	131678	NWJ	12/04/2003	Changes to Electrical Specifications section, Miscellaneous changes to I2C, GDI, RDI, Registers, and Digital Block chapters.
*E	131802	NWJ	12/22/2003	Changes to Electrical Specifications and miscellaneous small changes throughout the data sheet.
*F	229418	SFV	06/04/2004	New data sheet format and organization. Reference the *PSoC Programmable System-on-Chip Technical Reference Manual* for additional information. Title change.
*G	2619935	ONGE/AESA	12/11/2008	Changed title to “CY8C24123, CY8C24223, CY8C24423 PSoC® Programmable System-on-Chip™” Updated package diagrams 51-85188, 51-85024, 51-85014, and 51-85026. Added note on digital signaling in Table on page 23. Added Die Sales information note to Ordering Information on page 42. Updated data sheet template.

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