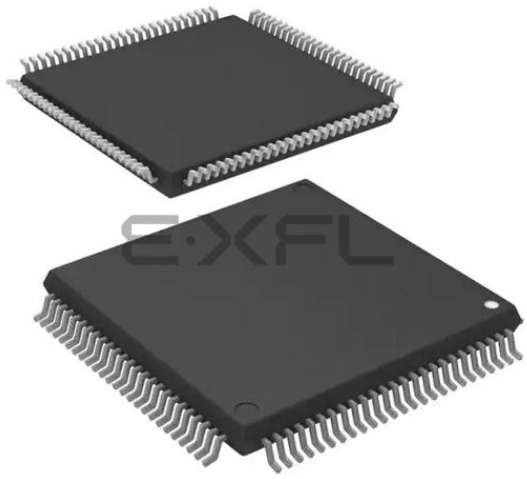
Renesas Electronics America Inc - UPD70F3794GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3794gc-ueu-ax

3.4.6 Peripheral I/O registers

(1/11)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF004H	Port DL register	PDL	R/W			√	0000H[Note]
FFFFF004H	Port DL register L	PDLL		√	√		00H[Note]
FFFFF005H	Port DL register H	PDLH		√	√		00H[Note]
FFFFF006H	Port DH register	PDH		√	√		00H[Note]
FFFFF00AH	Port CT register	PCT		√	√		00H[Note]
FFFFF00CH	Port CM register	PCM		√	√		00H[Note]
FFFFF024H	Port DL mode register	PMDL				√	FFFFH
FFFFF024H	Port DL mode register L	PMDLL		√	√		FFH
FFFFF025H	Port DL mode register H	PMDLH		√	√		FFH
FFFFF026H	Port DH mode register	PMDH		√	√		FFH
FFFFF02AH	Port CT mode register	PMCT		√	√		FFH
FFFFF02CH	Port CM mode register	PMCM		√	√		FFH
FFFFF044H	Port DL mode control register	PMCDL				√	0000H
FFFFF044H	Port DL mode control register L	PMCDLL		√	√		00H
FFFFF045H	Port DL mode control register H	PMCDLH		√	√		00H
FFFFF046H	Port DH mode control register	PMCDH		√	√		00H
FFFFF04AH	Port CT mode control register	PMCCT		√	√		00H
FFFFF04CH	Port CM mode control register	PMCCM		√	√		00H
FFFFF066H	Bus size configuration register	BSC				√	5555H
FFFFF06EH	System wait control register	VSWC			√		77H
FFFFF080H	DMA source address register 0L	DSA0L				√	Undefined
FFFFF082H	DMA source address register 0H	DSA0H				√	Undefined
FFFFF084H	DMA destination address register 0L	DDA0L				√	Undefined
FFFFF086H	DMA destination address register 0H	DDA0H				√	Undefined
FFFFF088H	DMA source address register 1L	DSA1L				√	Undefined
FFFFF08AH	DMA source address register 1H	DSA1H				√	Undefined
FFFFF08CH	DMA destination address register 1L	DDA1L				√	Undefined
FFFFF08EH	DMA destination address register 1H	DDA1H				√	Undefined
FFFFF090H	DMA source address register 2L	DSA2L				√	Undefined
FFFFF092H	DMA source address register 2H	DSA2H				√	Undefined
FFFFF094H	DMA destination address register 2L	DDA2L				√	Undefined
FFFFF096H	DMA destination address register 2H	DDA2H				√	Undefined
FFFFF098H	DMA source address register 3L	DSA3L				√	Undefined
FFFFF09AH	DMA source address register 3H	DSA3H				√	Undefined
FFFFF09CH	DMA destination address register 3L	DDA3L				√	Undefined
FFFFF09EH	DMA destination address register 3H	DDA3H				√	Undefined
FFFFF0C0H	DMA transfer count register 0	DBC0				√	Undefined
FFFFF0C2H	DMA transfer count register 1	DBC1				√	Undefined
FFFFF0C4H	DMA transfer count register 2	DBC2				√	Undefined
FFFFF0C6H	DMA transfer count register 3	DBC3				√	Undefined
FFFFF0D0H	DMA addressing control register 0	DADC0				√	0000H

Note The output latch is 00H or 0000H. When these registers are in the input mode, the pin statuses are read.

(1) Setting data to special registers

Set data to the special registers in the following sequence.

<1> Disable DMA operation.
<2> Prepare data to be set to the special register in a general-purpose register.
<3> Write the data prepared in <2> to the PRCMD register.
<4> Write the setting data to the special register (by using the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

(<5> to <9> Insert NOP instructions (5 instructions).)[Note]
<10> Enable DMA operation if necessary.

Note When switching to the IDLE mode or the STOP mode (PSC.STP bit = 1), 5 NOP instructions must be inserted immediately after switching is performed.

Caution To resume the DMA operation in the status before the DMA operation was disabled after a special sequence, the DCHCn register status must be stored before the DMA operation is disabled. After the DCHCn register status is stored, the DCHCn.TCn bit must be checked before the DMA operation is resumed and the following processing must be executed according to the TCn bit status, because completion of DMA transfer may occur before the DMA operation is disabled.

- **When the TCn bit is 0 (DMA transfer not completed), the contents of the DCHCn register stored before the DMA operation was disabled are written to the DCHCn register again.**
- **When the TCn bit is 1 (DMA transfer completed), DMA transfer completion processing is executed.**

Remark n = 0 to 3

[Example] PSC register (setting standby mode)

```
   ST.B r11, PSMR[r0]   ; Set PSMR register (setting IDLE1, IDLE2, and STOP modes).
<1>CLR1 0, DCHCn[r0]    ; Disable DMA operation.  n = 0 to 3
<2>MOV0x02, r10
<3>ST.B r10, PRCMD[r0]  ; Write PRCMD register.
<4>ST.B r10, PSC[r0]    ; Set PSC register.
<5>NOP[Note]            ; Dummy instruction
<6>NOP[Note]            ; Dummy instruction
<7>NOP[Note]            ; Dummy instruction
<8>NOP[Note]            ; Dummy instruction
<9>NOP[Note]            ; Dummy instruction
<10>SET1 0, DCHCn[r0]   ; Enable DMA operation.  n = 0 to 3
(next instruction)
```

There is no special sequence required to read a special register.

4.3.11 Port DL

Port DL is a 16-bit port for which I/O settings can be controlled in 1-bit units.

Port DL includes the following alternate-function pins.

Table 4-14. Port DL Alternate-Function Pins

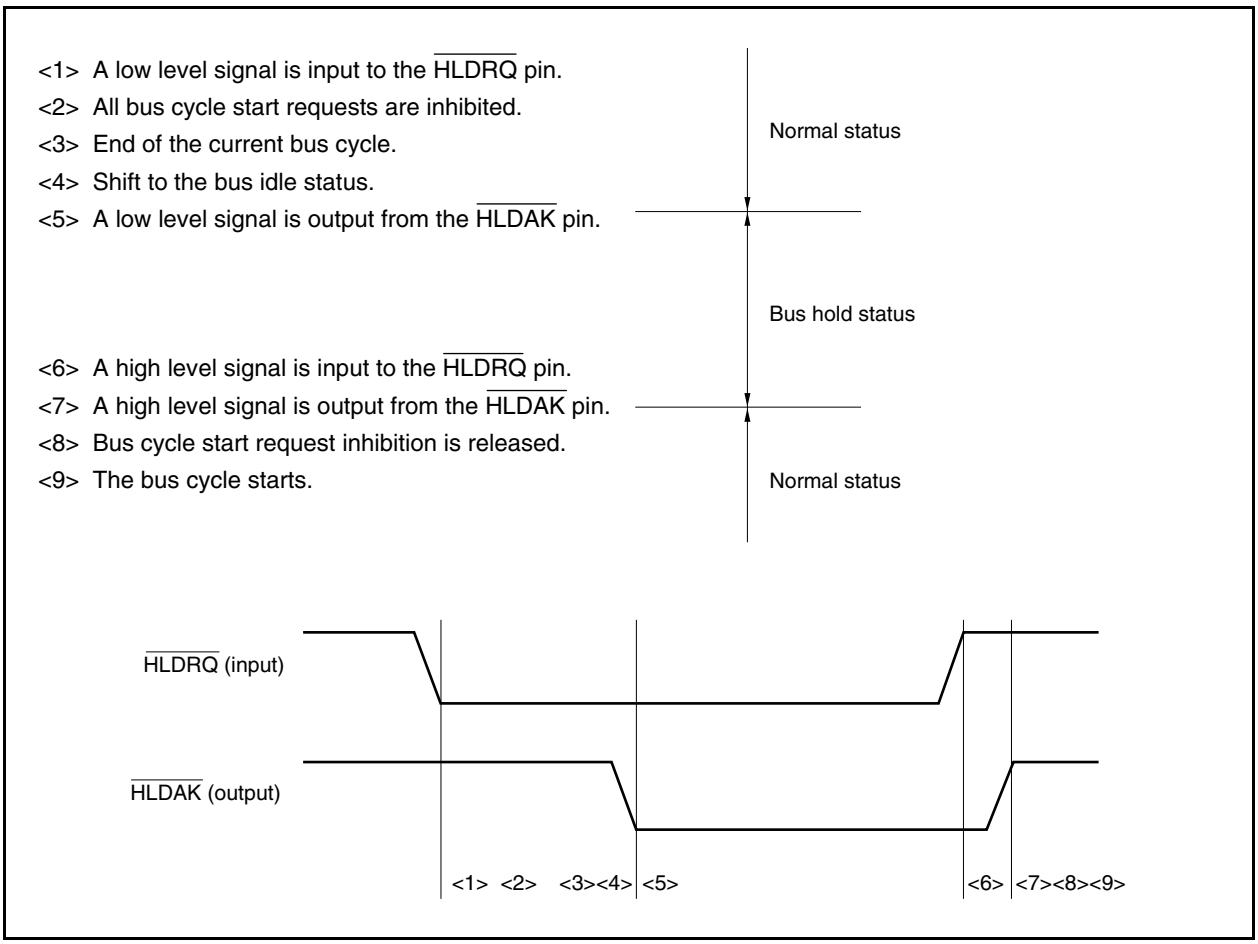
Pin No.		Function Name	Alternate Function		Remark	Block Type
GC	F1		Name	I/O		
71	C11	PDL0	AD0	I/O	–	D-3
72	C10	PDL1	AD1	I/O		D-3
73	C9	PDL2	AD2	I/O		D-3
74	B11	PDL3	AD3	I/O		D-3
75	B10	PDL4	AD4	I/O		D-3
76	A10	PDL5	AD5/FLMD1[Note]	I/O		D-3
77	A9	PDL6	AD6	I/O		D-3
78	B9	PDL7	AD7	I/O		D-3
79	A8	PDL8	AD8	I/O		D-3
80	B8	PDL9	AD9	I/O		D-3
81	C8	PDL10	AD10	I/O		D-3
82	A7	PDL11	AD11	I/O		D-3
83	B7	PDL12	AD12	I/O		D-3
84	C7	PDL13	AD13	I/O		D-3
85	D7	PDL14	AD14	I/O		D-3
86	B6	PDL15	AD15	I/O		D-3

Note Since this pin is set in the flash memory programming mode, it does not need to be manipulated by using the port control register. For details, see **CHAPTER 31 FLASH MEMORY**.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
F1: 121-pin plastic FBGA (8 × 8)

5.7.2 Bus hold procedure

The bus hold status transition procedure is shown below.

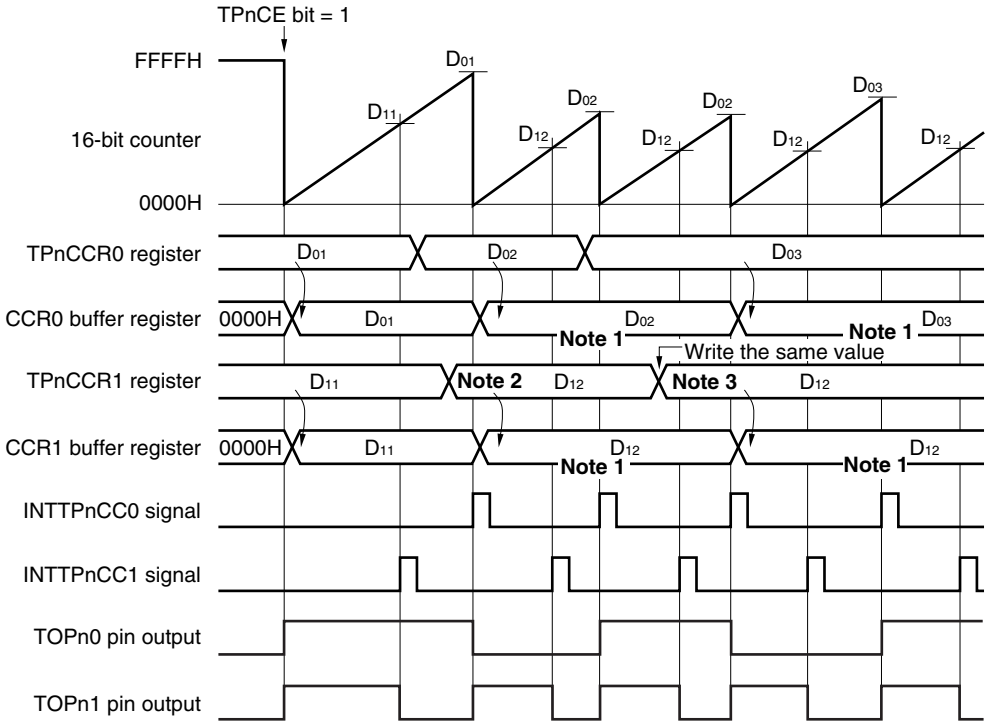


5.7.3 Operation in power save mode

Because the internal system clock is stopped in the STOP and IDLE modes, the bus hold status is not entered even if the $\overline{\text{HLDRQ}}$ pin is asserted.

In the HALT mode, the $\overline{\text{HLDAK}}$ pin is asserted as soon as the $\overline{\text{HLDRQ}}$ pin has been asserted, and the bus hold status is entered. When the $\overline{\text{HLDRQ}}$ pin is later deasserted, the $\overline{\text{HLDAK}}$ pin is also deasserted, and the bus hold status is exited.

Figure 7-5. Batch Write Timing



Notes 1. D_{03} is not transferred because the TPnCCR1 register was not written.

2. D_{12} is transferred to the CCR1 buffer register upon a match with the TPnCCR0 register value (D_{01}) because the TPnCCR1 register was written (D_{12}).

3. D_{12} is transferred to the CCR1 buffer register upon a match with the TPnCCR0 register value (D_{02}) because the TPnCCR1 register was written (D_{12}).

Remarks 1. D_{01}, D_{02}, D_{03}: Set value of TPnCCR0 register
D_{11}, D_{12}: Set value of TPnCCR1 register

2. The timing chart applies to the case when TMPn is being used as in the PWM output mode.

(3) Operation of interval timer based on input of external event count

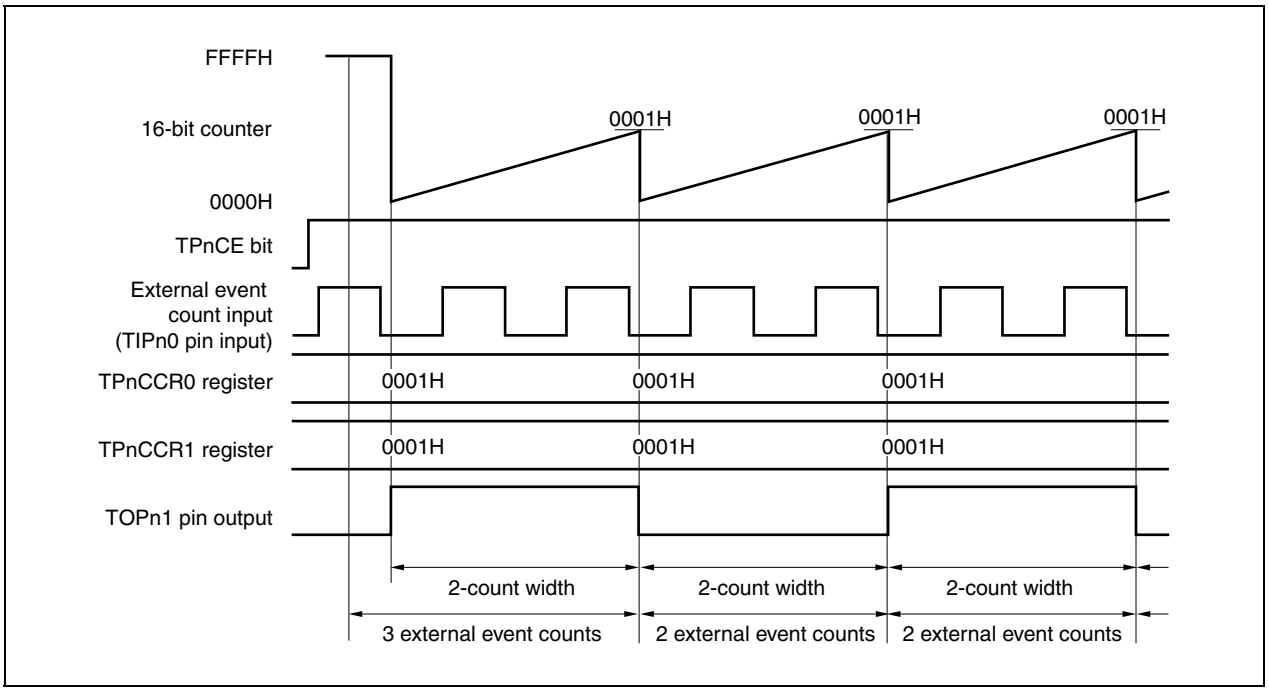
(a) Operation

When the 16-bit counter is incrementing based on the valid edge of the external count input (TIPn0 pin) in the interval timer mode, one external event count valid edge must be input immediately after the TPnCE bit changes from 0 to 1 to start the counter incrementing after the 16-bit counter is cleared from FFFFH to 0000H.

Once the TPnCCR0 and TPnCCR1 registers are set to 0001H (that is, the same value as was previously set), the TOPn1 pin output is inverted every two counts of the 16-bit counter.

Note that the TPnCTL1.TPnEEE bit can only be set to 1 when timer output (TOPn1) is used based on the input of an external event count.

Figure 7-16. Operation of Interval Timer Based on Input of External Event Count (TIPn0)



7.4.4 One-shot pulse output mode (TPnMD2 to TPnMD0 bits = 011)

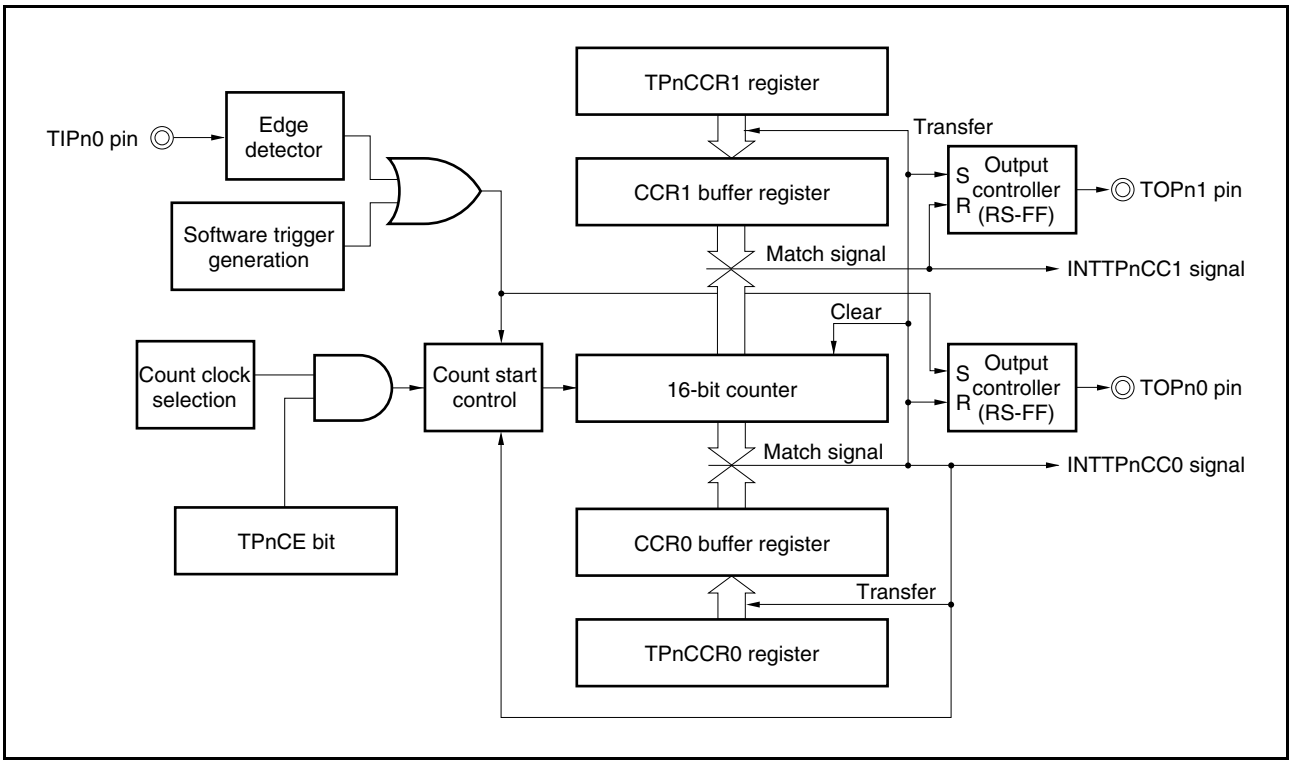
In the one-shot pulse output mode, when the TPnCTL0.TPnCE bit is set to 1, TMPn waits for a trigger, which is the valid edge of the external trigger input, and starts incrementing when this trigger is detected. TMPn then outputs a one-shot pulse from the TOPn1 pin.

Instead of the external trigger, a software trigger can also be generated to output the pulse. When the software trigger is used, the TOPn0 pin outputs the active level signal while the 16-bit counter is incrementing, and the inactive level signal when the counter is stopped (waiting for a trigger).

Remarks 1. For how to set the TIPn0, TOPn0, and TOPn1 pins, see **Table 7-2 Pins Used by TMPn** and **Table 4-15 Settings When Pins Are Used for Alternate Functions**.

2. For how to enable the INTTPnCC0 and INTTPnCC1 interrupt signals, see **CHAPTER 22 INTERRUPT SERVCING/EXCEPTION PROCESSING FUNCTION**.

Figure 7-38. Configuration of TMPn in One-Shot Pulse Output Mode



7.5 Selector

In the V850ES/JG3-L, the selector can be used to specify the capture trigger input for TMP as either a signal input to a port/timer alternate-function pin or peripheral I/O (TMP/UARTA) signal.

By using the selector, the following is possible:

- The TIP10 and TIP11 input signals of TMP1 can be selected as either the port/timer alternate-function pins (TIP10 and TIP11 pins) or the UARTA reception alternate-function pins (RXDA0 and RXDA1).
  → When the RXDA0 or RXDA1 signal of UART0 or UART1 is selected, the baud rate error in LIN reception transfer of UARTA can be calculated.

Cautions 1. When using the selector, set the capture trigger input of TMP before connecting the timer.
2. When setting the selector, first disable the peripheral I/O to be connected (TMP or UARTA).

The capture input for the selector is specified by the following register.

(1) Selector operation control register 0 (SELCNT0)

The SELCNT0 register is an 8-bit register that selects the capture trigger for TMP1.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF308H

	7	6	5	<4>	<3>	2	1	0
SELCNT0	0	0	0	ISEL4	ISEL3	0	0	0

ISEL4	Selection of TIP11 input signal (TMP1)
0	TIP11 pin input
1	RXDA1 pin input

ISEL3	Selection of TIP10 input signal (TMP1)
0	TIP10 pin input
1	RXDA0 pin input

Cautions 1. When setting the ISEL3 and ISEL4 bits to 1, set the corresponding pin to the capture input mode.
2. Be sure to clear bits 7 to 5 and 2 to 0 to "0".

(10) TMQ0 capture/compare register 3 (TQ0CCR3)

The TQ0CCR3 register can be used as a capture register or a compare register depending on the mode.

This register can be selected as a capture register or a compare register only in the free-running timer mode, according to the setting of the TQ0OPT0.TQ0CCS3 bit. In the pulse width measurement mode, the TQ0CCR3 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TQ0CCR3 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TQ0CCR3 register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing special on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R/W Address: FFFFF54CH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TQ0CCR3																

(a) Function as compare register

The TQ0CCR3 register can be rewritten even when the TQ0CTL0.TQ0CE bit = 1.

The set value of the TQ0CCR3 register is transferred to the CCR3 buffer register. When the value of the 16-bit counter matches the value of the CCR3 buffer register, a compare match interrupt request signal (INTTQ0CC3) is generated. If TOQ03 pin output is enabled at this time, the output of the TOQ03 pin is inverted (For details, see the descriptions of each operating mode.).

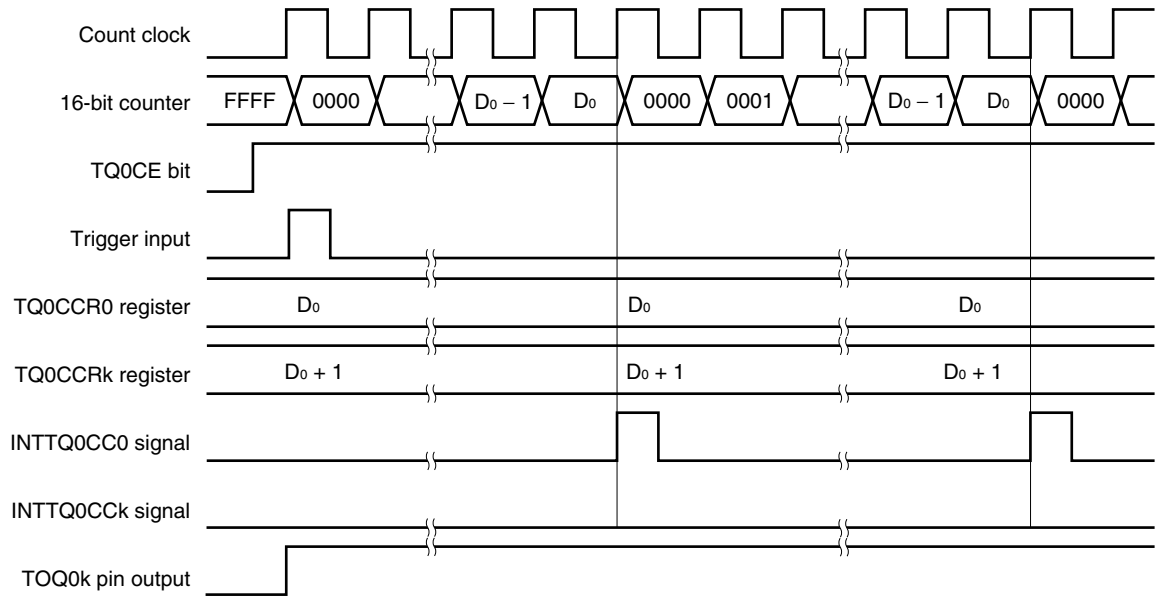
(b) Function as capture register

When the TQ0CCR3 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TQ0CCR3 register if the valid edge of the capture trigger input pin (TIQ03 pin) is detected. In the pulse-width measurement mode, the count value of the 16-bit counter is stored in the TQ0CCR3 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIQ03 pin) is detected.

Even if the capture operation and reading the TQ0CCR3 register conflict, the correct value of the TQ0CCR3 register can be read.

To output a 100% waveform, set the value of TQ0CCR0 register + 1 to the TQ0CCRk register.
If the value of the TQ0CCR0 register is FFFFH, a 100% waveform cannot be output.

Figure 8-32. Outputting 100% PWM Waveform



Remark k = 1 to 3

CHAPTER 10 WATCH TIMER

10.1 Functions

The watch timer has the following functions.

- Watch timer: An interrupt request signal (INTWT) is generated at intervals of 0.5 or 0.25 seconds by using the main clock or subclock.
- Interval timer: An interrupt request signal (INTWTI) is generated at set intervals.

The watch timer and interval timer functions can be used at the same time.

Caution INTWTI interrupt of the watch timer and INTRTC2 interrupt of RTC, and INTWT interrupt of the watch timer and INTRTC0 interrupt of RTC are alternate interrupt signals, and therefore cannot be used simultaneously.

(3) A/D converter mode register 2 (ADA0M2)

The ADA0M2 register specifies the hardware trigger mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF203H

	7	6	5	4	3	2	1	0
ADA0M2	0	0	0	0	0	0	ADA0TMD1	ADA0TMD0

ADA0TMD1	ADA0TMD0	Specification of hardware trigger mode
0	0	External trigger mode (when ADTRG pin valid edge is detected)
0	1	Timer trigger mode 0 (when INTTP2CC0 interrupt request is generated)
1	0	Timer trigger mode 1 (when INTTP2CC1 interrupt request is generated)
1	1	Setting prohibited

Cautions 1. In the following modes, write data to the ADA0M2 register while A/D conversion is stopped (ADA0M0.ADA0CE bit = 0), and then enable A/D conversion (ADA0CE bit = 1).

- **Normal conversion mode**
- **One-shot select mode/one-shot scan mode in high-speed conversion mode**

2. Be sure to clear bits 7 to 2 to "0".

14.5.5 Power-fail compare mode

In this mode, whether the input analog signal voltage is the specified voltage or higher or whether it is lower than the specified voltage is judged, and if the condition specified by the ADA0PFC bit is satisfied, the A/D conversion end interrupt request signal (INTAD) is generated.

- When the ADA0PFM.ADA0PFE bit is 0, the INTAD signal is generated each time A/D conversion is completed at the following timing (normal use of the A/D converter) .

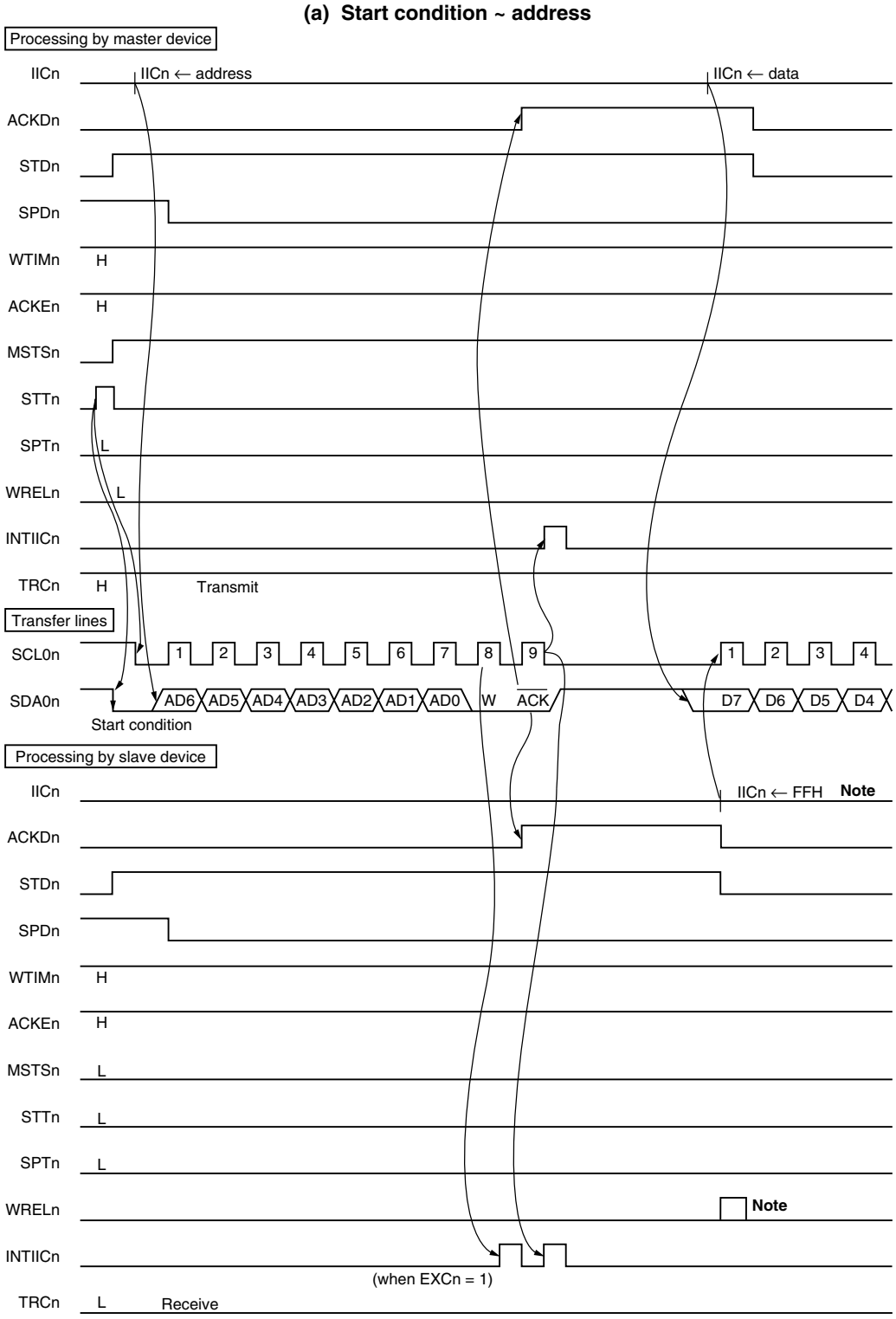
  - Continuous/one-shot select mode: After the fist A/D conversion is complete
  - Continuous/one-shot scan mode: After A/D conversions are performed sequentially for the analog input pins up to the one specified by the ADA0S register

- When the ADA0PFE bit is 1 and when the ADA0PFM.ADA0PFC bit is 0, the value of the ADA0CRnH register is compared with the value of the ADA0PFT register when conversion is completed, and the INTAD signal is generated only if ADA0CRnH ≥ ADA0PFT.
- When the ADA0PFE bit is 1 and when the ADA0PFC bit is 1, the value of the ADA0CRnH register is compared with the value of the ADA0PFT register when conversion is completed, and the INTAD signal is generated only if ADA0CRnH < ADA0PFT.

  Remark n = 0 to 11

In the power-fail compare mode, four modes are available: continuous select mode, continuous scan mode, one-shot select mode, and one-shot scan mode.

Figure 19-23. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

Remark n = 0 to 2

(12/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200386H	UF0 configuration/interface/endpoint descriptor register 224	UF0CIE224	R/W		√		Undefined
00200388H	UF0 configuration/interface/endpoint descriptor register 225	UF0CIE225	R/W		√		Undefined
0020038AH	UF0 configuration/interface/endpoint descriptor register 226	UF0CIE226	R/W		√		Undefined
0020038CH	UF0 configuration/interface/endpoint descriptor register 227	UF0CIE227	R/W		√		Undefined
0020038EH	UF0 configuration/interface/endpoint descriptor register 228	UF0CIE228	R/W		√		Undefined
00200390H	UF0 configuration/interface/endpoint descriptor register 229	UF0CIE229	R/W		√		Undefined
00200392H	UF0 configuration/interface/endpoint descriptor register 230	UF0CIE230	R/W		√		Undefined
00200394H	UF0 configuration/interface/endpoint descriptor register 231	UF0CIE231	R/W		√		Undefined
00200396H	UF0 configuration/interface/endpoint descriptor register 232	UF0CIE232	R/W		√		Undefined
00200398H	UF0 configuration/interface/endpoint descriptor register 233	UF0CIE233	R/W		√		Undefined
0020039AH	UF0 configuration/interface/endpoint descriptor register 234	UF0CIE234	R/W		√		Undefined
0020039CH	UF0 configuration/interface/endpoint descriptor register 235	UF0CIE235	R/W		√		Undefined
0020039EH	UF0 configuration/interface/endpoint descriptor register 236	UF0CIE236	R/W		√		Undefined
002003A0H	UF0 configuration/interface/endpoint descriptor register 237	UF0CIE237	R/W		√		Undefined
002003A2H	UF0 configuration/interface/endpoint descriptor register 238	UF0CIE238	R/W		√		Undefined
002003A4H	UF0 configuration/interface/endpoint descriptor register 239	UF0CIE239	R/W		√		Undefined
002003A6H	UF0 configuration/interface/endpoint descriptor register 240	UF0CIE240	R/W		√		Undefined
002003A8H	UF0 configuration/interface/endpoint descriptor register 241	UF0CIE241	R/W		√		Undefined
002003AAH	UF0 configuration/interface/endpoint descriptor register 242	UF0CIE242	R/W		√		Undefined
002003ACH	UF0 configuration/interface/endpoint descriptor register 243	UF0CIE243	R/W		√		Undefined
002003AEH	UF0 configuration/interface/endpoint descriptor register 244	UF0CIE244	R/W		√		Undefined
002003B0H	UF0 configuration/interface/endpoint descriptor register 245	UF0CIE245	R/W		√		Undefined

(32) UF0 GPR register (UF0GPR)

This register controls USBF and the USB interface.

This register is write-only, in 8-bit units. If this register is read, 00H is read. Be sure to clear bits 7 to 1 to “0”.

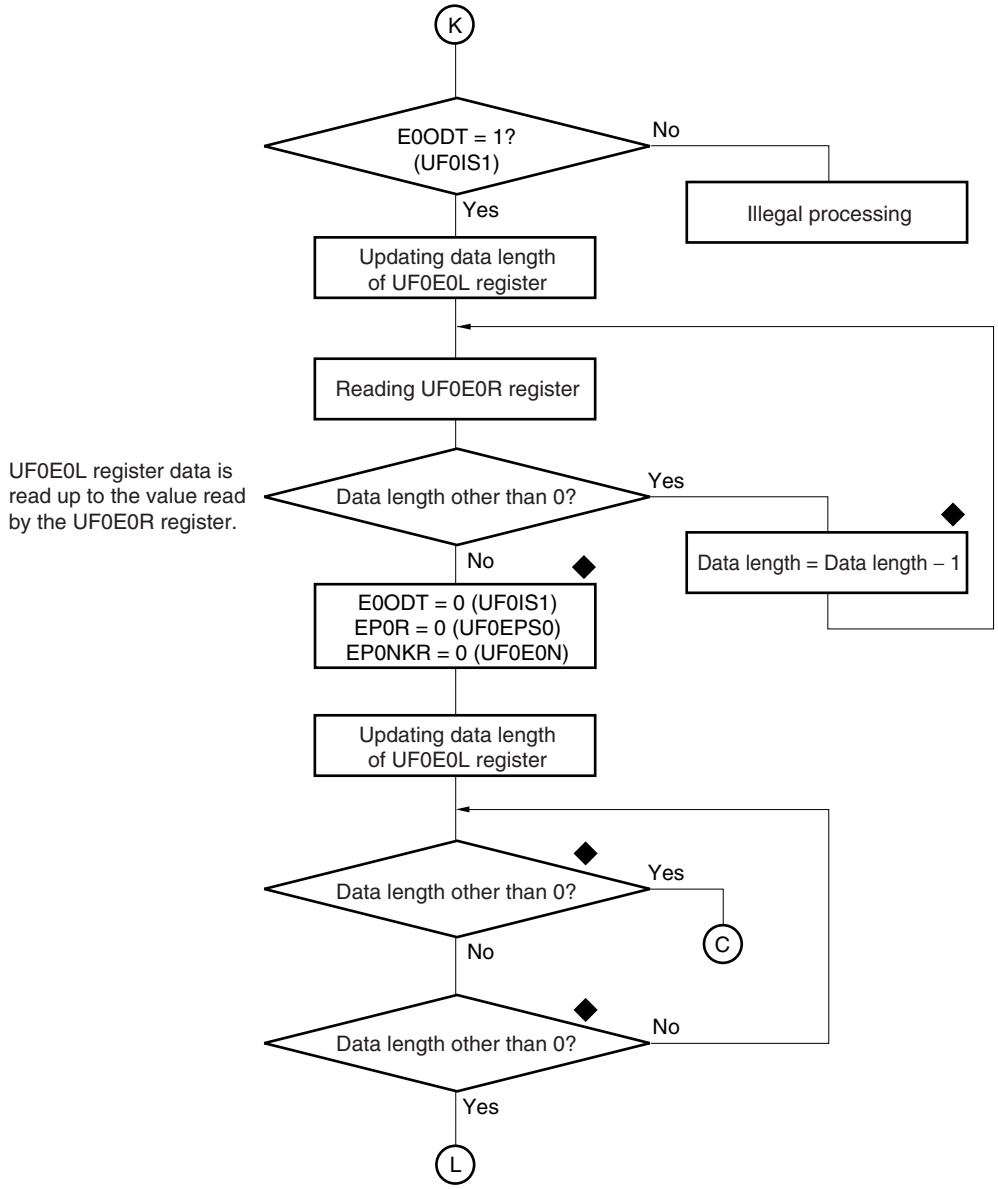
FW can reset the USBF by writing 1 to bit 0 of this register. This bit is automatically cleared to 0 after 1 has been written to it. Writing 0 to this bit is invalid.

	7	6	5	4	3	2	1	0	Address	After reset
UF0GPR	0	0	0	0	0	0	0	MRST	0020006EH	00H

Bit position	Bit name	Function
0	MRST	Set this bit to 1 to reset USBF. 1: Reset Actually, USBF is reset two USB clocks after this bit has been set to 1 by FW and the write signal has become inactive. Resetting USBF by the MRST bit while the system clock is operating has the same result as resetting by the $\overline{\text{RESET}}$ pin (hardware reset) (register value back to default value).

Figure 20-24. CPUDEC Request for Control Transfer (8/12)

(c) Control transfer (write) (2/4)



Remark ♦: Processing by hardware

After reset: FFFFH R/W Address: IMR3 FFFFF106H, IMR3L FFFFF106H, IMR3H FFFFF107H

	15	14	13	12	11	10	9	8
IMR3 (IMR3H[Note])	1	1	UC0TMK	UC0RMK	UA4TMK	UA4RMK	UA3TMK	UA3RMK
	7	6	5	4	3	2	1	0
IMR3L	RTC1MK	WTMK/ RTC0MK	WTMK/ RTC2MK	KRMK	DMAMK3	DMAMK2	DMAMK1	DMAMK0

After reset: FFFFH R/W Address: IMR2 FFFFF104H, IMR2L FFFFF104H, IMR2H FFFFF105H

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	ADMK	UA2TMK	UA2RMK/ IICMK0	UA1TMK	UA1RMK/ IIC2MK	UA0TMK/ CB4TMK	UA0RMK/ CB4RMK	CB3TMK
	7	6	5	4	3	2	1	0
IMR2L	CB3RMK	CB2TMK	CB2RMK	CB1TMK	CB1RMK	CB0TMK	CB0RMK/ IICMK1	TM0EQMK0

After reset: FFFFH R/W Address: IMR1 FFFFF102H, IMR1L FFFFF102H, IMR1H FFFFF103H

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	TP5CCMK1	TP5CCMK0	TP5OVMK	TP4CCMK1	TP4CCMK0	TP4OVMK	TP3CCMK1/ UA5TMK	TP3CCMK0
	7	6	5	4	3	2	1	0
IMR1L	TP3OVMK/ UA5RMK	TP2CCMK1	TP2CCMK0	TP2OVMK	TP1CCMK1/ UFMK0	TP1CCMK0	TP1OVMK/ UFMK1	TP0CCMK1

After reset: FFFFH R/W Address: IMR0 FFFFF100H, IMR0L FFFFF100H, IMR0H FFFFF101H

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	TP0CCMK0	TP0OVMK	TQ0CCMK3	TQ0CCMK2	TQ0CCMK1	TQ0CCMK0	TQ0OVMK	PMK7
	7	6	5	4	3	2	1	0
IMR0L	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

xxMKn	Setting of interrupt mask flag
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note To read or write bits 8 to 15 of the IMR0 to IMR3 registers in 8-bit or 1-bit units, specify them as bits 0 to 7 of IMR0H to IMR3H registers.

Caution Set bits 14 and 15 of the IMR3 register to 1. If the setting of these bits is changed, the operation is not guaranteed.

Remark xx: Identification name of each peripheral unit (see **Table 22-3 Interrupt Control Registers (xxICn)**).

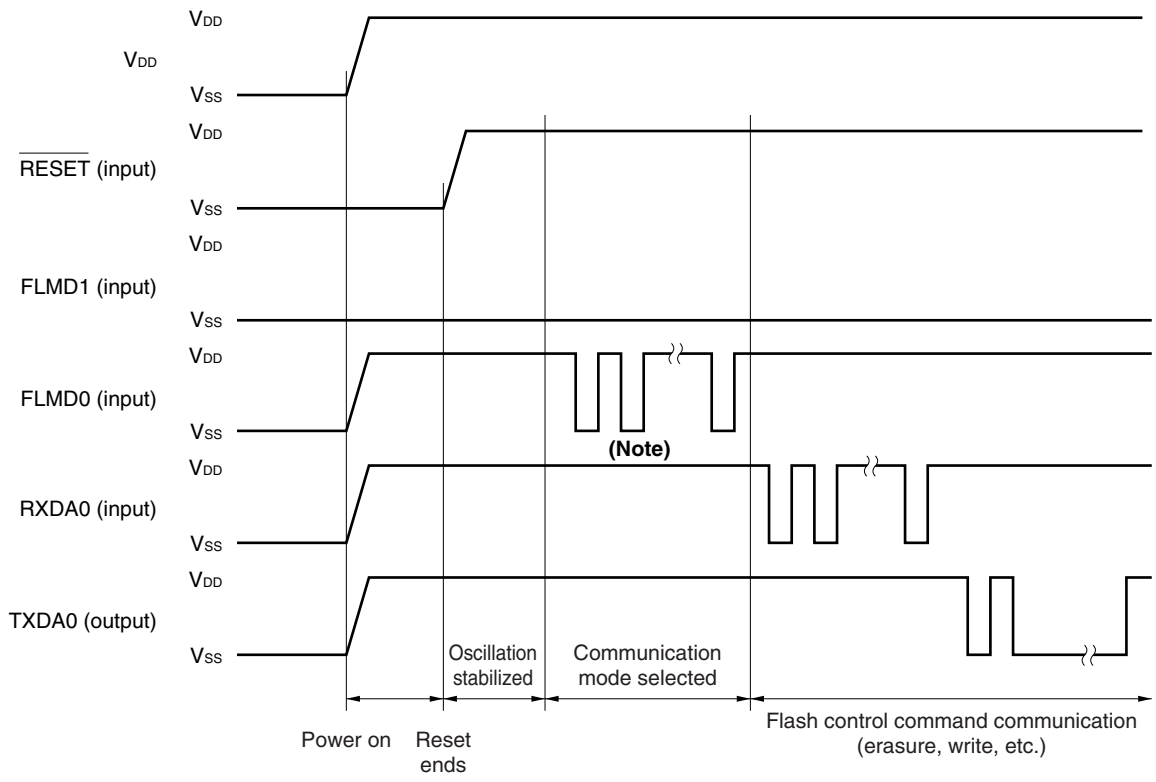
n: Peripheral unit number (see **Table 22-3 Interrupt Control Registers (xxICn)**)

31.4.5 Selection of communication mode

In the V850ES/JG3-L, the communication mode is selected by inputting pulses (12 pulses max.) to the FLMD0 pin after switching to the flash memory programming mode. The FLMD0 pulse is generated by the dedicated flash memory programmer.

The following shows the relationship between the number of pulses and the communication mode.

Figure 31-8. Selection of Communication Mode



Note The number of clocks is as follows according to the communication mode.

FLMD0 Pulse	Communication Mode	Remarks
0	UARTA0	Communication rate: 9,600 bps (after reset), LSB first
8	CSIB0	V850ES/JG3-L performs slave operation, MSB first
9	CSIB3	V850ES/JG3-L performs slave operation, MSB first
11	CSIB0 + HS	V850ES/JG3-L performs slave operation, MSB first
12	CSIB3 + HS	V850ES/JG3-L performs slave operation, MSB first
Other	RFU	Setting prohibited

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