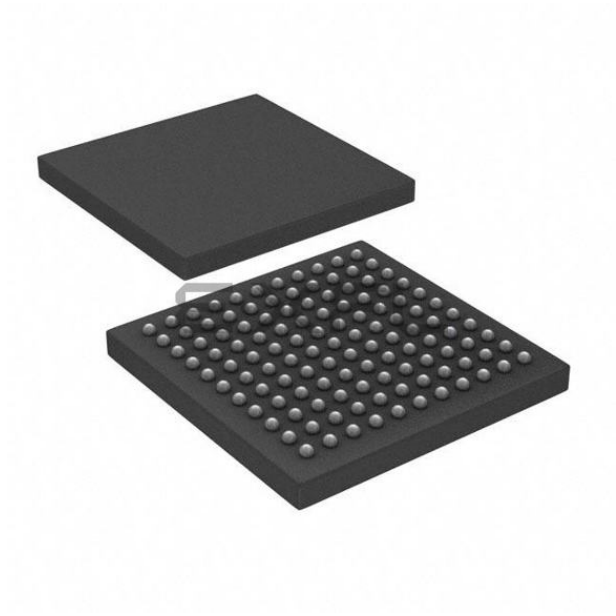
Renesas Electronics America Inc - UPD70F3795F1-CAH-A Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-LFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3795f1-cah-a

(19) DCU (debug control unit)

An on-chip debug function that uses the JTAG (Joint Test Action Group) communication specifications is provided. Switching between the normal port function and on-chip debugging function is done with the control pin input level and the OCDM register.

(20) Ports

The following general-purpose port functions and control pin functions are available.

Table 1-2. Port Functions

Port	I/O	Alternate Function
P0	5-bit I/O	NMI, external interrupt, A/D converter trigger, debug reset, real-time counter output
P1	2-bit I/O	D/A converter analog output
P3	7-bit I/O	External interrupt, serial interface, timer I/O
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Timer I/O, real-time output, key interrupt input, serial interface, debug I/O
P7	12-bit I/O	A/D converter analog input
P9	16-bit I/O	Serial interface, key interrupt input, timer I/O, external interrupt
PCM	4-bit I/O	External control signal
PCT	4-bit I/O	External control signal
PDH	5-bit I/O	External address bus
PDL	16-bit I/O	External address/data bus

(4/11)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF200H	A/D converter mode register 0	ADA0M0	R/W	√	√		00H
FFFFF201H	A/D converter mode register 1	ADA0M1		√	√		00H
FFFFF202H	A/D converter channel specification register	ADA0S		√	√		00H
FFFFF203H	A/D converter mode register 2	ADA0M2		√	√		00H
FFFFF204H	Power-fail compare mode register	ADA0PFM		√	√		00H
FFFFF205H	Power-fail compare threshold value register	ADA0PFT		√	√		00H
FFFFF210H	A/D conversion result register 0	ADA0CR0	R			√	Undefined
FFFFF211H	A/D conversion result register 0H	ADA0CR0H			√		Undefined
FFFFF212H	A/D conversion result register 1	ADA0CR1				√	Undefined
FFFFF213H	A/D conversion result register 1H	ADA0CR1H			√		Undefined
FFFFF214H	A/D conversion result register 2	ADA0CR2				√	Undefined
FFFFF215H	A/D conversion result register 2H	ADA0CR2H			√		Undefined
FFFFF216H	A/D conversion result register 3	ADA0CR3				√	Undefined
FFFFF217H	A/D conversion result register 3H	ADA0CR3H			√		Undefined
FFFFF218H	A/D conversion result register 4	ADA0CR4				√	Undefined
FFFFF219H	A/D conversion result register 4H	ADA0CR4H			√		Undefined
FFFFF21AH	A/D conversion result register 5	ADA0CR5				√	Undefined
FFFFF21BH	A/D conversion result register 5H	ADA0CR5H			√		Undefined
FFFFF21CH	A/D conversion result register 6	ADA0CR6				√	Undefined
FFFFF21DH	A/D conversion result register 6H	ADA0CR6H			√		Undefined
FFFFF21EH	A/D conversion result register 7	ADA0CR7				√	Undefined
FFFFF21FH	A/D conversion result register 7H	ADA0CR7H			√		Undefined
FFFFF220H	A/D conversion result register 8	ADA0CR8				√	Undefined
FFFFF221H	A/D conversion result register 8H	ADA0CR8H			√		Undefined
FFFFF222H	A/D conversion result register 9	ADA0CR9				√	Undefined
FFFFF223H	A/D conversion result register 9H	ADA0CR9H			√		Undefined
FFFFF224H	A/D conversion result register 10	ADA0CR10				√	Undefined
FFFFF225H	A/D conversion result register 10H	ADA0CR10H			√		Undefined
FFFFF226H	A/D conversion result register 11	ADA0CR11				√	Undefined
FFFFF227H	A/D conversion result register 11H	ADA0CR11H			√		Undefined
FFFFF280H	D/A conversion value setting register 0	DA0CS0	R/W		√		00H
FFFFF281H	D/A conversion value setting register 1	DA0CS1			√		00H
FFFFF282H	D/A converter mode register	DA0M		√	√		00H
FFFFF300H	Key return mode register	KRM		√	√		00H
FFFFF308H	Selector operation control register 0	SELCNT0		√	√		00H
FFFFF310H	CRC input register	CRCIN			√		00H
FFFFF312H	CRC data register	CRCD				√	0000H
FFFFF318H	Noise elimination control register	NFC			√		00H
FFFFF320H	Prescaler mode register 1	PRSM1		√	√		00H
FFFFF321H	Prescaler compare register 1	PRSCM1			√		00H
FFFFF324H	Prescaler mode register 2	PRSM2		√	√		00H
FFFFF325H	Prescaler compare register 2	PRSCM2			√		00H
FFFFF328H	Prescaler mode register 3	PRSM3		√	√		00H
FFFFF329H	Prescaler compare register 3	PRSCM3			√		00H

4.3.2 Port 1

Port 1 is a 2-bit port for which I/O settings can be controlled in 1-bit units.

Port 1 includes the following alternate-function pins.

Table 4-5. Port 1 Alternate-Function Pins

Pin No.		Function Name	Alternate Function		Remark	Block Type
GC	F1		Name	I/O		
3	E3	P10	ANO0	Output	–	A-2
4	E4	P11	ANO1	Output	–	A-2

Caution When the power is turned on, the P10 and P11 pins may output an undefined level temporarily even during reset.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
F1: 121-pin plastic FBGA (8 × 8)

(1) Port 1 register (P1)

After reset: 00H (output latch) R/W Address: FFFFF402H

	7	6	5	4	3	2	1	0
P1	0	0	0	0	0	0	P11	P10

P1n	Output data control (in output mode) (n = 0, 1)
0	Outputs 0
1	Outputs 1

Caution Do not read or write the P1 register during D/A conversion (see 15.4.3 Cautions).

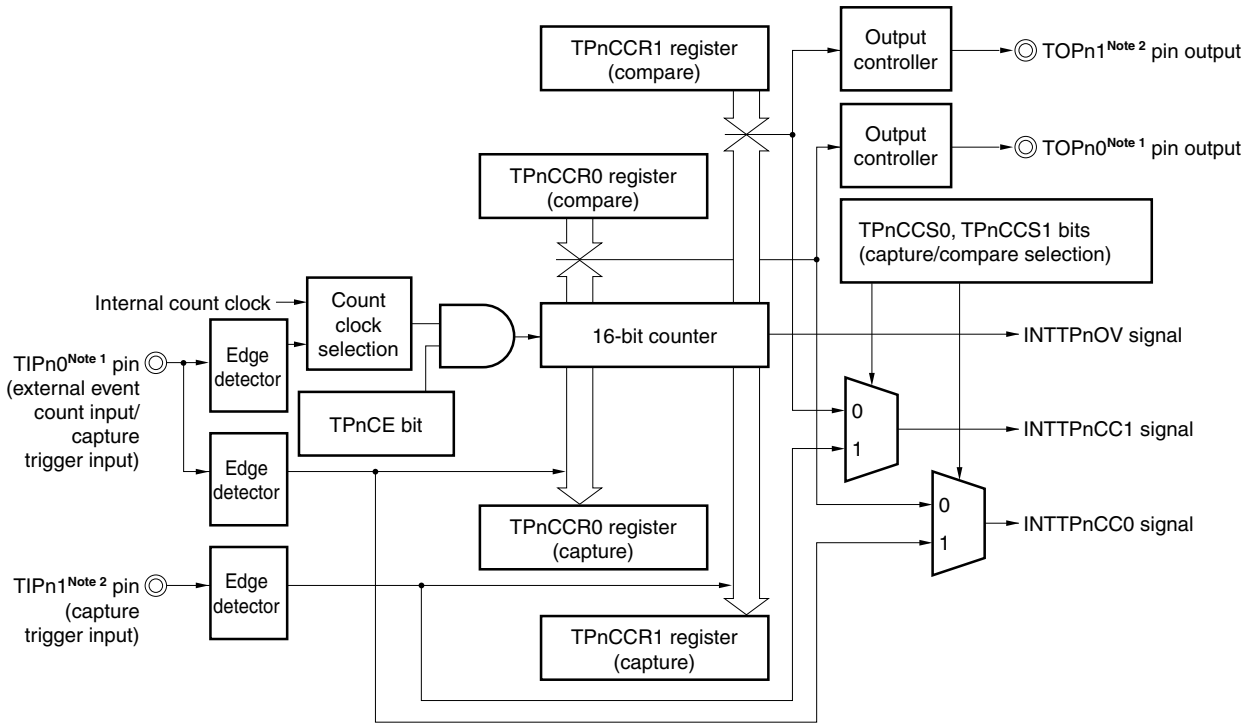
7.4.6 Free-running timer mode (TPnMD2 to TPnMD0 bits = 101)

In the free-running timer mode, TMPn starts incrementing when the TPnCTL0.TPnCE bit is set to 1. At this time, the TPnCCRa register can be used as a compare register or a capture register, according to the setting of the TPnOPT0.TPnCCS0 and TPnOPT0.TPnCCS1 bits.

Remarks 1. For how to set the TIPn0, TIPn1, TOPn0, and TOPn1 pins, see **Table 7-2 Pins Used by TMPn** and **Table 4-15 Settings When Pins Are Used for Alternate Functions**.

2. For how to enable the INTTPnCC0 and INTTPnCC1 interrupt signals, see **CHAPTER 22 INTERRUPT SERVICING/EXCEPTION PROCESSING FUNCTION**.

Figure 7-52. Configuration of TMPn in Free-Running Timer Mode

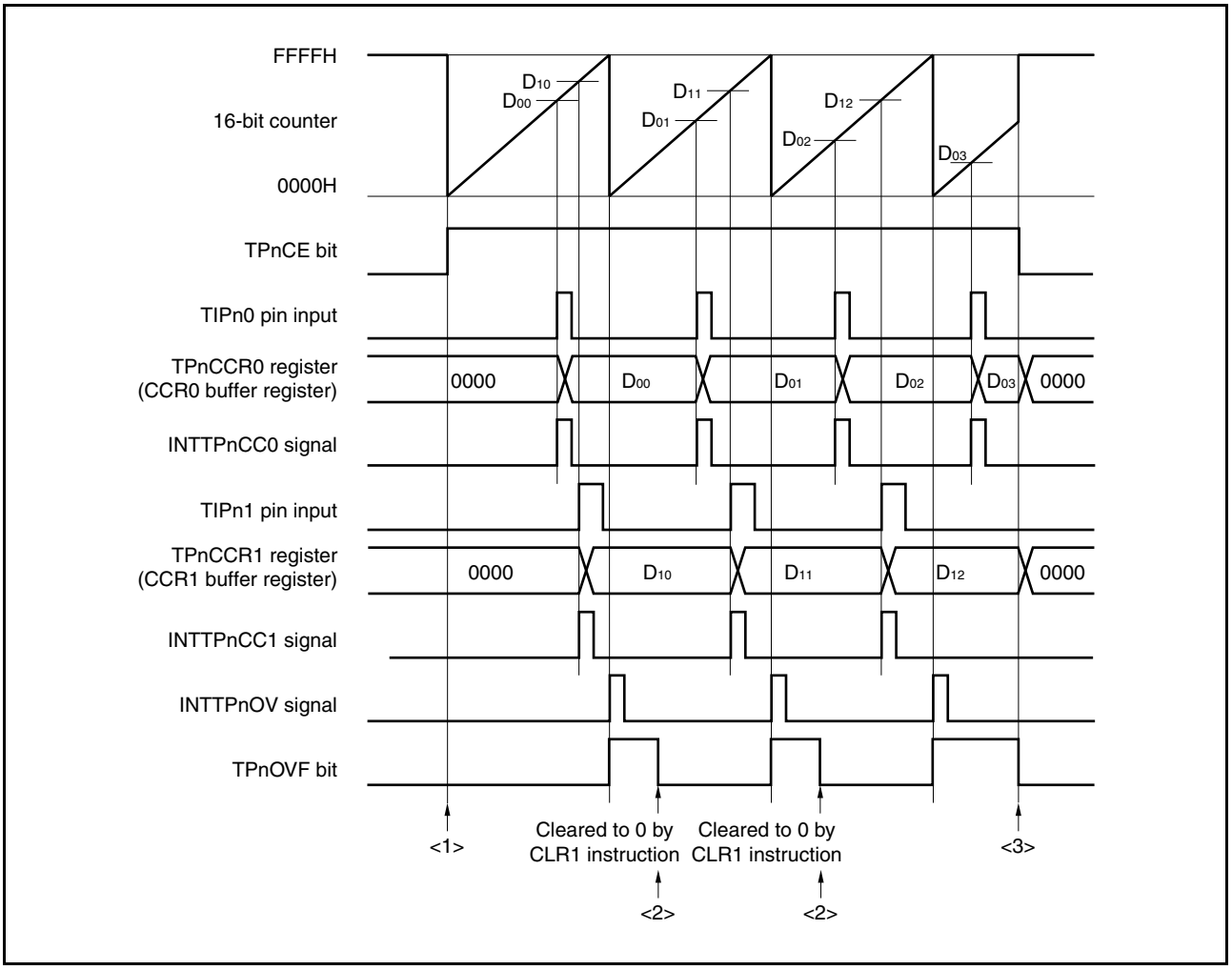


Notes 1. The external event count input/capture trigger input pin (TIPn0) can also be used as the timer output pin (TOPn0); however, only one of these functions can be used at a time.

2. The capture trigger input pin (TIPn1) can also be used as the timer output pin (TOPn1); however, only one of these functions can be used at a time.

(b) Using a capture/compare register as a capture register

Figure 7-57. Timing and Processing of Operations in Free-Running Timer Mode (Capture Function) (1/2)



(2) Using one-shot pulse mode

(a) Rewriting the TQ0CCRm register

When rewriting the value of the TQ0CCRm register to a smaller value, stop counting first and then change the set value.

When changing the value of the TQ0CCR0 register from D_{00} to D_{01} and the value of the TQ0CCRk register from D_{k0} to D_{k1}, if the registers are rewritten under any of the following conditions, a one-shot pulse will not be output as expected.

Condition 1 When rewriting the TQ0CCR0 register, if:

$D_{00} > D_{01}$ or,

$D_{00} <$ 16-bit counter value $< D_{01}$

In the case of condition 1, the 16-bit counter will not be cleared and will overflow in the cycle in which the new value is being written. The counter will be cleared for the first time at the newly written value (D_{01}).

Condition 2 When rewriting the TQ0CCRk register, if:

$D_{k0} > D_{k1}$ or,

$D_{k0} <$ 16-bit counter value $< D_{k1}$

In the case of condition 2, the TOQ0k pin output cannot be inverted to the active level in the cycle in which the new value is being written.

An example of what happens when condition 1 and condition 2 are satisfied in the same cycle is shown in Figure 8-42.

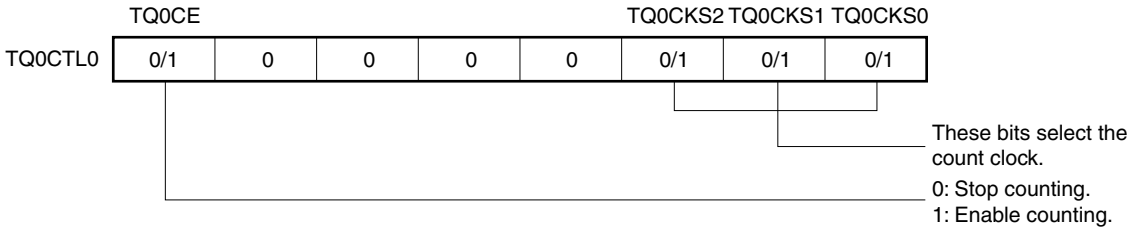
The 16-bit counter increments up to FFFFH, overflows, and starts incrementing again from 0000H.

When the 16-bit counter value matches D_{k1}, the INTTQ0CCk signal is generated and the TOQ0k pin output is set to the active level. Subsequently, when the 16-bit counter value matches D_{01}, the INTTQ0CC0 signal is generated, the TOQ0k pin output is set to the inactive level, and the counter stops incrementing.

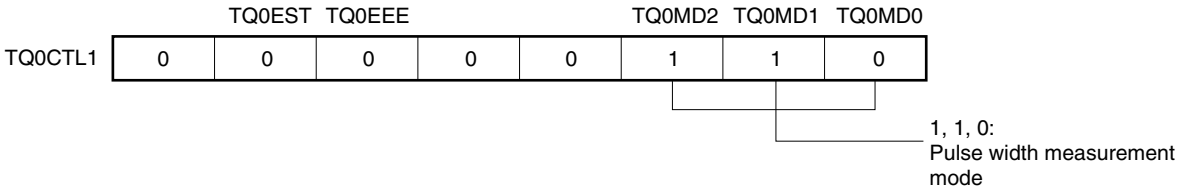
Remark m = 0 to 3
K = 1 to 3

Figure 8-67. Register Settings in Pulse Width Measurement Mode (1/2)

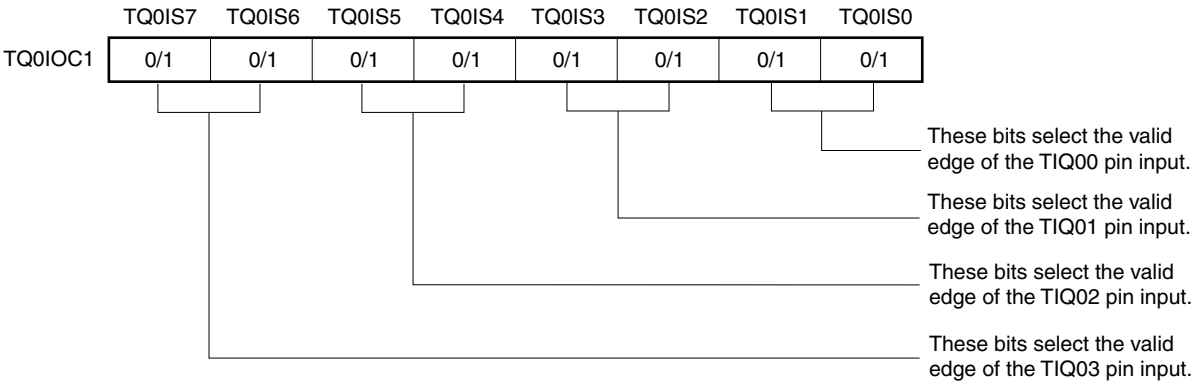
(a) TMQ0 control register 0 (TQ0CTL0)



(b) TMQ0 control register 1 (TQ0CTL1)



(c) TMQ0 I/O control register 1 (TQ0IOC1)



(d) TMQ0 option register 0 (TQ0OPT0)

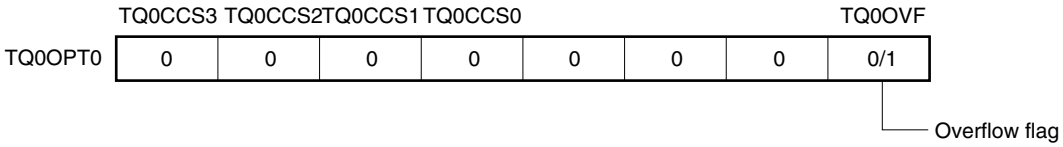
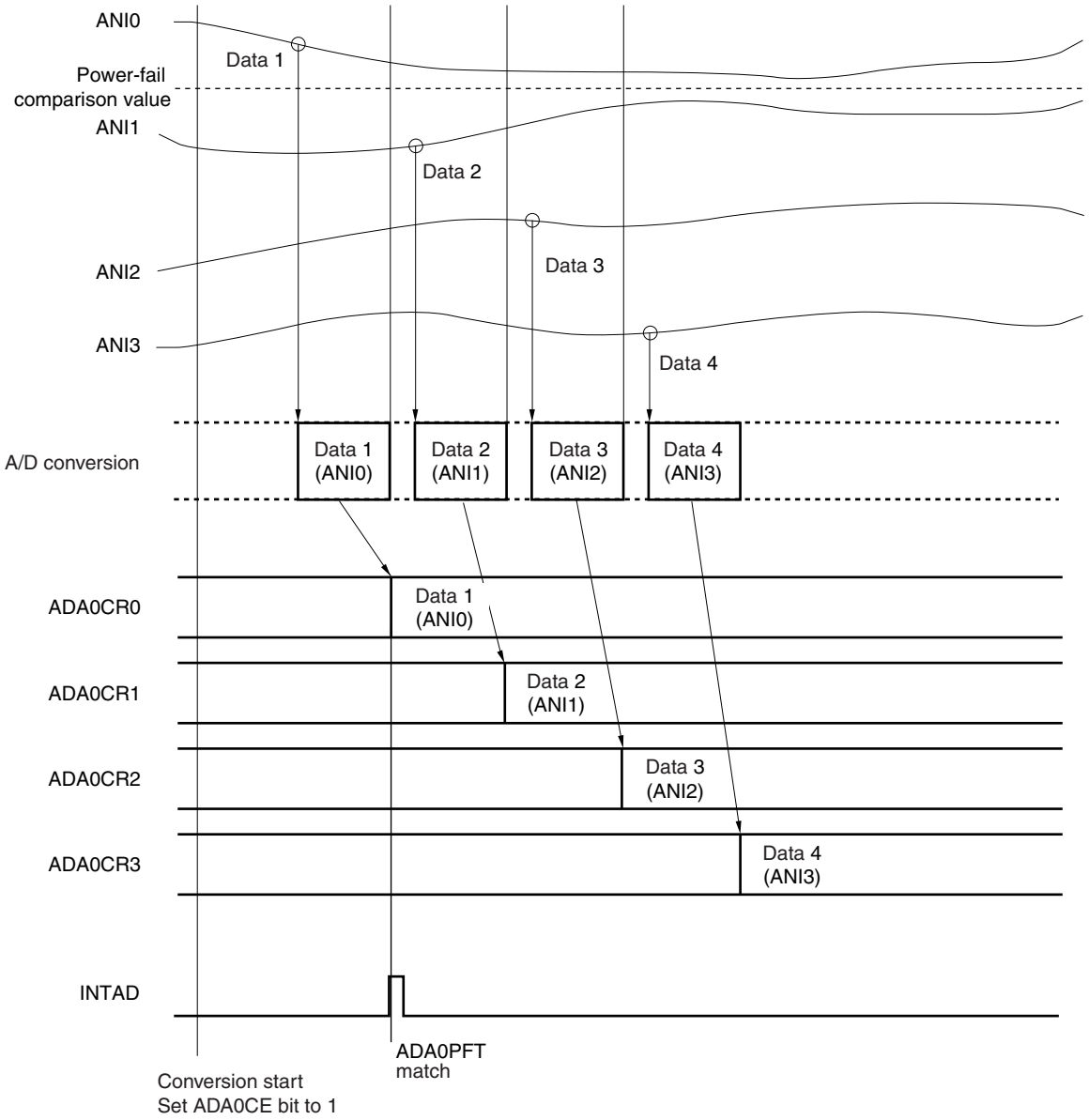


Figure 14-11. Example of Timing in One-Shot Scan Mode
(When Power-Fail Comparison Is Made: ADA0PFM.ADA0PFC bit = 0, ADA0S Register = 03H) (1/2)

(a) Timing example



Remark The above timing applies to the software trigger mode (ADA0M0.AD0TMD bit = 0) or the high-speed conversion mode (ADA0M1.ADA0HS1 bit = 1).

Table 17-6. Reception Error Causes

Error Flag	Reception Error	Cause
UC0PE	Parity error	The received parity bit does not match the setting.
UC0FE	Framing error	The stop bit was not detected.
UC0OVE	Overrun error	Reception of the next data was completed before data was read from the receive buffer.

When a reception error occurs, perform the following procedure according to the kind of error.

- Parity error
  If false data is received due to problems such as noise on the reception line, discard the received data and retransmit.

- Framing error
  A baud rate error may have occurred between the reception side and transmission side or a start bit may have been erroneously detected. Since this is a fatal error for the communication format, check that operation on the transmission side has stopped, initialize both sides, and then start the communication again.

- Overrun error
  1 frame of data is discarded because the next reception is completed before data was read from the receive buffer. If this data was needed, retransmit the data.

Caution In reception, be sure to read the UC0STR register before completion of the next reception to check whether an error has occurred. If an error has occurred, perform error processing.

(g) SET_CONFIGURATION() request

If any of wValue, wIndex, or wLength is other than the values shown in Table 20-3, a STALL response is made in the status stage.

- Default state: The CONF bit of the UF0 mode status register (UF0MODS) and the UF0 configuration register (UF0CNF) are set to 1 if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the CONF bit of the UF0MODS register and UF0CNF register are cleared to 0. In other words, the device skips the Addressed state and moves to the Configured state in which it responds to the Default address.
- Addressed state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device enters the Configured state if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the device remains in the Addressed state.
- Configured state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device returns to the Addressed state if the specified configuration value is 0 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 1, the device remains in the Configured state.

If the SET_CONFIGURATION() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) is set to 1, and an interrupt is issued. All Halt Features are cleared after the SET_CONFIGURATION() request has been completed even if the specified configuration value is the same as the current configuration value. If the SET_CONFIGURATION() request has been correctly processed, the data toggle of all endpoints is always initialized to DATA0 again (it is defined that the default status, Alternative Setting 0, is set from when the SET_CONFIGURATION request is received to when the SET_INTERFACE request is received).

(h) SET_FEATURE() request

A STALL response is made in the status stage if the SET_FEATURE() request is for a Feature that cannot be set or does not exist, or if the target is an interface or an endpoint that does not exist. A STALL response is also made if the wLength value is other than 0.

- Default state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Addressed state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Configured state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or an endpoint that exists; otherwise a STALL response is made in the status stage.

When the SET_FEATURE() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) and the EnHALT bit of the UF0 EPn status register L (UF0EnSL) are set to 1, and an interrupt is issued (n = 0 to 4, 7).

(23) UF0 INT clear 2 register (UF0IC2)

This register controls clearing the interrupt sources indicated by the UF0IS2 register.

This register is write-only, in 8-bit units. If this register is read, the value FFH is read.

FW can clear an interrupt source by writing 0 to the corresponding bit of this register. Even a bit that is automatically cleared to 0 by hardware can be cleared by FW before it is cleared by hardware. Writing 0 to a bit of this register automatically sets the bit to 1. Writing 1 is invalid.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 1, 3, 7) and the current setting of the interface.

	7	6	5	4	3	2	1	0	Address	After reset
UF0IC2	BKI2INC	BKI2 DTC	BKI1INC	BKI1 DTC	1	1	1	IT1DTC	00200040H	FFH

Bit position	Bit name	Function
7, 5	BKInINC	These bits clear the BLKInIN interrupt. 0: Clear
6, 4	BKInDTC	These bits clear the BLKInDT interrupt. 0: Clear
0	IT1DTC	These bits clear the INTnDT interrupt. 0: Clear

Remark n = 1, 2

(27) UF0 DMA status 0 register (UF0DMS0)

This register indicates the DMA status of Endpoint1 to Endpoint4.

This register is read-only, in 8-bit units.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 1 to 4) and the current setting of the interface.

	7	6	5	4	3	2	1	0	Address	After reset
UF0DMS0	0	0	DQE4	DQE3	DQE2	DQE1	0	0	0020004EH	00H

Bit position	Bit name	Function
5	DQE4	This bit indicates that a DMA read request is being issued from Endpoint4 to memory. 1: DMA read request from Endpoint4 is being issued. 0: DMA read request from Endpoint4 is not being issued (default value).
4	DQE3	This bit indicates that a DMA write request is being issued from memory to Endpoint3. Note that, even if data is in Endpoint3 (when the FIFO is not full and after the BKI2DED bit has been set to 1), the DMA request signal becomes active immediately and DMA transfer is started when the DQBI2MS bit of the UF0IDR register is set to 1. 1: DMA write request for Endpoint3 is being issued. 0: DMA write request for Endpoint3 is not being issued (default value).
3	DQE2	This bit indicates that a DMA read request is being issued from Endpoint2 to memory. 1: DMA read request from Endpoint2 is being issued. 0: DMA read request from Endpoint2 is not being issued (default value).
2	DQE1	This bit indicates that a DMA write request is being issued from memory to Endpoint1. Note that, even if data is in Endpoint1 (when the FIFO is not full and after the BKI1DED bit has been set to 1), the DMA request signal becomes active immediately and DMA transfer is started when the DQBI1MS bit of the UF0IDR register is set to 1. 1: DMA write request for Endpoint1 is being issued. 0: DMA write request for Endpoint1 is not being issued (default value).

Figure 20-10. Operation of UF0BI2 Register (2/3)

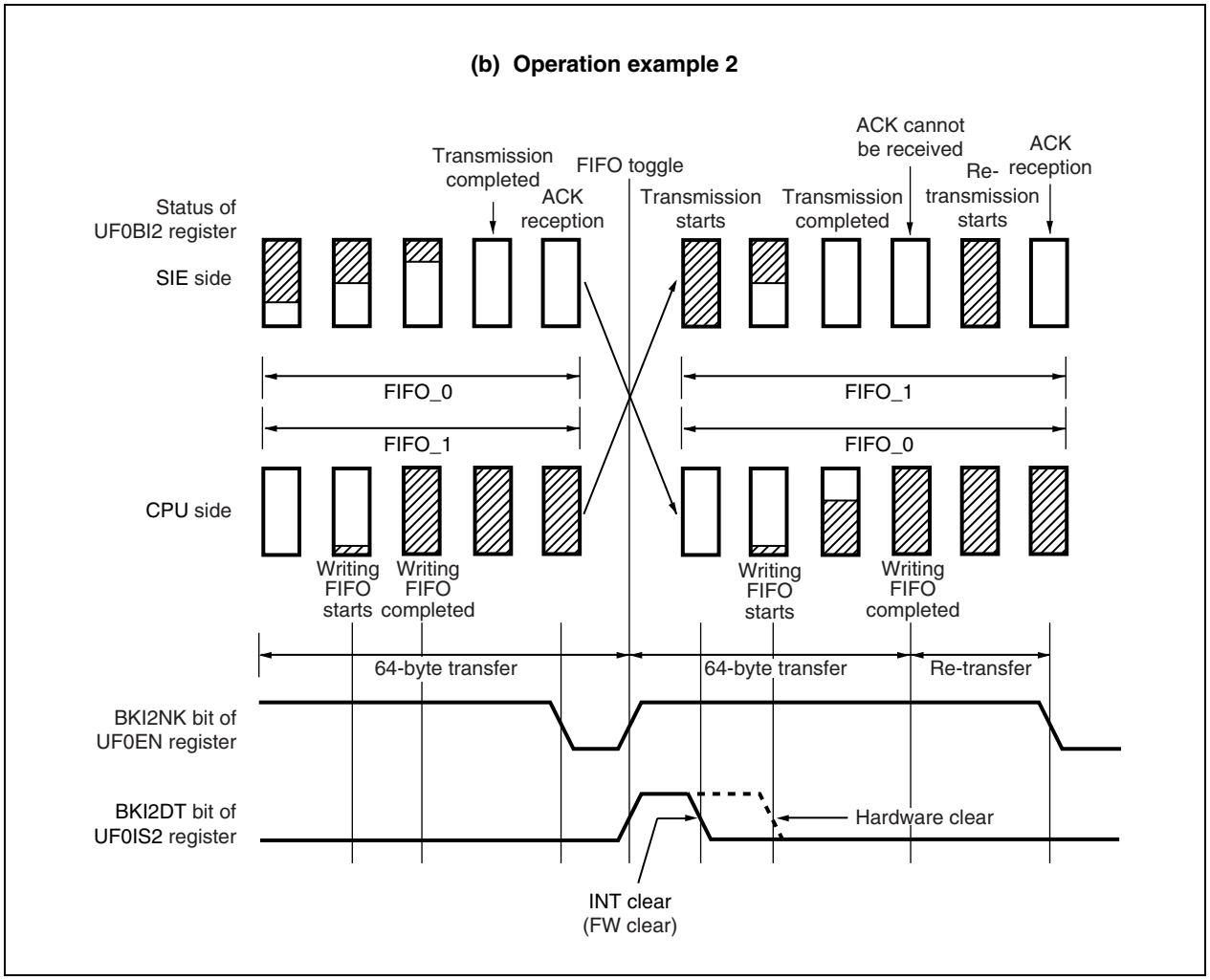
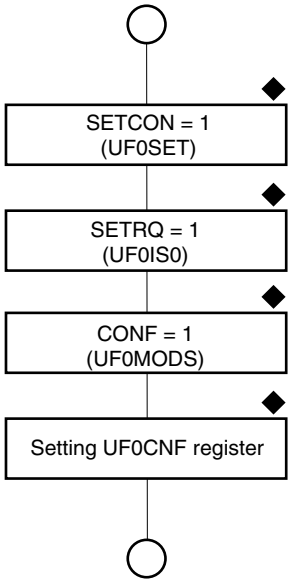
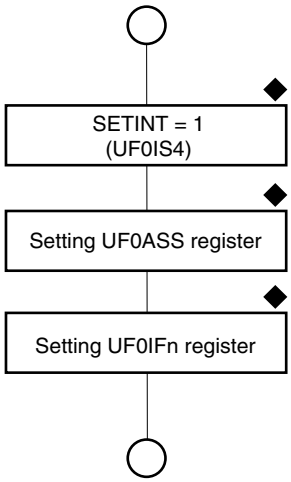


Figure 20-22. SET_CONFIGURATION Processing



Remark ♦: Processing by hardware

Figure 20-23. SET_INTERFACE Processing

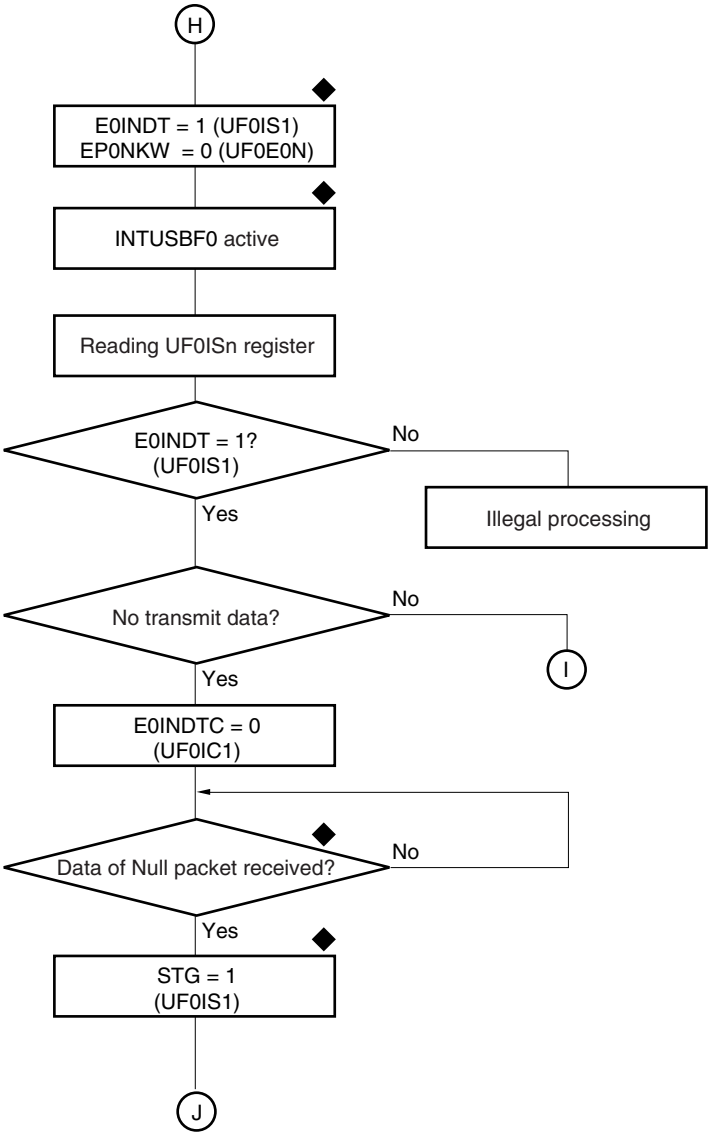


Remarks 1. n = 0 to 4

2. ♦: Processing by hardware

Figure 20-24. CPUDEC Request for Control Transfer (5/12)

(b) Control transfer (read) (3/4)



Remarks 1. n = 0, 1

2. ♦: Processing by hardware

CHAPTER 21 DMA FUNCTION (DMA CONTROLLER)

The V850ES/JG3-L includes a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer.

The DMAC controls data transfer between memory and I/Os, between memories, or between I/Os based on DMA requests issued by on-chip peripheral I/O (serial interfaces, timer/counters, and A/D converter), interrupts from external input pins, or software triggers (memory refers to internal RAM or external memory).

21.1 Features

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})
- Program execution using internal ROM during DMA transfer
- Transfer type: Two-cycle transfer
  - Data transfer between buses that have different bus widths
- Transfer mode: Single transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/Os (serial interfaces, timer/counters, A/D converter) or interrupts from external input pin
  - Requests triggered by software
- Transfer sources and destinations
  - Internal RAM ↔ On-chip peripheral I/O
  - On-chip peripheral I/O ↔ On-chip peripheral I/O
  - Internal RAM ↔ External memory
  - External memory ↔ On-chip peripheral I/O
  - External memory ↔ External memory

Table 31-6. Wiring of V850ES/JG3-L Flash Writing Adapters (FA-100GC-UEU-B) (1/2)

Flash Memory Programmer (FG-FP5) Connection Pin			Name of FA Board Pin	CSIB0 + HS Used		CSIB0 Used		UARTA0 Used	
Signal Name	I/O	Pin Function		Pin Name	Pin No. GC	Pin Name	Pin No. GC	Pin Name	Pin No. GC
SI/RxD	Input	Receive signal	SI	P41/SOB0/SCL01	23	P41/SOB0/SCL01	23	P30/TXDA0/SOB4	25
SO/TxD	Output	Transmit signal	SO	P40/SIB0/SDA01	22	P40/SIB0/SDA01	22	P31/RXDA0/INTP7/SIB4	26
SCK	Output	Transfer clock	SCK	P42/$\overline{SCKB0}$	24	P42/$\overline{SCKB0}$	24	Not needed	–
CLK	Output	Clock to V850ES/JG3-L	X1	Not needed	–	Not needed	–	Not needed	–
			X2	Not needed	–	Not needed	–	Not needed	–
/RESET	Output	Reset signal	/RESET	$\overline{RESET}$	14	$\overline{RESET}$	14	$\overline{RESET}$	14
FLMD0	Output	Write voltage	FLMD0	FLMD0	8	FLMD0	8	FLMD0	8
FLMD1	Output	Write voltage	FLMD1	PDL5/AD5/FLMD1	76	PDL5/AD5/FLMD1	76	PDL5/AD5/FLMD1	76
HS	Input	Handshake signal for CSI0 + HS communication	RESERVE/HS	PCM0/$\overline{WAIT}$	61	Not needed	–	Not needed	–
VDD	–	VDD voltage generation/voltage monitor	VDD	V_{DD}	9	V_{DD}	9	V_{DD}	9
				EV_{DD}	34, 70	EV_{DD}	34, 70	EV_{DD}	34, 70
				RV_{DD}	17	RV_{DD}	17	RV_{DD}	17
				UV_{DD}	30	UV_{DD}	30	UV_{DD}	30
				AV_{REF0}	1	AV_{REF0}	1	AV_{REF0}	1
				AV_{REF1}	5	AV_{REF1}	5	AV_{REF1}	5
GND	–	Ground	GND	V_{SS}	11	V_{SS}	11	V_{SS}	11
				AV_{SS}	2	AV_{SS}	2	AV_{SS}	2
				EV_{SS}	33, 69	EV_{SS}	33, 69	EV_{SS}	33, 69

Caution Be sure to connect the REGC pin to GND via a 4.7 μF (recommended value) capacitor.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

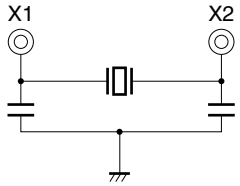
Figure 31-6. Wiring Example of V850ES/JG3-L Flash Writing Adapter (FA-100GC-UEU-B) (in CSIB0 + HS Mode) (2/2)

Notes 1. Corresponding pins when CSIB3 is used.

2. Wire the FLMD1 pin as shown below (recommended), or connect it to GND via a pull-down resistor on board.

3. Create an oscillator on the flash writing adapter (shown in broken lines) and supply a clock.
Here is an example of the oscillator.

Example:



4. Corresponding pins when UARTA0 is used.

Caution Do not input a high level to the $\overline{\text{DRST}}$ pin.

Remarks 1. The pins that are not used in flash memory programming remain in the same status as that immediately after a reset ends. Handle the pins not shown in accordance with the handling of unused pins (see **2.3 Pin I/O Circuit Types, I/O Buffer Power Supplies, and Connection of Unused Pins**).

2. This adapter is for a 100-pin plastic LQFP package.

Table 31-8. Relationship Between FLMD0 and FLMD1 Pins and Operation Mode Immediately After Reset Ends

FLMD0	FLMD1	Operation Mode
0	Don't care	Normal operation mode
V_{DD}	0	Flash memory programming mode
V_{DD}	V_{DD}	Setting prohibited

(3) Serial interface pin

The following shows the pins used by each serial interface.

Table 31-9. Pins Used by Serial Interfaces

Serial Interface	Pins Used
UARTA0	TXDA0, RXDA0
CSIB0	SOB0, SIB0, $\overline{\text{SCKB0}}$
CSIB3	SOB3, SIB3, $\overline{\text{SCKB3}}$
CSIB0 + HS	SOB0, SIB0, $\overline{\text{SCKB0}}$, PCM0
CSIB3 + HS	SOB3, SIB3, $\overline{\text{SCKB3}}$, PCM0

When connecting a dedicated flash memory programmer to a serial interface pin that is connected to another device on-board, care should be taken to avoid conflict of signals and malfunction of the other device.

(a) Conflict of signals

When the dedicated flash memory programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the other device or set the other device to the output high-impedance status.

Figure 31-12. Conflict of Signals (Serial Interface Input Pin)