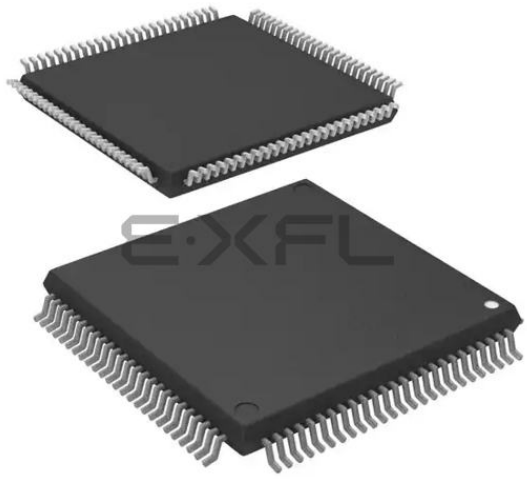
Renesas Electronics America Inc - UPD70F3795GC-UEU-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3795gc-ueu-ax

The mark <R> shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what: ” field.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

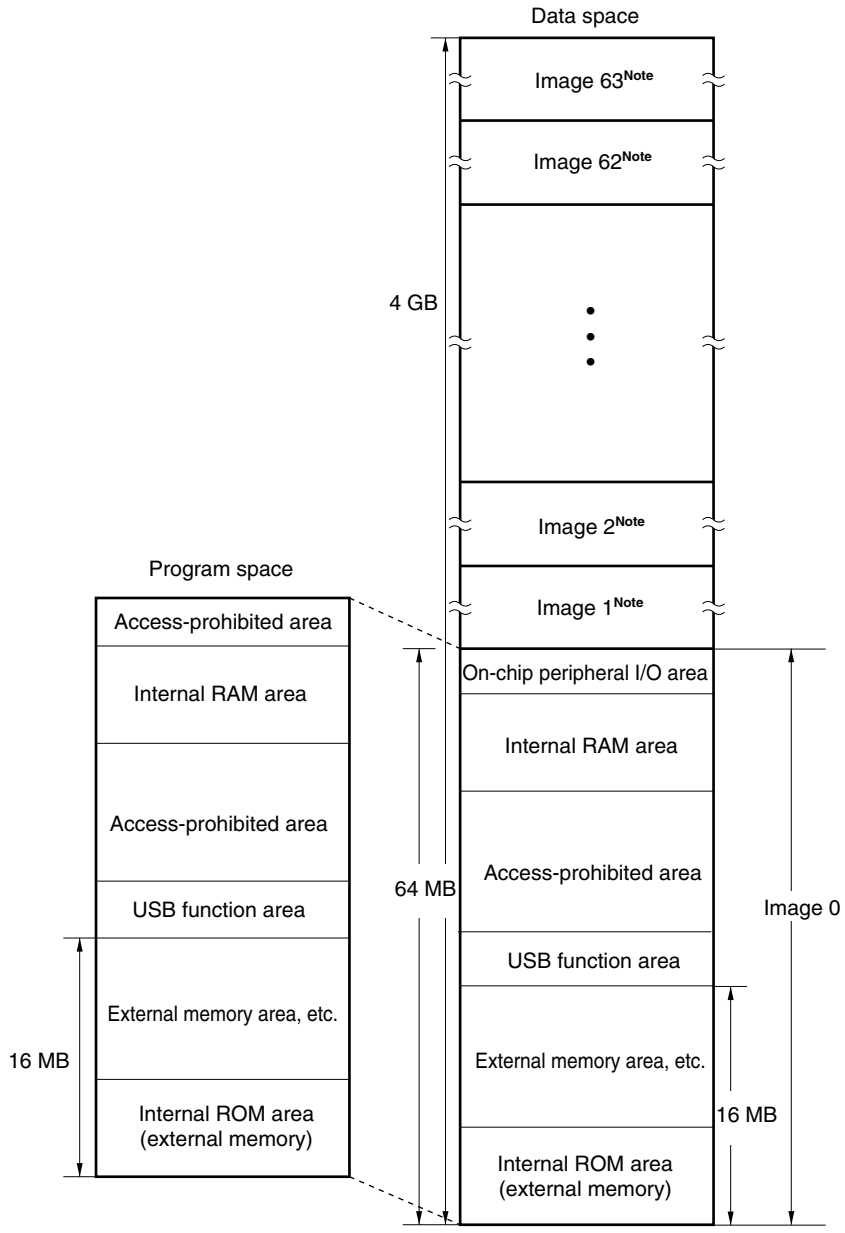
G (giga): $2^{30} = 1,024^3$

3.4 Address Space

3.4.1 CPU address space

For instruction addressing, up to a combined total of 16 MB of external memory area and internal ROM area, plus an internal RAM area, are supported in a linear address space (program space) of up to 64 MB. For operand addressing (data access), up to 4 GB of a linear address space (data space) is supported. The 4 GB address space, however, is viewed as 64 images of a 64 MB physical address space. This means that the same 64 MB physical address space is accessed regardless of the value of bits 31 to 26.

Figure 3-1. Address Space Image



Note Image 0 appears repeatedly for images 1 to 63.

(7) Port 0 function register (PF0)

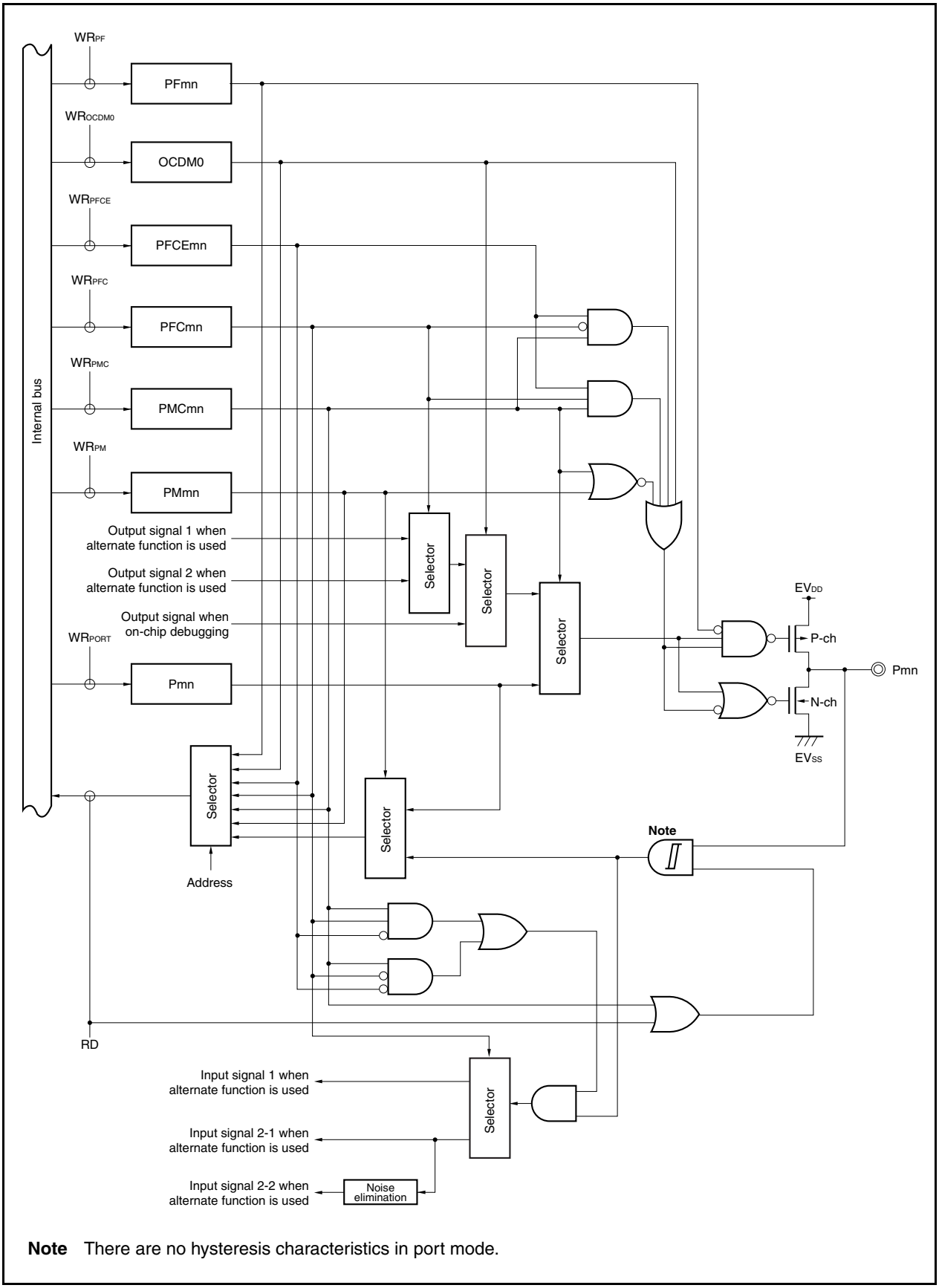
After reset: 00H R/W Address: FFFFFC60H

	7	6	5	4	3	2	1	0
PF0	0	PF06	PF05	PF04	PF03	PF02	0	0

PF0n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 2 to 6)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up to EV_{DD} or higher, be sure to set the PF0n bit to 1.

Figure 4-23. Block Diagram of Type U-7



Note There are no hysteresis characteristics in port mode.

(7) TMPn capture/compare register 0 (TPnCCR0)

The TPnCCR0 register can be used as a capture register or a compare register depending on the mode.

This register can be selected as a capture register or a compare register only in the free-running timer mode, according to the setting of the TPnOPT0.TPnCCS0 bit. In the pulse width measurement mode, the TPnCCR0 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TPnCCR0 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TPnCCR0 register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing special on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R/W Address: TP0CCR0 FFFFF596H, TP1CCR0 FFFFF5A6H, TP2CCR0 FFFFF5B6H, TP3CCR0 FFFFF5C6H, TP4CCR0 FFFFF5D6H, TP5CCR0 FFFFF5E6H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPnCCR0																

(n = 0 to 5)

(2) Using one-shot pulse mode

(a) Rewriting the TPnCCRa register

When rewriting the value of the TPnCCRa register to a smaller value, stop counting first and then change the set value.

When changing the value of the TPnCCR0 register from D_{00} to D_{01} and the value of the TPnCCR1 register from D_{10} to D_{11}, if the registers are rewritten under any of the following conditions, a one-shot pulse will not be output as expected.

Condition 1 When rewriting the TPnCCR0 register, if:

$D_{00} > D_{01}$ or,

D_{00} < 16-bit counter value < D_{01}

In the case of condition 1, the 16-bit counter will not be cleared and will overflow in the cycle in which the new value is being written. The counter will be cleared for the first time at the newly written value (D_{01}).

Condition 2 When rewriting the TPnCCR1 register, if:

$D_{10} > D_{11}$ or,

D_{10} < 16-bit counter value < D_{11}

In the case of condition 2, the TOPn1 pin output cannot be inverted to the active level in the cycle in which the new value is being written.

An example of what happens when condition 1 and condition 2 are satisfied in the same cycle is shown in Figure 7-42.

The 16-bit counter increments up to FFFFH, overflows, and starts incrementing again from 0000H.

When the 16-bit counter value matches D_{11}, the INTTPnCC1 signal is generated and the TOPn1 pin output is set to the active level. Subsequently, when the 16-bit counter value matches D_{01}, the INTTPnCC0 signal is generated, the TOPn1 pin output is set to the inactive level, and the counter stops incrementing.

8.4 Operations

TMQ0 can execute the following operations:

Table 8-7. TMQ0 Operating Modes

Operating Mode	TQ0CTL1.TQ0EST Bit (Software Trigger Bit)	TIQ00 Pin (External Trigger Input)	Capture/Compare Register Setting	Compare Register Write	Count Clock
Interval timer mode	Invalid	Invalid	Compare only	Anytime write	Internal/external
External event count mode[Note 1]	Invalid	Invalid	Compare only	Anytime write	External
External trigger pulse output mode[Note 2]	Valid	Valid	Compare only	Batch write	Internal
One-shot pulse output mode[Note 2]	Valid	Valid	Compare only	Anytime write	Internal
PWM output mode	Invalid	Invalid	Compare only	Batch write	Internal/external
Free-running timer mode	Invalid	Invalid	Can be switched	Anytime write	Internal/external
Pulse width measurement mode[Note 2]	Invalid	Invalid	Capture only	Not applicable	Internal

Notes 1. When using the external event count mode, specify that the valid edge of the TIQ00 pin capture trigger input is not detected (by clearing the TQ0IOC1.TQ0IS1 and TQ0IOC1.TQ0IS0 bits to 0).

2. When using the external trigger pulse output mode, one-shot pulse output mode, and pulse width measurement mode, select the internal clock as the count clock (by clearing the TQ0CTL1.TQ0EEE bit to 0).

8.4.3 External trigger pulse output mode (TQ0MD2 to TQ0MD0 bits = 010)

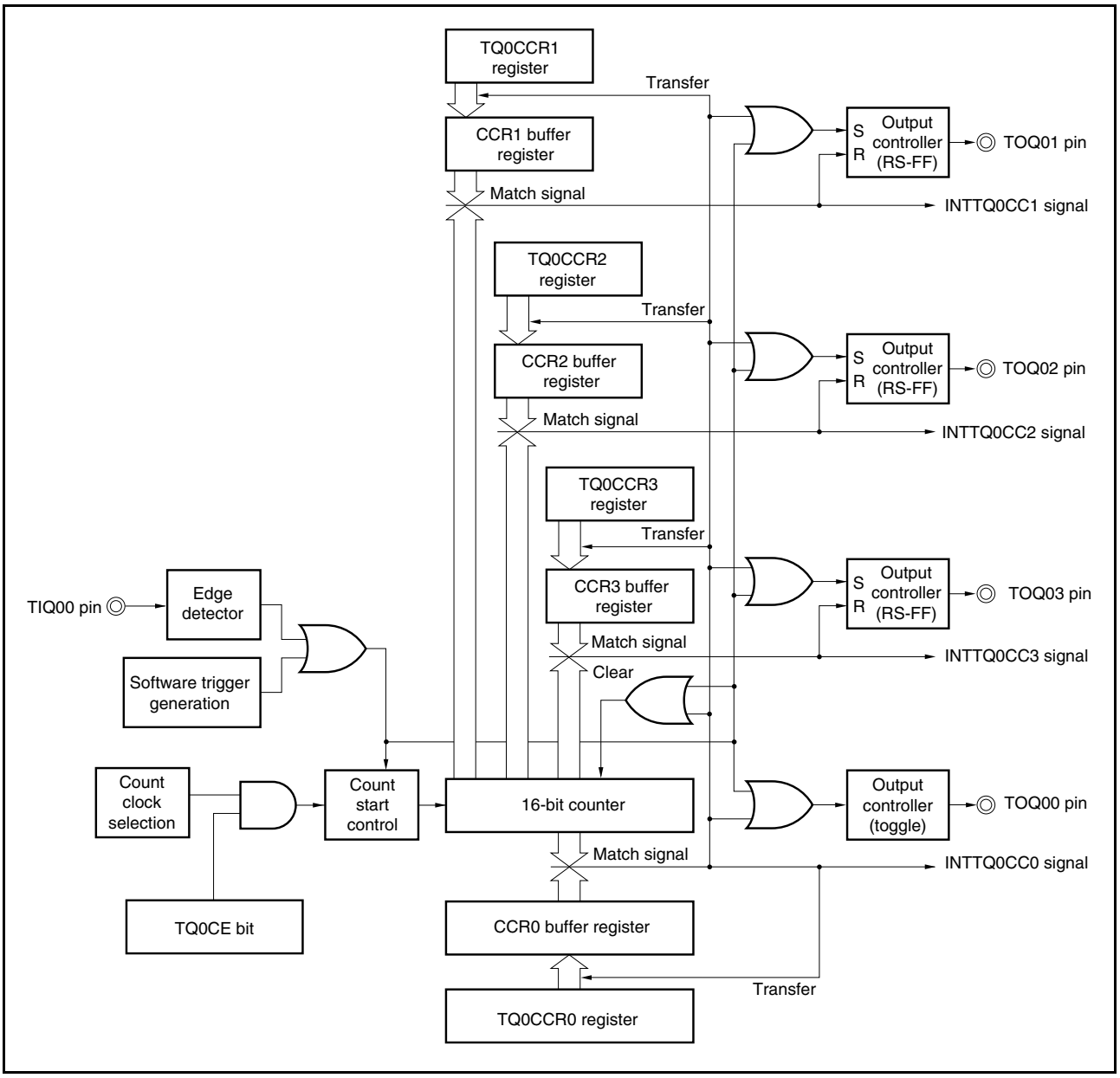
In the external trigger pulse output mode, when the TQ0CTL0.TQ0CE bit is set to 1, TMQ0 waits for a trigger, which is the valid edge of the external trigger input signal, and starts incrementing when this trigger is detected. TMQ0 then outputs a PWM waveform from the TOQ01 to TOQ03 pins.

Pulses can also be output by generating a software trigger instead of using the external trigger. When using a software trigger instead of the external trigger, a square wave that has one cycle of the PWM waveform as half its cycle can also be output from the TOQ00 pin.

Remarks 1. For how to set the TIQ00 and TOQ00 to TOQ03 pins, see **Table 8-2 Pins Used by TMQ0** and **Table 4-15 Settings When Pins Are Used for Alternate Functions**.

2. For how to enable the INTTQ0CC0 to INTTQ0CC3 interrupt signals, see **CHAPTER 22 INTERRUPT SERVICING/EXCEPTION PROCESSING FUNCTION**.

Figure 8-26. Configuration of TMQ0 in External Trigger Pulse Output Mode



(1) Operations in one-shot pulse output mode

Figure 8-41. Timing and Processing of Operations in One-Shot Pulse Output Mode (1/2)

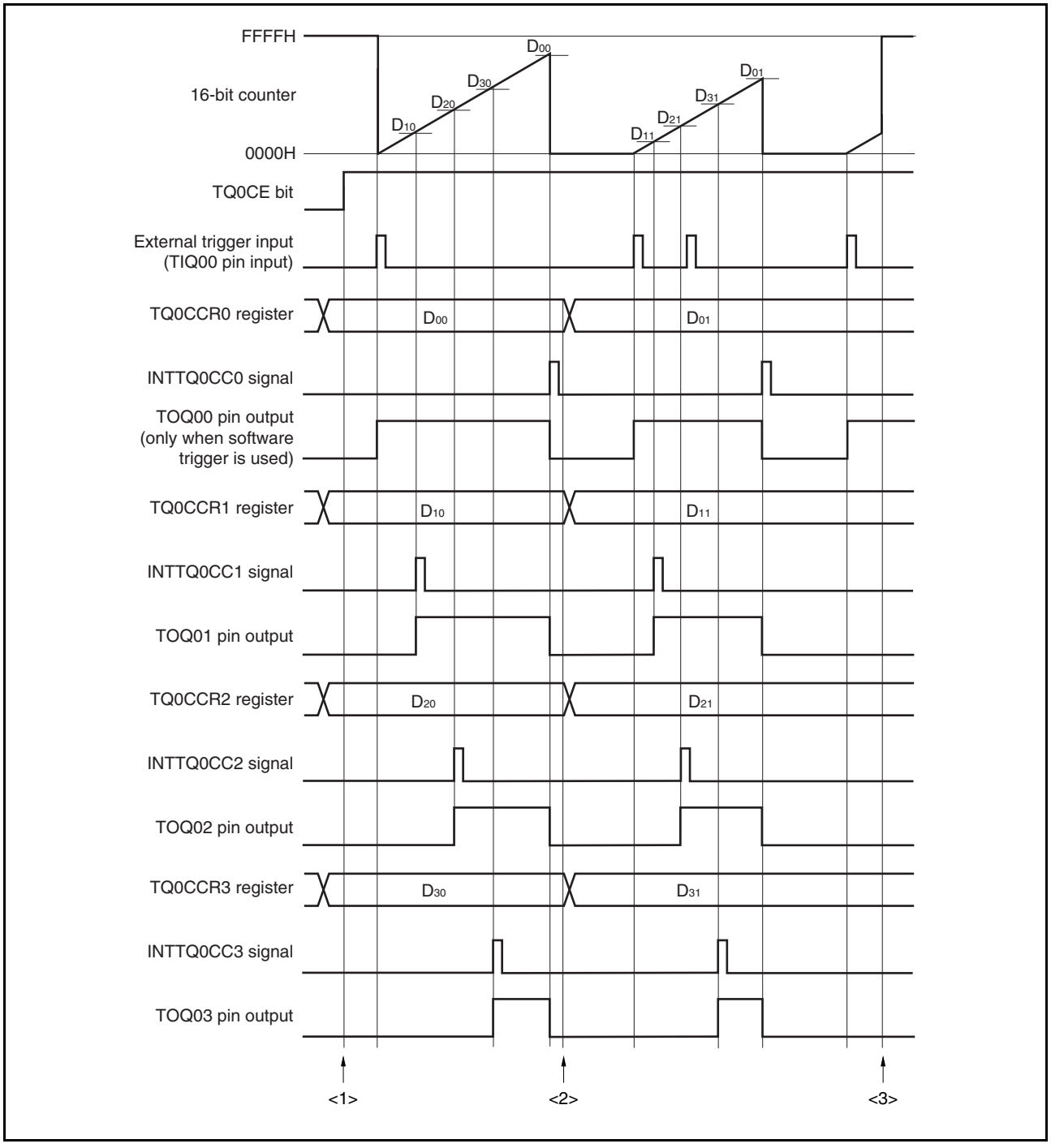


Figure 8-46. Register Settings in PWM Output Mode (2/3)

(c) TMQ0 I/O control register 0 (TQ0IOC0)

	TQ0OL3	TQ0OE3	TQ0OL2	TQ0OE2	TQ0OL1	TQ0OE1	TQ0OL0	TQ0OE0
TQ0IOC0	0/1	0/1	0/1	0/1	0/1	0/1	0/1 Note	0/1 Note

0: Disable TOQ00 pin output.
1: Enable TOQ00 pin output.

Output level when TOQ00 pin is disabled:
0: Low level
1: High level

0: Disable TOQ01 pin output.
1: Enable TOQ01 pin output.

Active level of TOQ01 pin output:
0: High level
1: Low level

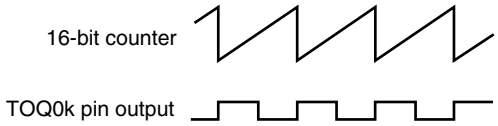
0: Disable TOQ02 pin output.
1: Enable TOQ02 pin output.

Active level of TOQ02 pin output:
0: High level
1: Low level

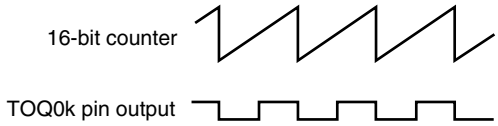
0: Disable TOQ03 pin output.
1: Enable TOQ03 pin output.

Active level of TOQ03 pin output:
0: High level
1: Low level

- When TQ0OLk bit is 0:



- When TQ0OLk bit is 1:



(d) TMQ0 I/O control register 2 (TQ0IOC2)

					TQ0EES1	TQ0EES0	TQ0ETS1	TQ0ETS0
TQ0IOC2	0	0	0	0	0/1	0/1	0	0

These bits select the valid edge of the external trigger input.

(e) TMQ0 counter read buffer register (TQ0CNT)

The value of the 16-bit counter can be read by reading this register.

Note Set this bit to 0 when not using the TOQ00 pin in the PWM output mode.

(7) Minute count register (RC1MIN)

The RC1MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (2 × 32.768 kHz) later. Set a decimal value of 00 to 59 to this register in BCD code.

This register can be read or written 8-bit units.

Caution Setting a value other than 00 to 59 to the RC1MIN register is prohibited.

Remark See **11.4.1 Initial settings**, **11.4.2 Rewriting each counter during real-time counter operation**, and **11.4.3 Reading each counter during real-time counter operation** when reading or writing the RC1MIN register.

After reset: **Note** R/W Address: FFFFFAD3H

	7	6	5	4	3	2	1	0
RC1MIN	0							

Note RV_{DD} power-on reset : 00H
Other kind of reset : Previous value retained

(8) Hour count register (RC1HOUR)

The RC1HOUR register is an 8-bit register that takes a value of 0 to 23 or 1 to 12 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (2 × 32.768 kHz) later. Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

This register can be read or written 8-bit units.

However, the value of this register is 00H if the AMPM bit is set to 1 after apply power to RV_{DD} power-on reset**.**

Cautions 1. Bit 5 of the RC1HOUR register indicates a.m. (0) or p.m. (1) if AMPM = 0 (if the 12-hour system is selected).

2. Setting a value other than 01 to 12, 21 to 32 (AMPM bit= 0), or 00 to 23 (AMPM bit = 1) to the RC1HOUR register is prohibited.

Remark See **11.4.1 Initial settings**, **11.4.2 Rewriting each counter during real-time counter operation**, and **11.4.3 Reading each counter during real-time counter operation** when reading or writing the RC1HOUR register.

After reset: **Note** R/W Address: FFFFFAD4H

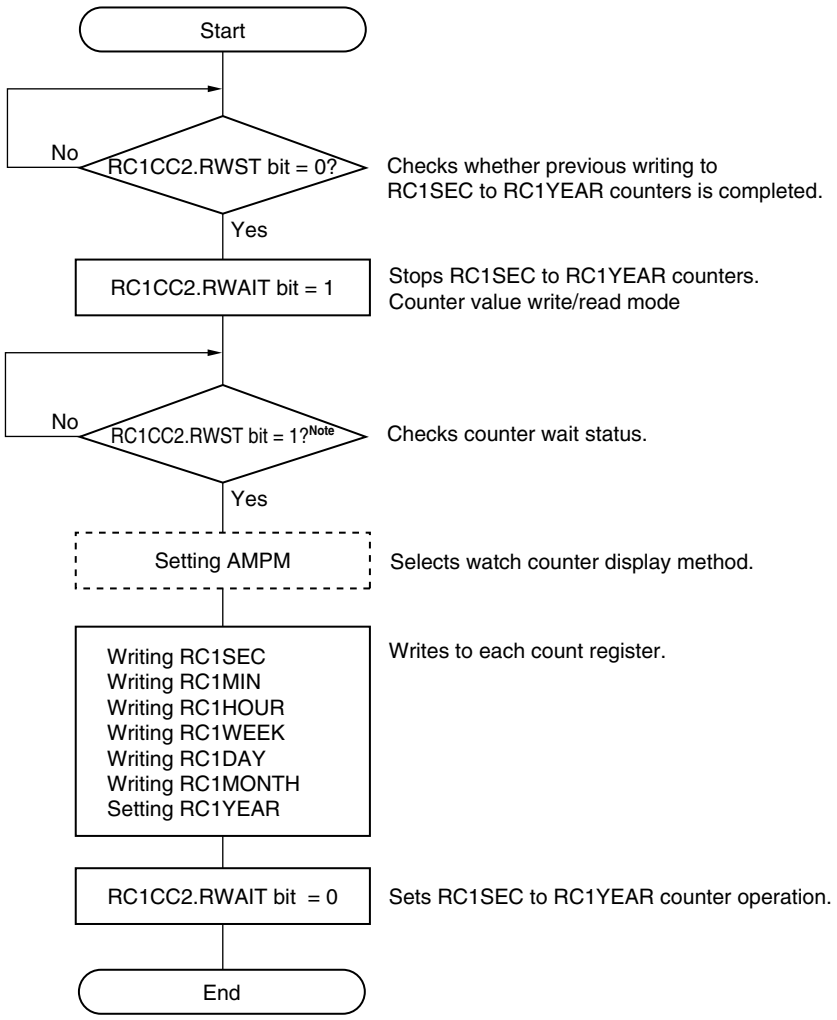
	7	6	5	4	3	2	1	0
RC1HOUR	0	0						

Note RV_{DD} power-on reset : 12H
Other kind of reset : Previous value retained

11.4.2 Rewriting each counter during real-time counter operation

Set as follows when rewriting each counter (RC1SEC, RC1MIN, RC1HOUR, RC1WEEK, RC1DAY, RC1MONTH, RC1YEAR) during real-time counter operation (RC1PWR = 1, RTCE = 1).

Figure 11-3. Rewriting Each Counter During Real-time Counter Operation



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations for setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.
If RWAIT = 1 is set, the operation of RC1SEC to RC1YEAR is stopped. If a carry occurs from RC1SUBC while RWAIT = 1, one carry can be internally retained. However, if two or more carries occur, the number of carries cannot be retained.

Remark RC1SEC, RC1MIN, RC1HOUR, RC1WEEK, RC1DAY, RC1MONTH, and RC1YEAR may berewrite in any sequence.
All the registers do not have to be set and only some registers may be read.

(13) A/D conversion result hysteresis characteristics

The successive comparison type A/D converter holds the analog input voltage in the internal sample & hold capacitor and then performs A/D conversion. After A/D conversion has finished, the analog input voltage remains in the internal sample & hold capacitor. As a result, the following phenomena may occur.

- When the same channel is used for A/D conversions, if the voltage is higher or lower than the previous A/D conversion, then hysteresis characteristics may appear where the conversion result is affected by the previous value. Thus, even if the conversion is performed at the same potential, the result may vary.
- When switching the analog input channel, hysteresis characteristics may appear where the conversion result is affected by the previous channel value. This is because one A/D converter is used for the A/D conversions. Thus, even if the conversion is performed at the same potential, the result may vary.

Therefore, to obtain a more accurate conversion result, perform A/D conversion twice successively for the same channel, and discard the first conversion result.

(2) UARTAn control register 1 (UAnCTL1)

The UAnCTL1 register is an 8-bit register that selects the UARTAn base clock.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

Caution Clear the UAnCTL0.UAnPWR bit to 0 before rewriting the UAnCTL1 register.

After reset: 00H R/W Address: UA0CTL1 FFFFFA01H, UA1CTL1 FFFFFA11H, UA2CTL1 FFFFFA21H, UA3CTL1 FFFFFA31H, UA4CTL1 FFFFFA41H, UA5CTL1 FFFFFA51H

UAnCTL1 (n = 0 to 5)

7	6	5	4	3	2	1	0
0	0	0	0	UAnCKS3	UAnCKS2	UAnCKS1	UAnCKS0

UAnCKS3	UAnCKS2	UAnCKS1	UAnCKS0	Base clock (f_{UCLK}) selection
0	0	0	0	fxx
0	0	0	1	fxx/2
0	0	1	0	fxx/4
0	0	1	1	fxx/8
0	1	0	0	fxx/16
0	1	0	1	fxx/32
0	1	1	0	fxx/64
0	1	1	1	fxx/128
1	0	0	0	fxx/256
1	0	0	1	fxx/512
1	0	1	0	fxx/1,024
1	0	1	1	External clock[Note] (ASCKA0 pin)
Other than above				Setting prohibited

Note Only UARTA0 is valid; setting UARTA1 to UARTA5 are prohibited.

Remark fxx: Main clock frequency

19.6.7 Wait state cancellation method

In the case of I²C0n, a wait state can be canceled normally in the following ways (n = 0 to 2).

- By writing data to the IICn register
- By setting the IICCn.WRELn bit to 1 (wait state cancellation)
- By setting the IICCn.STTn bit to 1 (start condition generation)
- By setting the IICCn.SPTn bit to 1 (stop condition generation)

If any of these wait state cancellation actions is performed, I²C0n will cancel the wait state and restart communication.

When canceling the wait state and sending data (including addresses), write data to the IICn register.

To receive data after canceling the wait state, or to complete data transmission, set the WRELn bit to 1.

To generate a restart condition after canceling the wait state, set the STTn bit to 1.

To generate a stop condition after canceling the wait state, set the SPTn bit to 1.

Cancel each wait state only once.

For example, if data is written to the IICn register following wait state cancellation by setting the WRELn bit to 1, a conflict between the SDA0n line change timing and the IICn register write timing may result in the data output to the SDA0n line being incorrect.

Even in other operations, if communication is stopped halfway, clearing the IICCn.IICEn bit to 0 will stop communication, enabling the wait state to be cancelled.

If the I²C bus deadlocks due to noise, etc., setting the IICCn.LRELn bit to 1 causes the communication to stop, enabling the wait state to be cancelled.

(12) UF0 INT status 1 register (UF0IS1)

This register indicates the interrupt source. If the contents of this register are changed, the EPCINT0B signal becomes active.

This register is read-only, in 8-bit units.

If an interrupt request (INTUSBF0) is generated from USBF, the FW must read this register to identify the interrupt source.

Each bit of this register is forcibly cleared to 0 when 0 is written to the corresponding bit of the UF0IC1 register. However, the SUCES and STG bits of the UF0IS1 register are automatically cleared to 0 when the next SETUP token has been received.

Caution In the USBF, multiple interrupt sources, such as Bus Reset, Resume, and Short, are ORed internally and are issued as a single interrupt request (INTUSBF0). Therefore, in the case of the occurrence of multiple interrupt sources, they are ORed and issued as an INTUSBF0 interrupt request.

For example, if a Bus Reset interrupt source and Resume interrupt source occur, the two sources are ORed and an INTUSBF0 interrupt request is issued.

Under these conditions, if the Bus Reset interrupt source is cleared to 0 (UF0IC0.BUSRSTC = 0), the V850ES/JG3-L internal INTUSBF0 interrupt request may remain set to 1 since the Resume interrupt source will still be remaining. The new interrupt request flag (US0BIC.US0BIF), therefore, might not be set to 1.

In this case, after performing clear processing for each interrupt request with the INTUSBF0 interrupt servicing routine, confirm the flag status for the UF0IS0 and UF0IS1 registers again, and if there are any interrupt sources with flags set to 1, perform flag clearing (only the applicable bits need to be cleared (do not perform a batch clearing)).

	7	6	5	4	3	2	1	0	Address	After reset
UF0IS1	0	E0IN	E0INDT	E0ODT	SUCES	STG	PROT	CPU DEC	00200022H	00H

Bit position	Bit name	Function
6	E0IN	This bit indicates that an IN token for Endpoint0 has been received and that the hardware has automatically transmitted NAK. 1: IN token is received and NAK is transmitted (interrupt request is generated). 0: IN token is not received (default value).
5	E0INDT	This bit indicates that data has been correctly transmitted from the UF0E0W register. 1: Transmission from UF0E0W register is completed (interrupt request is generated). 0: Transmission from UF0E0W register is not completed (default value). Data is transmitted in synchronization with the IN token next to the one that set the EP0NKW bit of the UF0E0N register to 1. This bit is automatically set to 1 by hardware when the host correctly receives that data. It is also set to 1 even if the data is a Null packet. This bit is automatically cleared to 0 by hardware when the first write access is made to the UF0E0W register.

(40) UF0 endpoint 3 interface mapping register (UF0E3IM)

This register specifies for which Interface and Alternative Setting Endpoint3 is valid.

This register can be read or written in 8-bit units.

The setting of this register and the Alternative Setting selected by the SET_INTERFACE request indicate whether Endpoint3 is currently valid, and the hardware determines how the GET_STATUS/CLEAR_FEATURE/SET_FEATURE Endpoint3 request and the IN transaction to Endpoint3 are responded to, and whether the related bits are valid or invalid.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E3IM	E3EN2	E3EN1	E3EN0	E32AL1	E35AL4	E35AL3	E35AL2	E35AL1	0020008AH	00H

Bit position	Bit name	Function
7 to 5	E3EN2 to E3EN0	These bits set a link between the Interface of Endpoint3 and the two-/five-series Alternative Setting. The endpoint is linked with Alternative Setting 0. The endpoint linked with Alternative Setting 0 cannot be excluded from Alternative Setting 1 to 4.

E3EN2	E3EN1	E3EN0	Link status
1	1	1	Not linked with Interface
1	1	0	
1	0	1	Linked with Interface 4 and Alternative Setting 0
1	0	0	Linked with Interface 3 and Alternative Setting 0
0	1	1	Linked with Interface 2 and Alternative Setting 0
0	1	0	Linked with Interface 1 and Alternative Setting 0
0	0	1	Linked with Interface 0 and Alternative Setting 0
0	0	0	Not linked with Interface (default value)

When these bits are set to 110 or 111, they are invalid even if the E32AL1 bit is cleared to 0.

If the endpoint is linked, setting of the CONF bit of the UF0MODS register to 1 indicates that Endpoint3 is valid.

4	E32AL1	This bit validates Endpoint3 when the two-series Alternative Setting and the Alternative Setting of the linked Interface are set to 1. 1: Validate the endpoint when Alternative Setting 1 is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting 1 is set with CONF bit = 1 (default value). This bit is valid when the E35AL4 to E35AL1 bits are 0000.
3 to 0	E35ALn	These bits validate Endpoint3 when the five-series Alternative Setting and the Alternative Setting of the linked Interface are set to n. 1: Validate the endpoint when Alternative Setting n is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting n is set with CONF bit = 1 (default value).

Remark n = 1 to 4

CHAPTER 27 LOW-VOLTAGE DETECTOR (LVI)

27.1 Functions

The low-voltage detector (LVI) has the following functions.

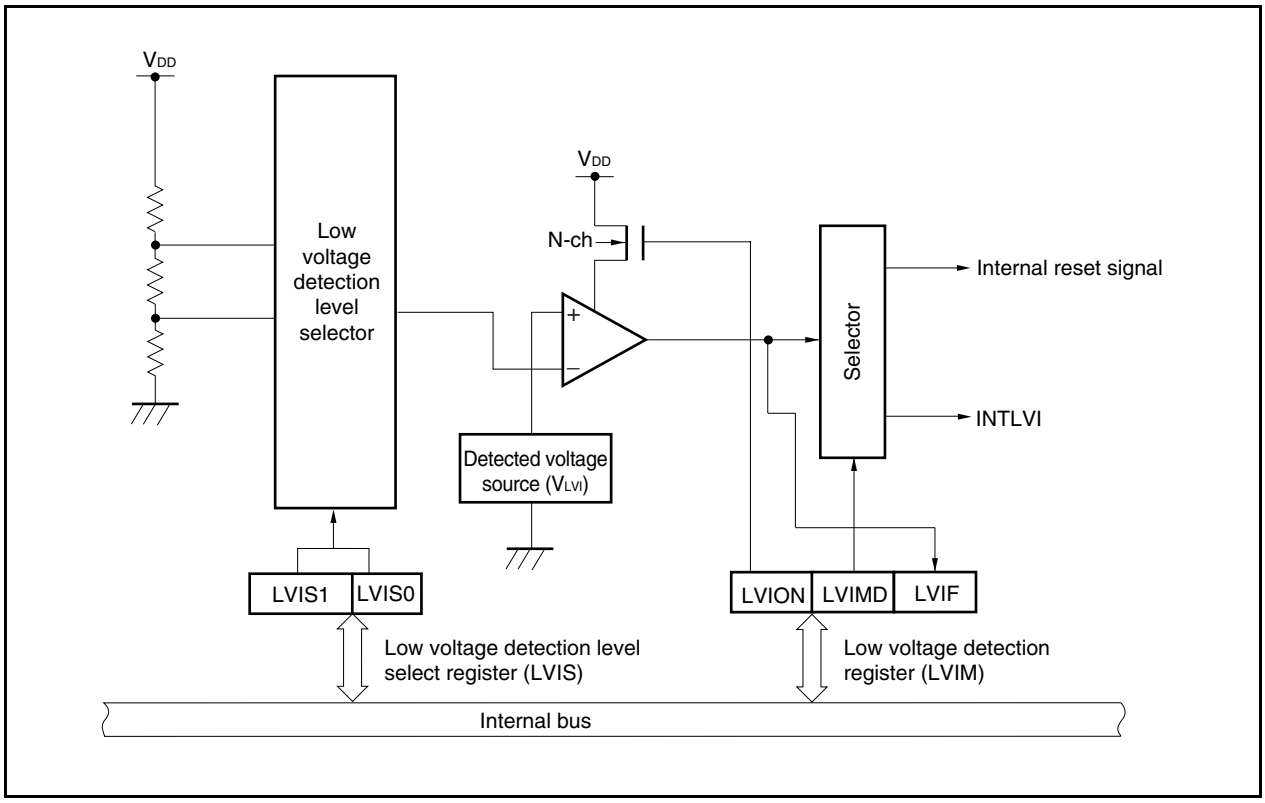
- If interrupt occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector compares the supply voltage (V_{DD}) and the detection voltage (V_{LVI}), and generates an internal interrupt signal when the supply voltage drops below or rises above the detection voltage.
- If reset occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector generates an internal reset signal when the supply voltage (V_{DD}) drops below the detection voltage (V_{LVI}).
- The level of the supply voltage to be detected can be changed by software.
- Interrupt or reset signal can be selected by software.
- The low-voltage detector is operable in the standby mode.

If a reset occurs when the low-voltage detector is selected to generate a reset signal, the RESF.LVIRF bit is set to 1. For details about the RESF register, see **25.3 Register to Check Reset Source**.

27.2 Configuration

The block diagram of the low-voltage detector is shown below.

Figure 27-1. Block Diagram of Low-Voltage Detector

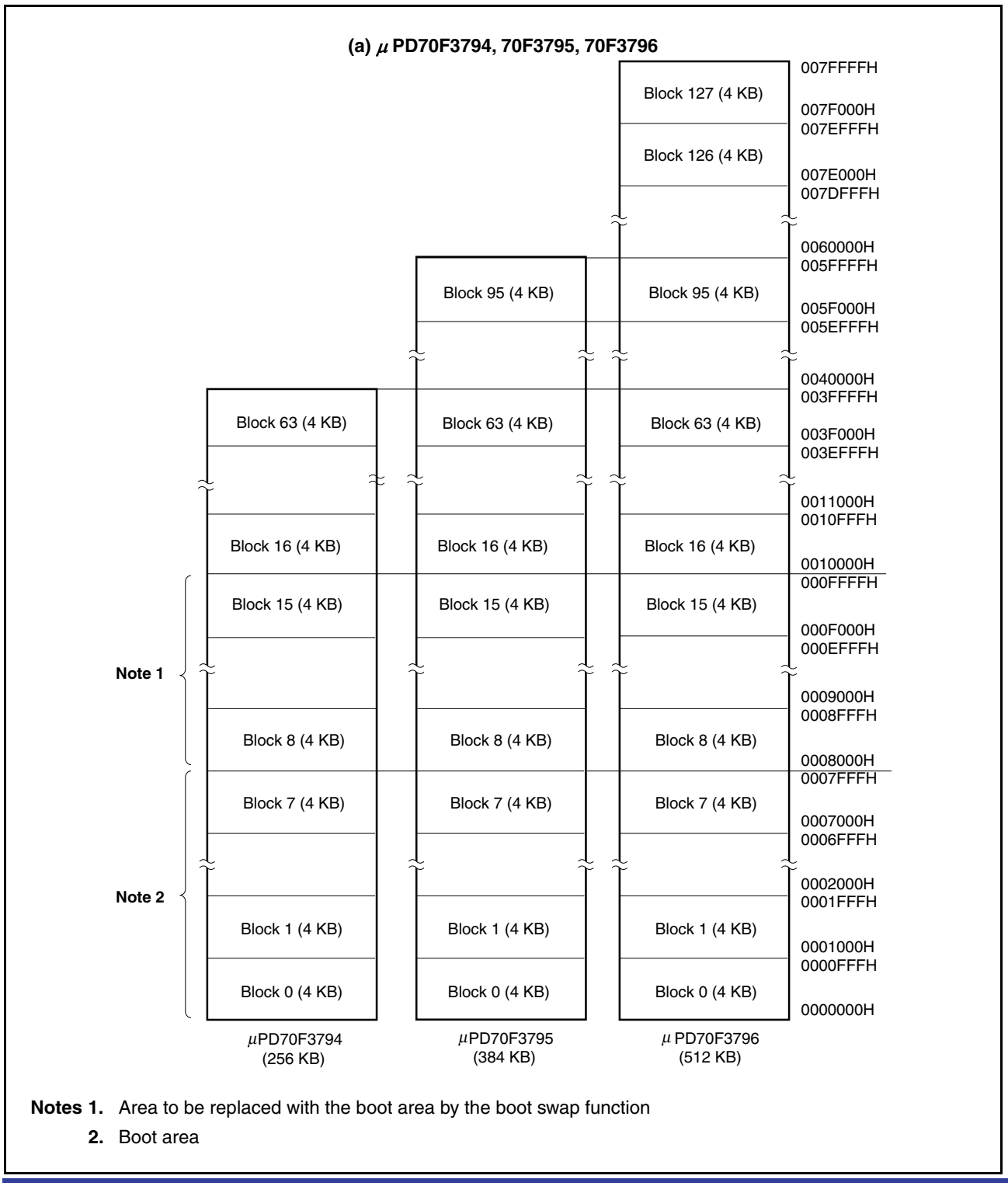


31.2 Memory Configuration

The V850ES/JG3-L internal flash memory area is divided into 64 or 96 or 128 blocks and can be erased in block units. All the blocks can also be erased at once.

When the boot swap function is used, the physical memory located at the addresses of blocks 0 to 7 is replaced by the physical memory located at the addresses of blocks 8 to 15. For details of the boot swap function, see **31.5 Rewriting by Self Programming**.

Figure 31-1. Flash Memory Mapping



Notes 1. Area to be replaced with the boot area by the boot swap function

2. Boot area

(11/19)

Symbol	Name	Unit	Page
UA3TX	UARTA3 transmit data register	UARTA	553
UA4CTL0	UARTA4 control register 0	UARTA	547
UA4CTL1	UARTA4 control register 1	UARTA	571
UA4CTL2	UARTA4 control register 2	UARTA	572
UA4OPT0	UARTA4 option control register 0	UARTA	549
UA4RIC	Interrupt control register	INTC	979
UA4RX	UARTA4 receive data register	UARTA	553
UA4STR	UARTA4 status register	UARTA	551
UA4TIC	Interrupt control register	INTC	979
UA4TX	UARTA4 transmit data register	UARTA	553
UA5CTL0	UARTA5 control register 0	UARTA	547
UA5CTL1	UARTA5 control register 1	UARTA	571
UA5CTL2	UARTA5 control register 2	UARTA	572
UA5OPT0	UARTA5 option control register 0	UARTA	549
UA5RIC	Interrupt control register	INTC	979
UA5RX	UARTA5 receive data register	UARTA	553
UA5STR	UARTA5 status register	UARTA	551
UA5TIC	Interrupt control register	INTC	979
UA5TX	UARTA5 transmit data register	UARTA	553
UC0CTL0	UARTC0 control register 0	UARTC	584
UC0CTL1	UARTC0 control register 1	UARTC	610
UC0CTL2	UARTC0 control register 2	UARTC	611
UC0OPT0	UARTC0 option control register 0	UARTC	586
UC0OPT1	UARTC0 option control register 1	UARTC	588
UC0RIC	Interrupt control register	INTC	979
UC0RX	UARTC0 receive data register	UARTC	591
UC0RXL	UARTC0 receive data register L	UARTC	591
UC0STR	UARTC0 status register	UARTC	590
UC0TIC	Interrupt control register	INTC	979
UC0TX	UARTC0 transmit data register	UARTC	592
UC0TXL	UARTC0 transmit data register L	UARTC	592
UCKSEL	USB clock select register	USBF	764
UF0AAS	UF0 active alternative setting register	USBF	826
UF0ADRS	UF0 address register	USBF	863
UF0AIFN	UF0 active interface number register	USBF	825
UF0ASS	UF0 alternative setting status register	USBF	827
UF0BI1	UF0 bulk-in 1 register	USBF	846
UF0BI2	UF0 bulk-in 2 register	USBF	850
UF0BO1	UF0 bulk-out 1 register	USBF	839
UF0BO1L	UF0 bulk-out 1 length register	USBF	842
UF0BO2	UF0 bulk-out 2 register	USBF	843
UF0BO2L	UF0 bulk-out 2 length register	USBF	846
UF0CIE0	UF0 configuration/interface/endpoint descriptor register 0	USBF	869
UF0CIE1	UF0 configuration/interface/endpoint descriptor register 1	USBF	869
UF0CIE2	UF0 configuration/interface/endpoint descriptor register 2	USBF	869