Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 15x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atsam3s1ca-au

1. SAM3S Description

Atmel's SAM3S series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 64 MHz and features up to 256 Kbytes of Flash and up to 48 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, 6x general-purpose 16-bit timers, an RTC, an ADC, a 12-bit DAC and an analog comparator.

The SAM3S series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders

The SAM3S device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM3S to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V and is available in 48-, 64- and 100-pin QFP, 48- and 64-pin QFN, and 100-pin BGA packages.

The SAM3S series is the ideal migration path from the SAM7S series for applications that require more performance. The SAM3S series is pin-to-pin compatible with the SAM7Sseries.

1.1 Configuration Summary

The SAM3S series devices differ in memory size, package and features list. Table 1-1 below summarizes the configurations of the device family

Table 1-1. Configuration Summary

Device	Flash	SRAM	Timer Counter Channels	GPIOs	UART/ USARTs	ADC	12-bit DAC Output	External Bus Interface	HSMCI	Package
SAM3S4C	256 Kbytes single plane	48 Kbytes	6	79	2/2(1)	16 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S4B	256 Kbytes single plane	48 Kbytes	3	47	2/2	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S4A	256 Kbytes single plane	48 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S2C	128 Kbytes single plane	32 Kbytes	6	79	2/2(1)	16 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S2B	128 Kbytes single plane	32 Kbytes	3	47	2/2	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S2A	128 Kbytes single plane	32 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S1C	64 Kbytes single plane	16 Kbytes	6	79	2/2(1)	16 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S1B	64 Kbytes single plane	16 Kbytes	3	47	2/2	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S1A	64 Kbytes single plane	16 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48

Note: 1. Full Modem support on USART1.

2. SAM3S Block Diagram

Figure 2-1. SAM3S 100-pin Version Block Diagram

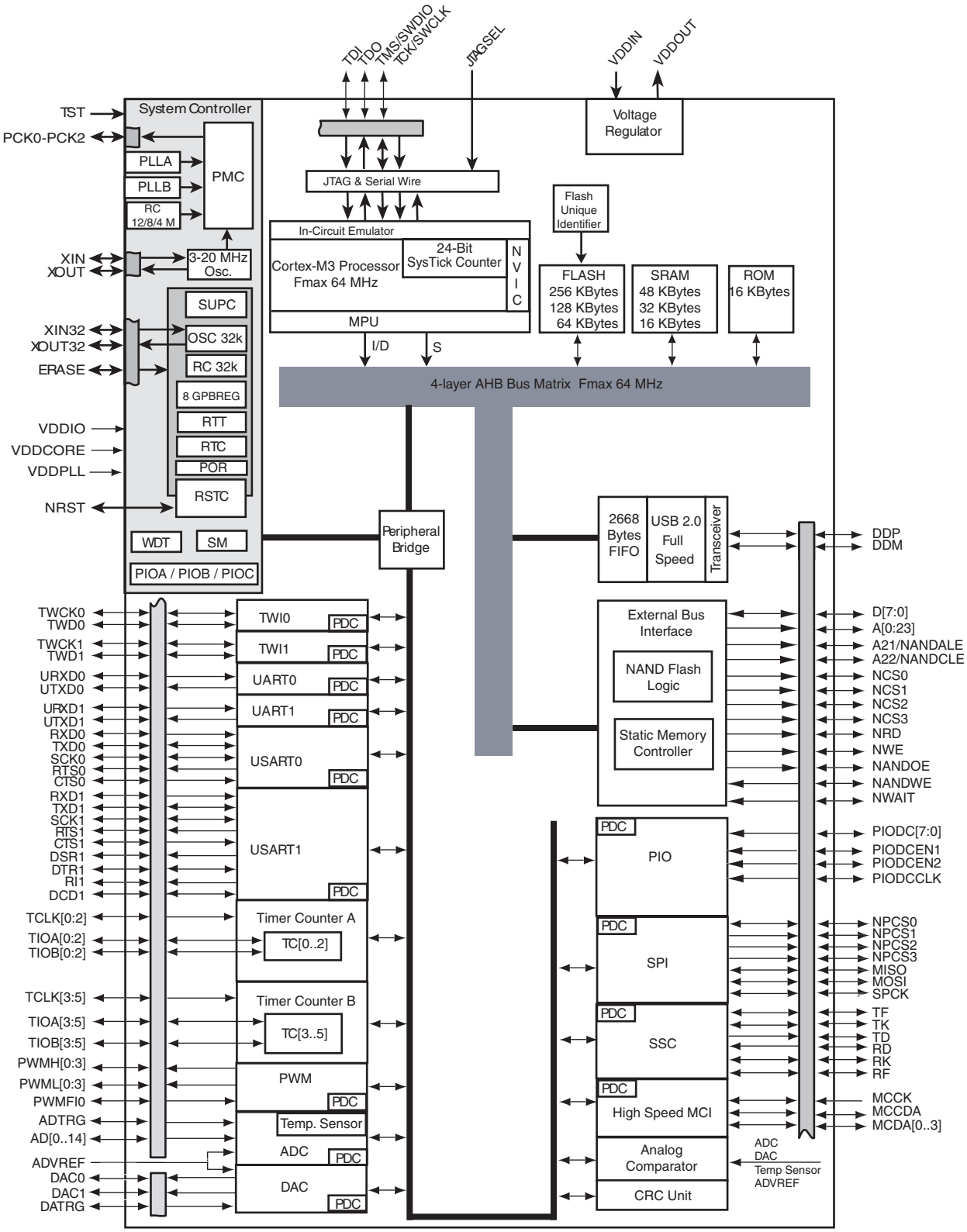


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Universal Asynchronous Receiver Transmitter - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs[2] - Internal pull-up enabled - Schmitt Trigger enabled[1]
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
PIO Controller - Parallel Capture Mode (PIOA Only)					
PIODC0-PIODC7	Parallel Capture Mode Data	Input		VDDIO	
PIODCCLK	Parallel Capture Mode Clock	Input			
PIODCEN1-2	Parallel Capture Mode Enable	Input			
External Bus Interface					
D0 - D7	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Input			
RI1	USART1 Ring Indicator	Input			

4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3S4/2/1C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD1	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/ AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/ AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/ AD2	23	PA8/*XOUT32*/ PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/*XIN32*/ PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

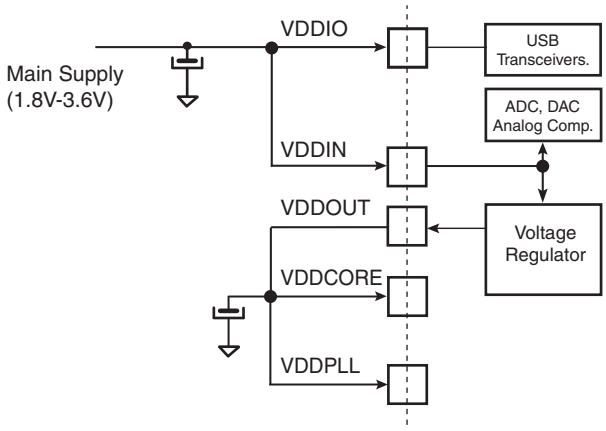
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

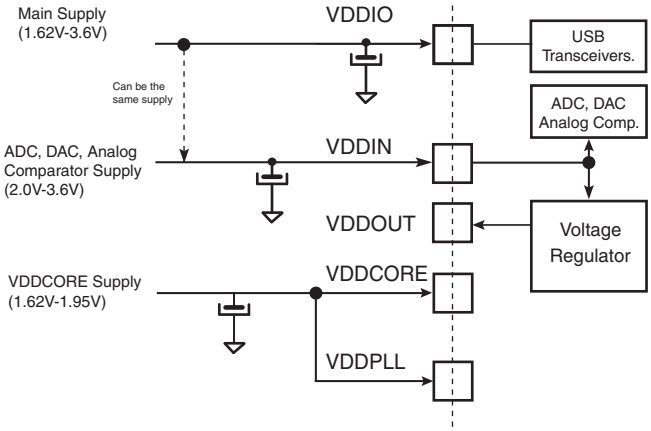
As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 2.0V, USB is not usable.
With VDDIN < 2.0V, ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply and VDDIN ≥ 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.

6. Input/Output Lines

The SAM3S has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

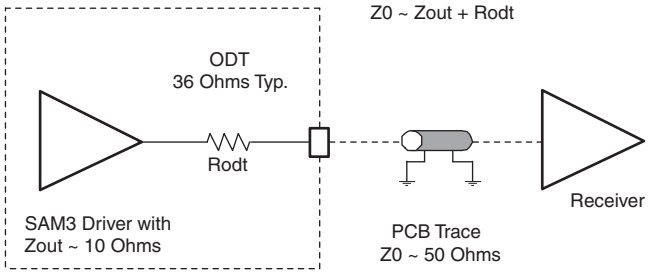
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3S embeds high speed pads able to handle up to 32 MHz for HSMCI (MCK/2), 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), see Figure 6-1. It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3S) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3S system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store
- Three-stage pipeline
- Single cycle 32-bit multiply
- Hardware divide
- Thumb and Debug states
- Handler and Thread modes
- Low latency ISR entry and exit

7.2 APB/AHB bridge

The SAM3S product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S product manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

7.4 Matrix Slaves

The Bus Matrix of the SAM3S product manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

9.1.3.9 *Fast Flash Programming Interface*

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST and PA0 and PA1are tied low.

9.1.3.10 *SAM-BA® Boot*

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 *GPNVM Bits*

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

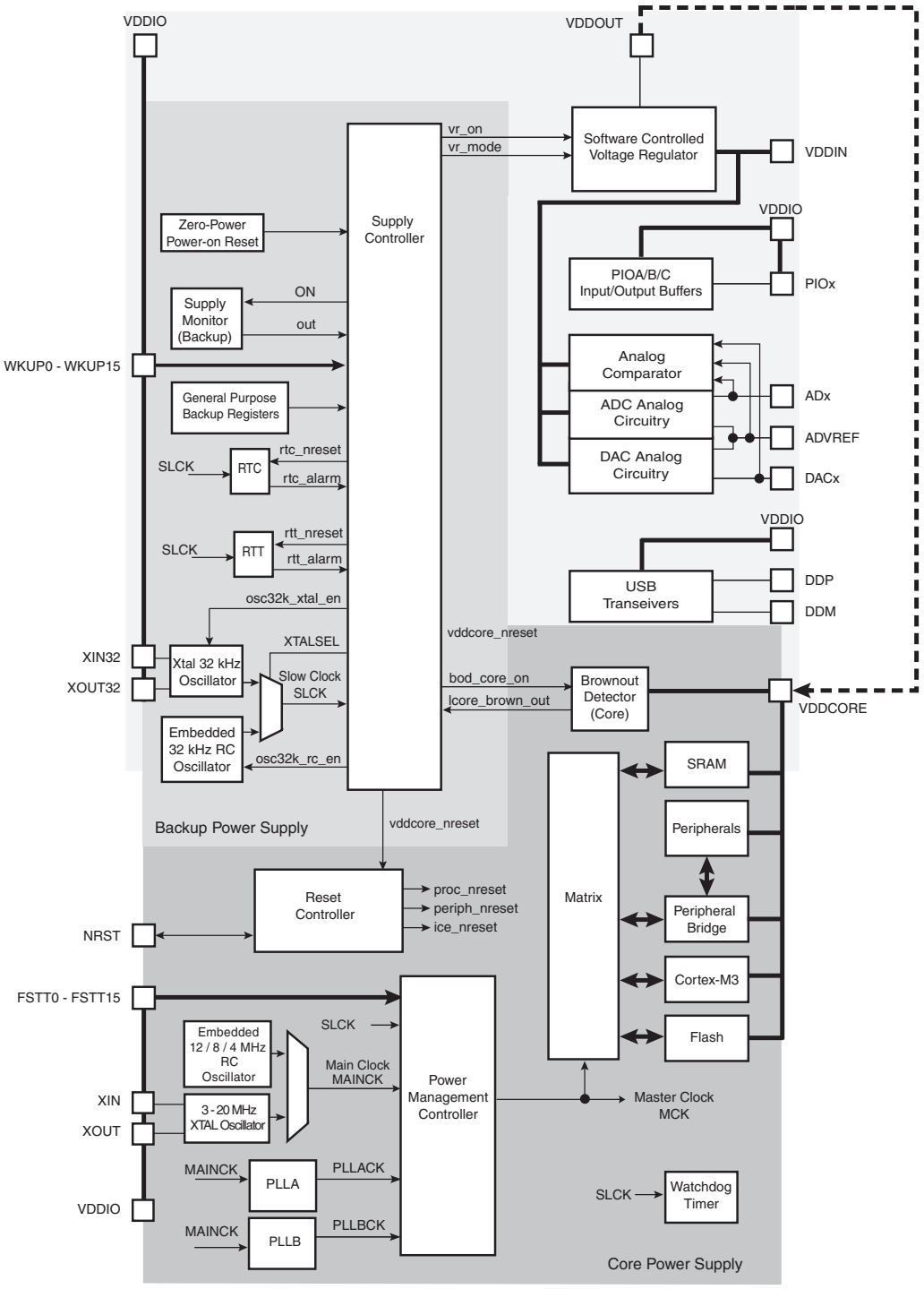
- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
  - Chip Select, Write enable or Read enable Control Mode

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in Figure 10-1 on page 35.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock oscillator with bypass mode
- One Low-Power RC oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 60 to 130 MHz programmable PLL (PLLA), capable to provide the clock MCK to the processor and to the peripherals. The PLLA input frequency is from 3.5 to 20 MHz.

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC	X		Enhanced Embedded Flash Controller
7	-	-		Reserved
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	SMC
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	HSMCI	X	X	High Speed Multimedia Card Interface
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	TC2	X	X	Timer/Counter 2
26	TC3	X	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	X	X	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	X	X	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

11.2 Peripheral Signal Multiplexing on I/O Lines

The SAM3S product features 2 PIO controllers on 48-pin and 64-pin versions (PIOA, PIOB) or 3 PIO controllers on the 100-pin version, (PIOA, PIOB, PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S 64-pin and 100-pin PIO Controllers control up to 32 lines. (See, Table 10-2.) Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following pages define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PA0	PWMH0	TIOA0	A17	WKUP0		High drive
PA1	PWMH1	TIOB0	A18	WKUP1		High drive
PA2	PWMH2	SCK0	DATRG	WKUP2		High drive
PA3	TWD0	NPCS3				High drive
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWMH3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1	PWMFI0	WKUP6		
PA10	UTXD0	NPCS2				
PA11	NPCS0	PWMH0		WKUP7		
PA12	MISO	PWMH1				
PA13	MOSI	PWMH2				
PA14	SPCK	PWMH3		WKUP8		
PA15	TF	TIOA1	PWML3	WKUP14/PIODCEN1		
PA16	TK	TIOB1	PWML2	WKUP15/PIODCEN2		
PA17	TD	PCK1	PWMH3	AD0		
PA18	RD	PCK2	A14	AD1		
PA19	RK	PWML0	A15	AD2/WKUP9		
PA20	RF	PWML1	A16	AD3/WKUP10		
PA21	RXD1	PCK1		AD8		64/100-pin versions
PA22	TXD1	NPCS3	NCS2	AD9		64/100-pin versions
PA23	SCK1	PWMH0	A19	PIODCCLK		64/100-pin versions
PA24	RTS1	PWMH1	A20	PIODC0		64/100-pin versions
PA25	CTS1	PWMH2	A23	PIODC1		64/100-pin versions
PA26	DCD1	TIOA2	MCDA2	PIODC2		64/100-pin versions
PA27	DTR1	TIOB2	MCDA3	PIODC3		64/100-pin versions
PA28	DSR1	TCLK1	MCCDA	PIODC4		64/100-pin versions
PA29	RI1	TCLK2	MCCK	PIODC5		64/100-pin versions
PA30	PWML2	NPCS2	MCDA0	WKUP11/PIODC6		64/100-pin versions
PA31	NPCS1	PCK2	MCDA1	PIODC7		64/100-pin versions

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

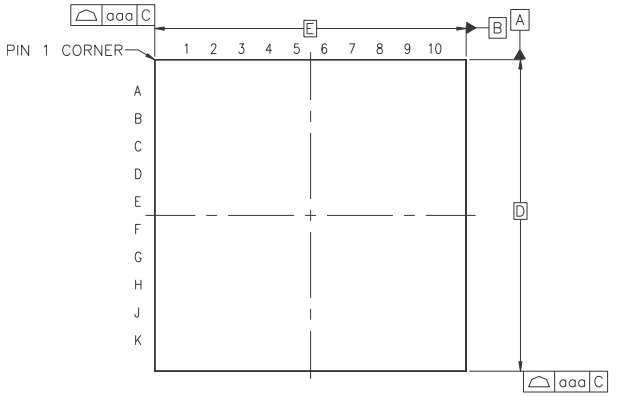
I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWMH0			AD4		
PB1	PWMH1			AD5		
PB2	URXD1	NPCS2		AD6/ WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DDM	
PB11					DDP	
PB12	PWML1				ERASE	
PB13	PWML2	PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWMH3		DAC1		64/100-pin versions

- output selection:
  - Internal signal
  - external pin
  - selectable inverter
- Interrupt on:
  - Rising edge, Falling edge, toggle

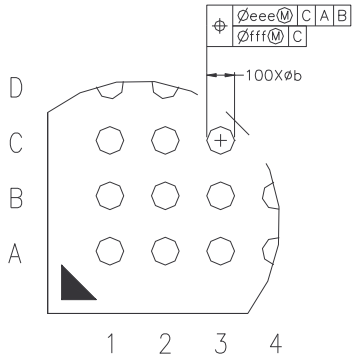
12.14 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

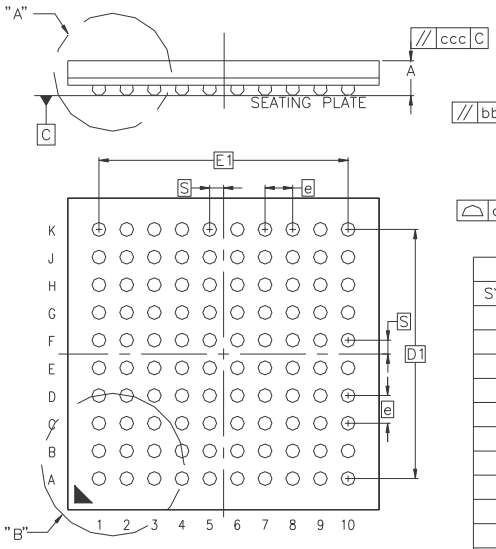
Figure 13-2. 100-ball LFBGA Package Drawing



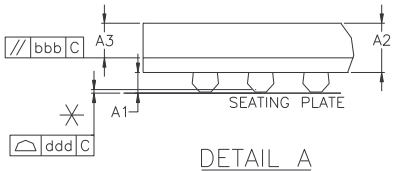
TOP VIEW



DETAIL B(2:1)



BOTTOM VIEW



DETAIL A

ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 13-1. 48-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		