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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 64MHz |
| Connectivity | EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 79 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 15x10/12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFBGA |
| Supplier Device Package | 100-TFBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsam3s2ca-cur |

# 1. SAM3S Description

Atmel's SAM3S series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 64 MHz and features up to 256 Kbytes of Flash and up to 48 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, 6x general-purpose 16-bit timers, an RTC, an ADC, a 12-bit DAC and an analog comparator.

The SAM3S series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders

The SAM3S device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM3S to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V and is available in 48-, 64- and 100-pin QFP, 48- and 64-pin QFN, and 100-pin BGA packages.

The SAM3S series is the ideal migration path from the SAM7S series for applications that require more performance. The SAM3S series is pin-to-pin compatible with the SAM7Sseries.

## 1.1 Configuration Summary

The SAM3S series devices differ in memory size, package and features list. Table 1-1 below summarizes the configurations of the device family

**Table 1-1.** Configuration Summary

| Device | Flash | SRAM | Timer Counter Channels | GPIOs | UART/ USARTs | ADC | 12-bit DAC Output | External Bus Interface | HSMCI | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| SAM3S4C | 256 Kbytes single plane | 48 Kbytes | 6 | 79 | 2/2(1) | 16 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S4B | 256 Kbytes single plane | 48 Kbytes | 3 | 47 | 2/2 | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S4A | 256 Kbytes single plane | 48 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |
| SAM3S2C | 128 Kbytes single plane | 32 Kbytes | 6 | 79 | 2/2(1) | 16 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S2B | 128 Kbytes single plane | 32 Kbytes | 3 | 47 | 2/2 | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S2A | 128 Kbytes single plane | 32 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |
| SAM3S1C | 64 Kbytes single plane | 16 Kbytes | 6 | 79 | 2/2(1) | 16 ch. | 2 | 8-bit data, 4 chip selects, 24-bit address | 1 port 4 bits | LQFP100 BGA100 |
| SAM3S1B | 64 Kbytes single plane | 16 Kbytes | 3 | 47 | 2/2 | 10 ch. | 2 | - | 1 port 4 bits | LQFP64 QFN 64 |
| SAM3S1A | 64 Kbytes single plane | 16 Kbytes | 3 | 34 | 2/1 | 8 ch. | - | - | - | LQFP48 QFN 48 |

Note: 1. Full Modem support on USART1.

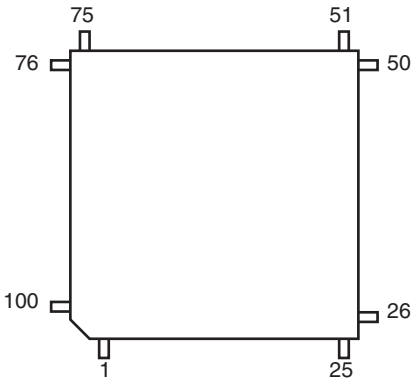
# 4. Package and Pinout

## 4.1 SAM3S4/2/1C Package and Pinout

Figure 4-2 shows the orientation of the 100-ball LFBGA Package

### 4.1.1 100-lead LQFP Package Outline

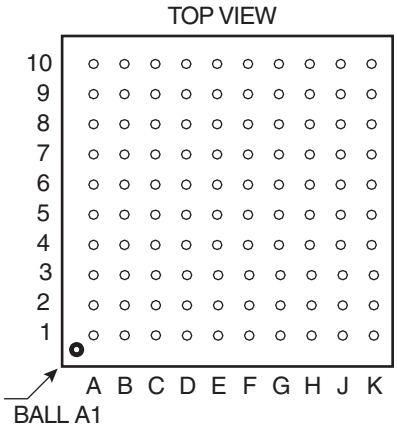
**Figure 4-1.** Orientation of the 100-lead LQFP Package




### 4.1.2 100-ball LFBGA Package Outline

The 100-Ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

**Figure 4-2.** Orientation of the 100-BALL LFBGA Package



### 4.1.4 100-ball LFBGA Pinout

**Table 4-2.** 100-ball LFBGA SAM3S4/2/1C Pinout

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A1 | PB1/AD5 | C6 | TCK/SWCLK/PB7 | F1 | PA18/PGMD6/AD1 | H6 | PC4 |
| A2 | PC29 | C7 | PC16 | F2 | PC26 | H7 | PA11/PGMM3 |
| A3 | VDDIO | C8 | PA1/PGMEN1 | F3 | VDDOUT | H8 | PC1 |
| A4 | PB9/PGMCK/XIN | C9 | PC17 | F4 | GND | H9 | PA6/PGMNOE |
| A5 | PB8/XOUT | C10 | PA0/PGMEN0 | F5 | VDDIO | H10 | TDI/PB4 |
| A6 | PB13/DAC0 | D1 | PB3/AD7 | F6 | PA27/PGMD15 | J1 | PC15/AD11 |
| A7 | DDP/PB11 | D2 | PB0/AD4 | F7 | PC8 | J2 | PC0 |
| A8 | DDM/PB10 | D3 | PC24 | F8 | PA28 | J3 | PA16/PGMD4 |
| A9 | TMS/SWDIO/PB6 | D4 | PC22 | F9 | TST | J4 | PC6 |
| A10 | JTAGSEL | D5 | GND | F10 | PC9 | J5 | PA24/PGMD12 |
| B1 | PC30 | D6 | GND | G1 | PA21/PGMD9/AD8 | J6 | PA25/PGMD13 |
| B2 | ADVREF | D7 | VDDCORE | G2 | PC27 | J7 | PA10/PGMM2 |
| B3 | GNDANA | D8 | PA2/PGMEN2 | G3 | PA15/PGMD3 | J8 | GND |
| B4 | PB14/DAC1 | D9 | PC11 | G4 | VDDCORE | J9 | VDDCORE |
| B5 | PC21 | D10 | PC14 | G5 | VDDCORE | J10 | VDDIO |
| B6 | PC20 | E1 | PA17/PGMD5/AD0 | G6 | PA26/PGMD14 | K1 | PA22/PGMD10/AD9 |
| B7 | PA31 | E2 | PC31 | G7 | PA12/PGMD0 | K2 | PC13/AD10 |
| B8 | PC19 | E3 | VDDIN | G8 | PC28 | K3 | PC12/AD12 |
| B9 | PC18 | E4 | GND | G9 | PA4/PGMNCMD | K4 | PA20/PGMD8/AD3 |
| B10 | TDO/TRACESWO/ PB5 | E5 | GND | G10 | PA5/PGMRDY | K5 | PC5 |
| C1 | PB2/AD6 | E6 | NRST | H1 | PA19/PGMD7/AD2 | K6 | PC3 |
| C2 | VDDPLL | E7 | PA29/AD13 | H2 | PA23/PGMD11 | K7 | PC2 |
| C3 | PC25 | E8 | PA30/AD14 | H3 | PC7 | K8 | PA9/PGMM1 |
| C4 | PC23 | E9 | PC10 | H4 | PA14/PGMD2 | K9 | PA8/XOUT32/PGMM0 |
| C5 | ERASE/PB12 | E10 | PA3 | H5 | PA13/PGMD1 | K10 | PA7/XIN32/ PGMNVALID |

# 5. Power Considerations

## 5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

## 5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

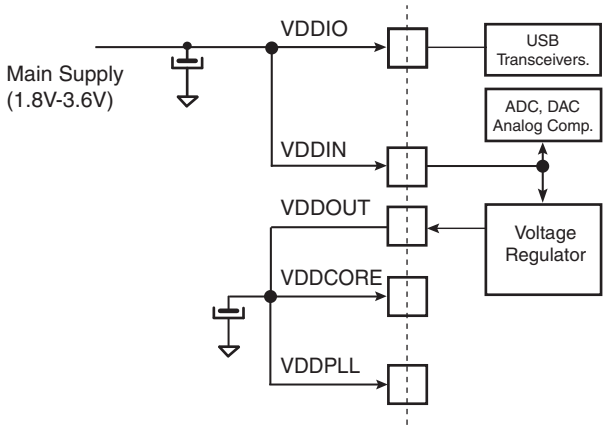
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

## 5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

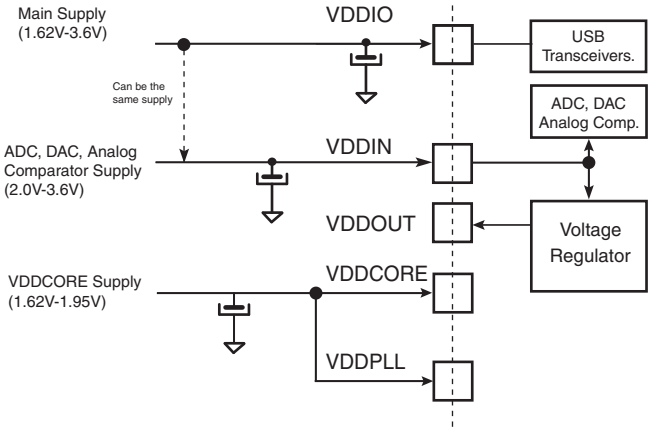
As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

**Figure 5-1.** Single Supply




Note: Restrictions
With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

**Figure 5-2.** Core Externally Supplied




Note: Restrictions
With Main Supply < 2.0V, USB is not usable.
With VDDIN < 2.0V, ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply and VDDIN ≥ 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

### 5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

### 5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

## 5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

**Figure 5-4.** Wake-up Source

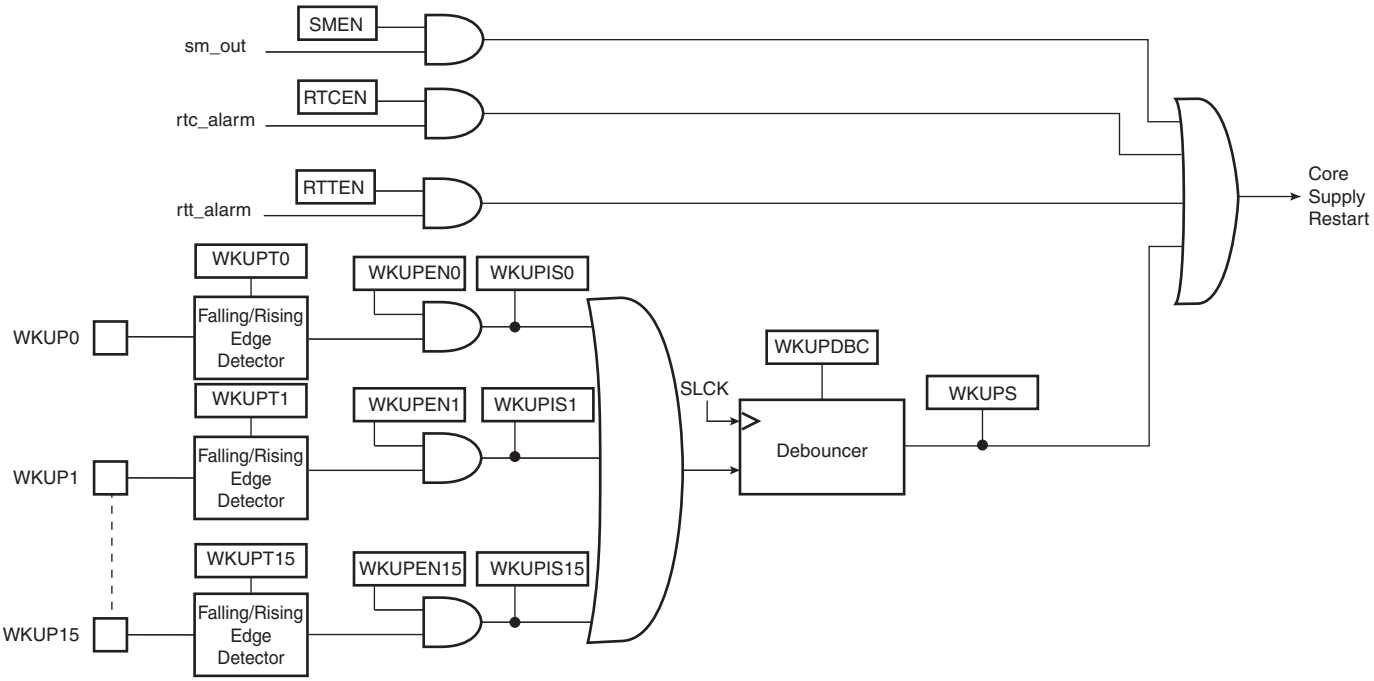


**Table 6-1.** System I/O Configuration Pin List.

| SYSTEM_IO bit number | Default function after reset | Other function | Constraints for normal start | Configuration |
|---|---|---|---|---|
| 12 | ERASE | PB12 | Low Level at startup(1) | In Matrix User Interface Registers (Refer to the SystemIO Configuration Register in the Bus Matrix section of the product datasheet.) |
| 10 | DDM | PB10 | - | |
| 11 | DDP | PB11 | - | |
| 7 | TCK/SWCLK | PB7 | - | |
| 6 | TMS/SWDIO | PB6 | - | |
| 5 | TDO/TRACESWO | PB5 | - | |
| 4 | TDI | PB4 | - | |
| - | PA7 | XIN32 | - | See footnote (2) below |
| - | PA8 | XOUT32 | - | |
| - | PB9 | XIN | - | See footnote (3) below |
| - | PB8 | XOUT | - | |

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode,
2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.
3. In the product Datasheet Refer to: 3 to 20 MHZ Crystal Oscillator information in PMC section.

### 6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 6.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.

**Table 7-4.** Peripheral DMA Controller (Continued)

| Instance Name | Channel T/R | 100 & 64 Pins | 48 Pins |
|---|---|---|---|
| UART0 | Receive | x | x |
| USART1 | Receive | x | x |
| USART0 | Receive | x | x |
| ADC | Receive | x | x |
| SPI | Receive | x | x |
| SSC | Receive | x | x |
| HSMCI | Receive | x | N/A |
| PIOA | Receive | x | x |

## 7.7 Debug and Test Features

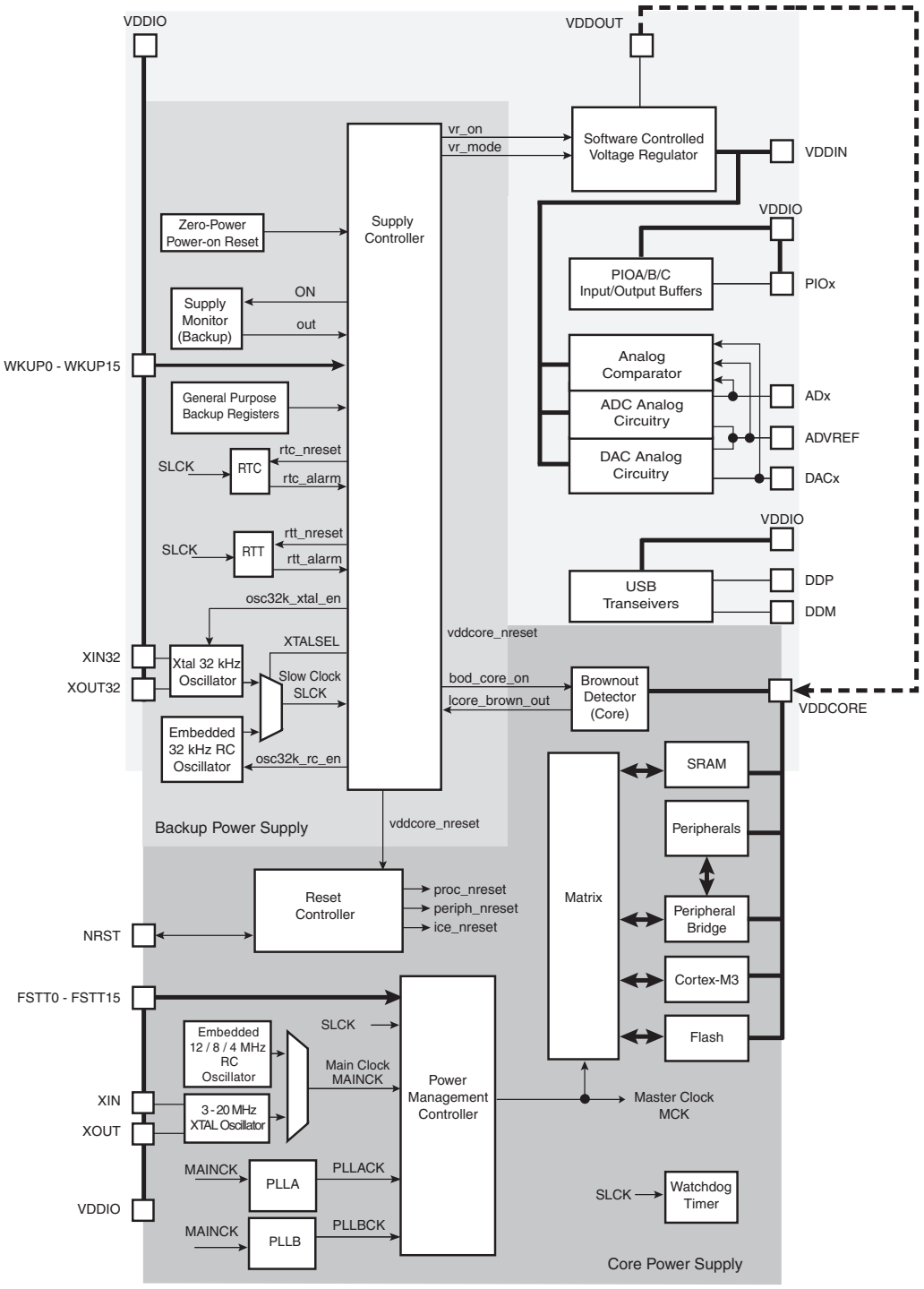
- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

# 10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in Figure 10-1 on page 35.

**Figure 10-1.** System Controller Block Diagram




FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

## 10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

## 10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

**Table 10-2.** PIO available according to pin count

| Version | 48 pin | 64 pin | 100 pin |
|---|---|---|---|
| **PIOA** | 21 | 32 | 32 |
| **PIOB** | 13 | 15 | 15 |
| **PIOC** | - | - | 32 |

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up or pull-down on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

# 12. Embedded Peripherals Overview

## 12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

## 12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and $I^2C$ compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

## 12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

## 12.4 Universal Synchronous Asynchronous Receiver Transceiver (USART)

- Programmable Baud Rate Generator with Fractional Baud rate support
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
  - Full modem line support on USART1 (DCD-DSR-DTR-RI)
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- SPI Mode
  - Master or Slave
  - Serial Clock programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

## 12.5 Synchronous Serial Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, $I^2S$, TDM Buses, Magnetic Card Reader)
- Contains an independent receiver and transmitter and a common clock divider
- Offers configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

## 12.6 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting

- Programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

## 12.8 High Speed Multimedia Card Interface (HSMCI)

- 4-bit or 1-bit Interface
- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD and SDHC Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V1.1.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- HSMCI has one slot supporting
  - One MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
  - One SDIO Card
- Support for stream, block and multi-block data read and write

## 12.9 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64 bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

## 12.10 Analog-to-Digital Converter (ADC)

- up to 16 Channels,
- 10/12-bit resolution
- up to 1 MSample/s
- programmable sequence of conversion on each channel
- Integrated temperature sensor
- Single ended/differential conversion

- output selection:
  - Internal signal
  - external pin
  - selectable inverter
- Interrupt on:
  - Rising edge, Falling edge, toggle

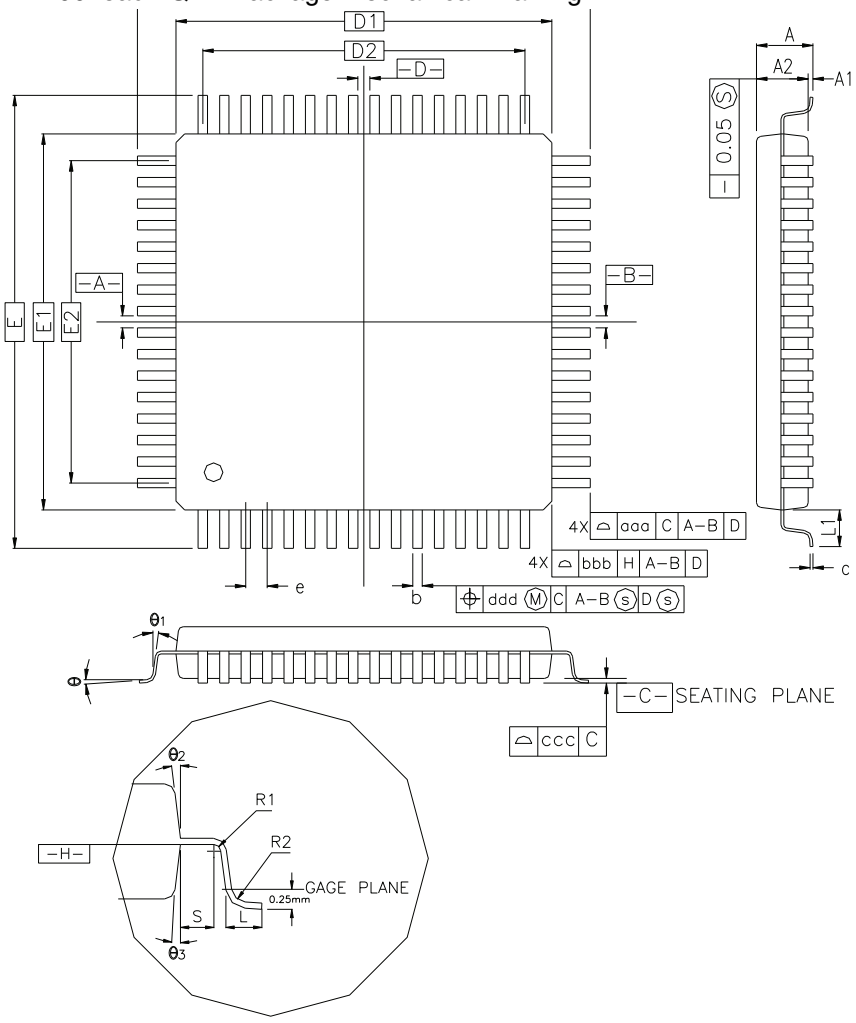
## 12.14 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

# 13. Package Drawings

The SAM3S series devices are available in LQFP, QFN and LFBGA packages.

**Figure 13-1.** 100-lead LQFP Package Mechanical Drawing




COTROL DIMENSIONS ARE IN MILLIMETERS.

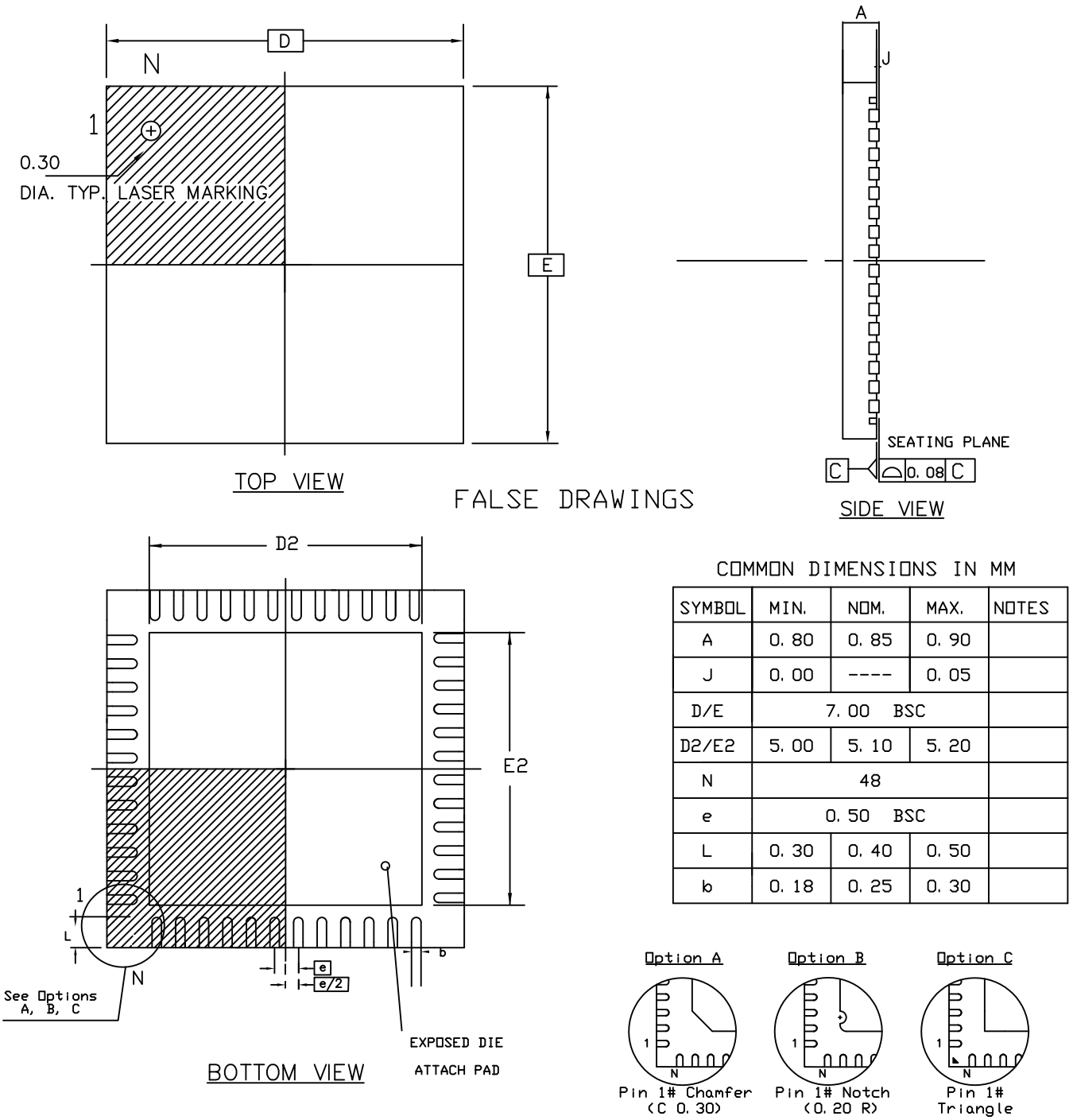
| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | |
| A | — | — | 1.60 | — | — | 0 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0 |
| D | 16.00 BSC. | | | 0.630 BSC | | |
| D1 | 14.00 BSC. | | | 0.551 BSC | | |
| E | 16.00 BSC. | | | 0.630 BSC | | |
| E1 | 14.00 BSC. | | | 0.551 BSC | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0 |
| R1 | 0.08 | — | — | 0.003 | — | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | |
| θ1 | 0° | — | — | 0° | — | |
| θ2 | 11° | 12° | 13° | 11° | 12° | |
| θ3 | 11° | 12° | 13° | 11° | 12° | |
| c | 0.09 | — | 0.20 | 0.004 | — | 0 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 12.00 | | | 0.472 | | |
| E2 | 12.00 | | | 0.472 | | |
| TOLERANCES OF FORM AND POSITIC | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

**Table 13-2.** 64-lead LQFP Package Dimensions (in mm)

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | **Min** | **Nom** | **Max** | **Min** | **Nom** | **Max** |
| A | – | – | 1.60 | – | – | 0.063 |
| A1 | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| D1 | 10.00 BSC | | | 0.383 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| E1 | 10.00 BSC | | | 0.383 BSC | | |
| R2 | 0.08 | – | 0.20 | 0.003 | – | 0.008 |
| R1 | 0.08 | – | – | 0.003 | – | – |
| q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | – | – | 0° | – | – |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | – | 0.20 | 0.004 | – | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | – | – | 0.008 | – | – |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 7.50 | | | 0.285 | | |
| E2 | 7.50 | | | 0.285 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

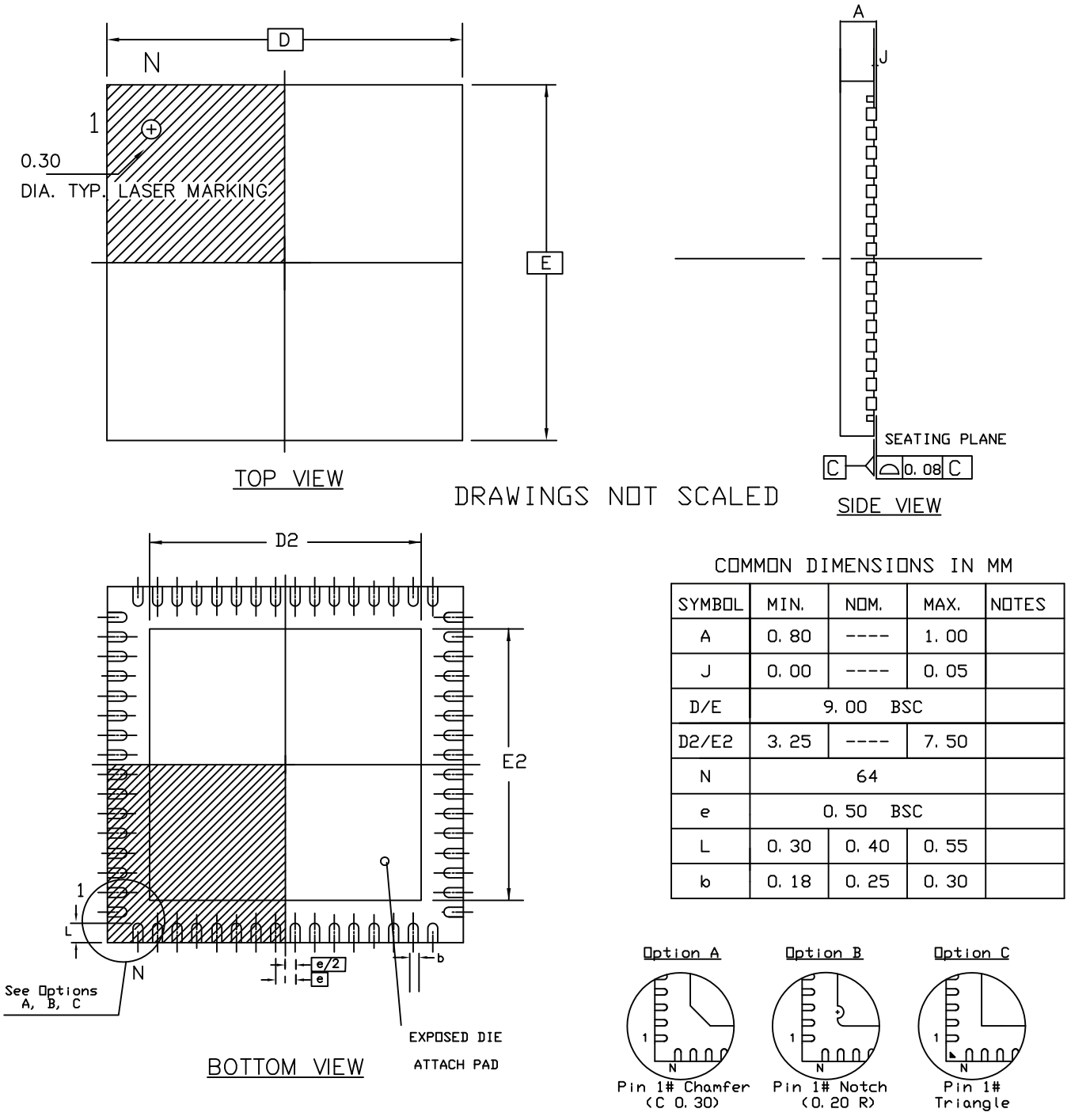
**Figure 13-4.** 48-pad QFN Package




COMMON DIMENSIONS IN MM

| SYMBOL | MIN. | NOM. | MAX. | NOTES |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | |
| J | 0.00 | ---- | 0.05 | |
| D/E | 7.00 BSC | | | |
| D2/E2 | 5.00 | 5.10 | 5.20 | |
| N | 48 | | | |
| e | 0.50 BSC | | | |
| L | 0.30 | 0.40 | 0.50 | |
| b | 0.18 | 0.25 | 0.30 | |

**Figure 13-5.** 64-pad QFN Package Drawing




COMMON DIMENSIONS IN MM

| SYMBOL | MIN. | NOM. | MAX. | NOTES |
|---|---|---|---|---|
| A | 0.80 | ---- | 1.00 | |
| J | 0.00 | ---- | 0.05 | |
| D/E | 9.00 BSC | | | |
| D2/E2 | 3.25 | ---- | 7.50 | |
| N | 64 | | | |
| e | 0.50 BSC | | | |
| L | 0.30 | 0.40 | 0.55 | |
| b | 0.18 | 0.25 | 0.30 | |

# 14. Ordering Information

**Table 14-1.** Ordering Codes for SAM3S Devices

| Ordering Code | MRL | Flash (Kbytes) | Package (Kbytes) | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|
| ATSAM3S4CA-AU | A | 256 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S4CA-CU | A | 256 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S4BA-AU | A | 256 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S4BA-MU | A | 256 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S4AA-AU | A | 256 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S4AA-MU | A | 256 | QFN48 | Green | Industrial -40°C to 85°C |
| ATSAM3S2CA-AU | A | 128 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S2CA-CU | A | 128 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S2BA-AU | A | 128 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S2BA-MU | A | 128 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S2AA-AU | A | 128 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S2AA-MU | A | 128 | QFN48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CA-AU | A | 64 | QFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1CA-CU | A | 64 | BGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BA-AU | A | 64 | QFP64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1BA-MU | A | 64 | QFN64 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AA-AU | A | 64 | QFP48 | Green | Industrial -40°C to 85°C |
| ATSAM3S1AA-MU | A | 64 | QFN48 | Green | Industrial -40°C to 85°C |