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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MSP430 CPU16
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8 + 256B)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/texas-instruments/msp430f2471tpmr

Figure 2-3. SAM3S 48-pin Version Block Diagram

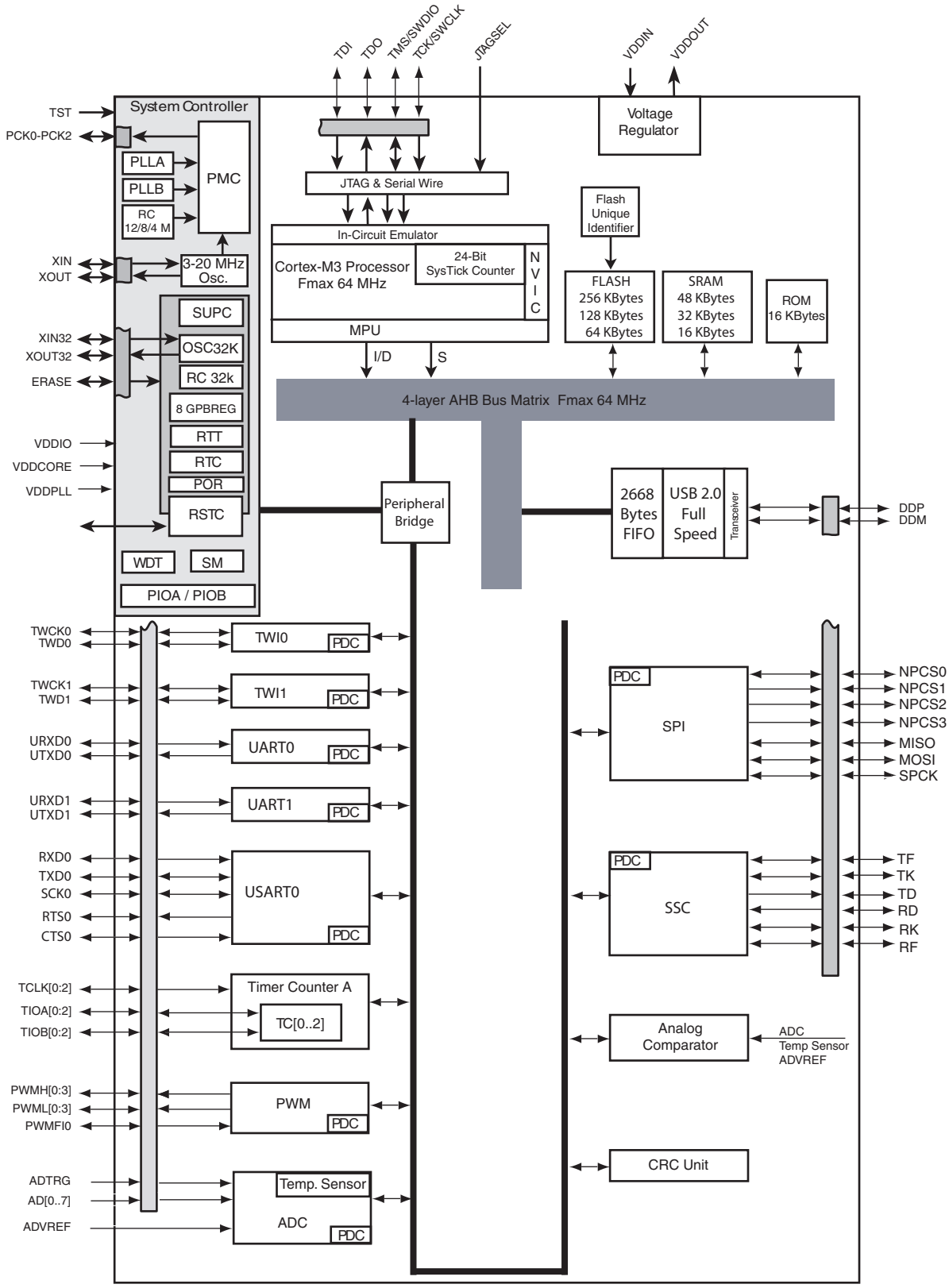


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Universal Asynchronous Receiver Transmitter - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs[2] - Internal pull-up enabled - Schmitt Trigger enabled[1]
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
PIO Controller - Parallel Capture Mode (PIOA Only)					
PIODC0-PIODC7	Parallel Capture Mode Data	Input		VDDIO	
PIODCCLK	Parallel Capture Mode Clock	Input			
PIODCEN1-2	Parallel Capture Mode Enable	Input			
External Bus Interface					
D0 - D7	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Input			
RI1	USART1 Ring Indicator	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled
PWMFI0	**PWM Fault Input**	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog			
Analog-to-Digital Converter - ADC					
AD0 - AD14	Analog Inputs	Analog, Digital			
ADTRG	ADC Trigger	Input		VDDIO	
12-bit Digital-to-Analog Converter - DAC					
DAC0 - DAC1	Analog output	Analog, Digital			
DACTRG	DAC Trigger	Input		VDDIO	

4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3S4/2/1C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD1	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

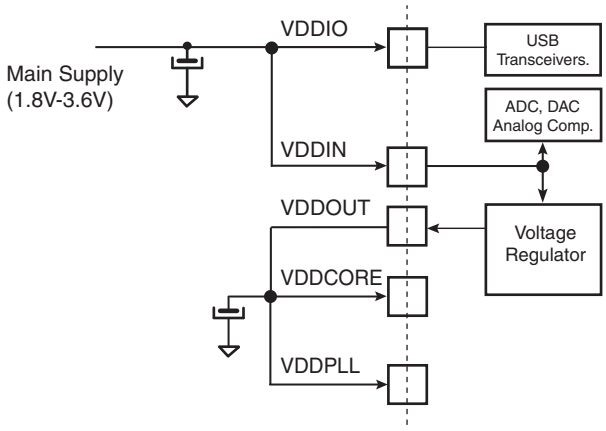
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

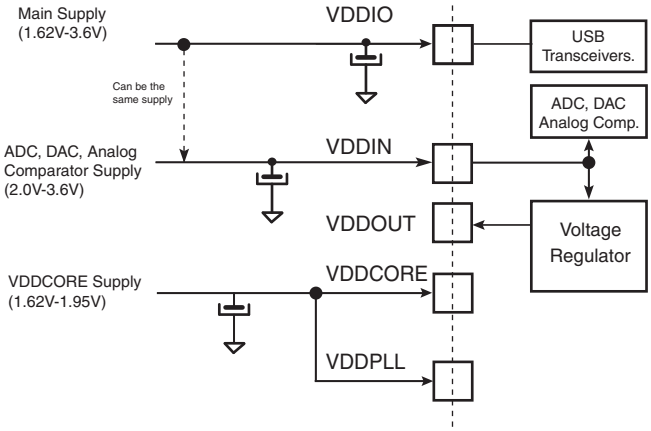
As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 2.0V, USB is not usable.
With VDDIN < 2.0V, ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply and VDDIN ≥ 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.

6. Input/Output Lines

The SAM3S has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

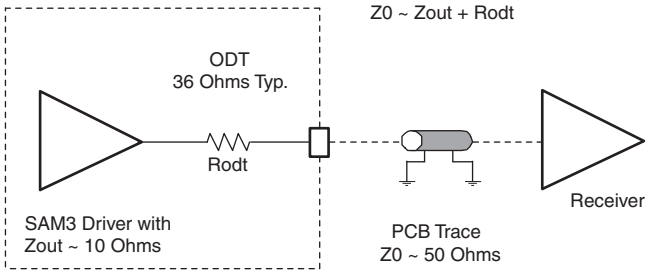
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3S embeds high speed pads able to handle up to 32 MHz for HSMCI (MCK/2), 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), see Figure 6-1. It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3S) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3S system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

Table 7-4. Peripheral DMA Controller (Continued)

Instance Name	Channel T/R	100 & 64 Pins	48 Pins
UART0	Receive	x	x
USART1	Receive	x	x
USART0	Receive	x	x
ADC	Receive	x	x
SPI	Receive	x	x
SSC	Receive	x	x
HSMCI	Receive	x	N/A
PIOA	Receive	x	x

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

The ATSAM3S4 product (256-Kbyte internal Flash version) embeds a total of 48 Kbytes high-speed SRAM.

The ATSAM3S2 product (128-Kbyte internal Flash version) embeds a total of 32 Kbytes high-speed SRAM.

The ATSAM3S1 product (64-Kbyte internal Flash version) embeds a total of 16 Kbytes high-speed SRAM.

The SRAM is accessible over System Cortex-M3 bus at address 0x2000 0000.

The SRAM is in the bit band region. The bit band alias region is mapped from 0x2200 0000 to 0x23FF FFFF.

9.1.2 Internal ROM

The SAM3S product embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

The Flash of the ATSAM3S4 (256-Kbytes internal Flash version) is organized in one bank of 1024 pages (Single plane) of 256 bytes.

The Flash of the ATSAM3S2 (128-Kbytes internal Flash version) is organized in one bank of 512 pages (Single plane) of 256 bytes.

The Flash of the ATSAM3S1 (64-Kbytes internal Flash version) is organized in one bank of 256 pages (Single plane) of 256 bytes.

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

9.1.3.4 *Flash Speed*

The user needs to set the number of wait states depending on the frequency used.

For more details, refer to the AC Characteristics sub section in the product Electrical Characteristics Section.

9.1.3.5 *Lock Regions*

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Number of Lock Bits

Product	Number of Lock Bits	Lock Region Size
ATSAM3S4	16	16 kbytes (64 pages)
ATSAM3S2	8	16 kbytes (64 pages)
ATSAM3S1	4	16 kbytes (64 pages)

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 *Security Bit Feature*

The SAM3S features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 *Calibration Bits*

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 *Unique Identifier*

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 *Fast Flash Programming Interface*

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST and PA0 and PA1are tied low.

9.1.3.10 *SAM-BA® Boot*

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 *GPNVM Bits*

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

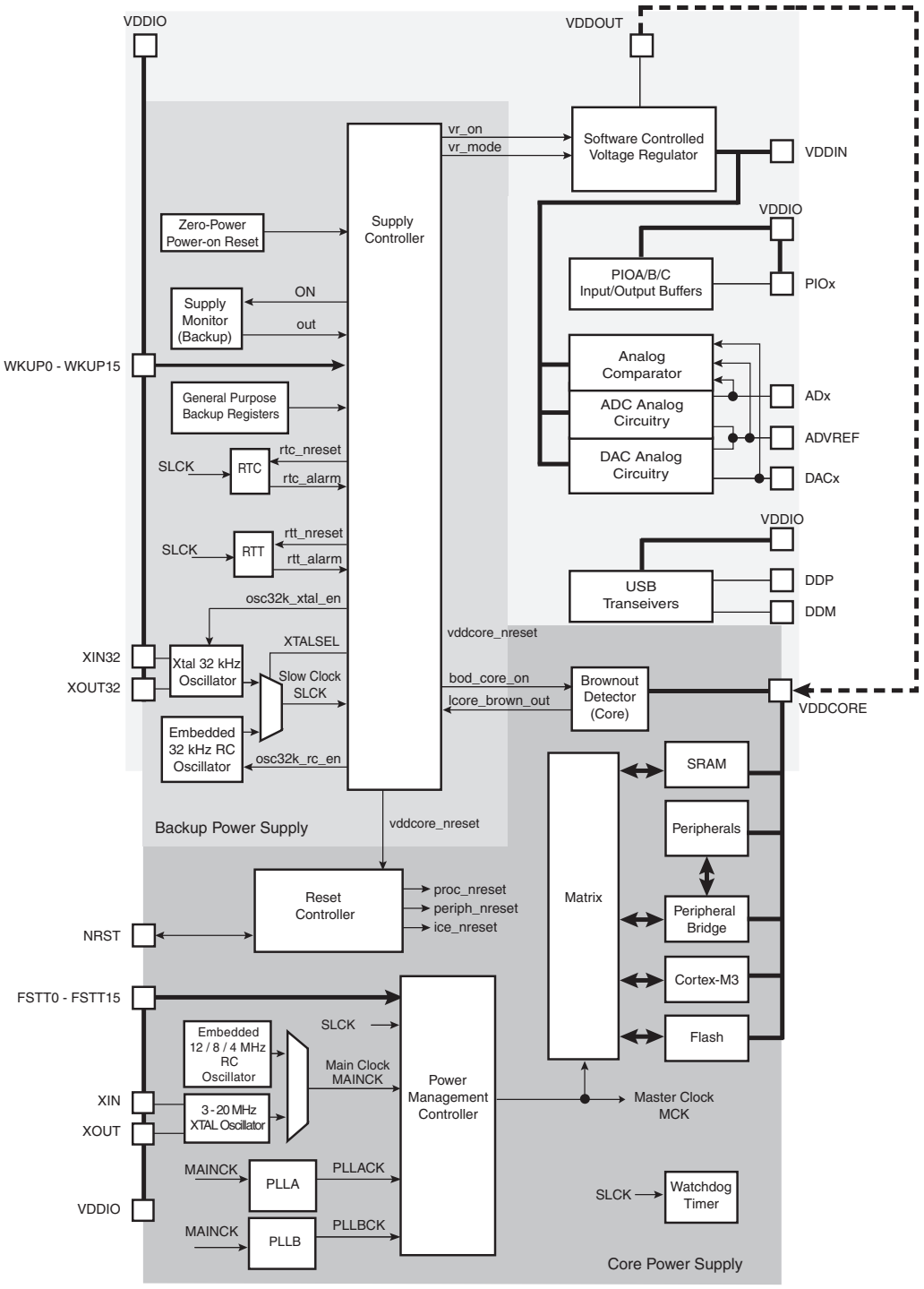
- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
  - Chip Select, Write enable or Read enable Control Mode

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in Figure 10-1 on page 35.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up or pull-down on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC	X		Enhanced Embedded Flash Controller
7	-	-		Reserved
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	SMC
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	HSMCI	X	X	High Speed Multimedia Card Interface
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	TC2	X	X	Timer/Counter 2
26	TC3	X	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	X	X	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	X	X	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0				100-pin version
PC1	D1	PWML1				100-pin version
PC2	D2	PWML2				100-pin version
PC3	D3	PWML3				100-pin version
PC4	D4	NPCS1				100-pin version
PC5	D5					100-pin version
PC6	D6					100-pin version
PC7	D7					100-pin version
PC8	NWE					100-pin version
PC9	NANDOE					100-pin version
PC10	NANDWE					100-pin version
PC11	NRD					100-pin version
PC12	NCS3			AD12		100-pin version
PC13	NWAIT	PWML0		AD10		100-pin version
PC14	NCS0					100-pin version
PC15	NCS1	PWML1		AD11		100-pin version
PC16	A21/NANDALE					100-pin version
PC17	A22/NANDCLE					100-pin version
PC18	A0	PWMH0				100-pin version
PC19	A1	PWMH1				100-pin version
PC20	A2	PWMH2				100-pin version
PC21	A3	PWMH3				100-pin version
PC22	A4	PWML3				100-pin version
PC23	A5	TIOA3				100-pin version
PC24	A6	TIOB3				100-pin version
PC25	A7	TCLK3				100-pin version
PC26	A8	TIOA4				100-pin version
PC27	A9	TIOB4				100-pin version
PC28	A10	TCLK4				100-pin version
PC29	A11	TIOA5		AD13		100-pin version
PC30	A12	TIOB5		AD14		100-pin version
PC31	A13	TCLK5				100-pin version

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

14. Ordering Information

Table 14-1. Ordering Codes for SAM3S Devices

Ordering Code	MRL	Flash (Kbytes)	Package (Kbytes)	Package Type	Temperature Operating Range
ATSAM3S4CA-AU	A	256	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S4CA-CU	A	256	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S4BA-AU	A	256	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S4BA-MU	A	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S4AA-AU	A	256	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S4AA-MU	A	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S2CA-AU	A	128	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S2CA-CU	A	128	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S2BA-AU	A	128	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S2BA-MU	A	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S2AA-AU	A	128	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S2AA-MU	A	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S1CA-AU	A	64	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S1CA-CU	A	64	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S1BA-AU	A	64	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S1BA-MU	A	64	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S1AA-AU	A	64	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S1AA-MU	A	64	QFN48	Green	Industrial -40°C to 85°C

Revision History

Doc. Rev	Comments	Change Request Ref.
6500CS	Missing PGMD8 to 15 added to Table 4-1, “100-lead LQFP SAM3S4/2/1C Pinout” and Table 4-2, “100-ball LFBGA SAM3S4/2/1C Pinout”. Section 5.7 “Fast Startup” updated. Typo fixed on back page: ‘techincal’ --> ‘technical’. Typos fixed in Section 1. “SAM3S Description”. Missing title added to Table 14-1. PLLA input frequency range updated in Section 10.5 “Clock Generator”. A sentence completed in Section 5.5.2 “Wait Mode”. Last sentence removed from Section 9.1.3.10 “SAM-BA® Boot”. ‘three GPNVM bits’ replaced by ‘two GPNVM bits’ in Section 9.1.3.11 “GPNVM Bits”. Leftover sentence removed from Section 4.1 “SAM3S4/2/1C Package and Pinout”.	rfo 7536 7524 7494 7492 7428 7394
6500BS	“Packages” on page 1, package size or pitch updated. Table 1-1, “Configuration Summary”, ADC column updated, footnote gives precision on reserved channel. Table 4-2, “100-ball LFBGA SAM3S4/2/1C Pinout”, pinout information is available. Figure 5-1, "Single Supply",Figure 5-2, "Core Externally Supplied" , updated notes below figures. Figure 5-2, "Core Externally Supplied", Figure 5-3, "Backup Battery", ADC, DAC, Analog Comparator supply is 2.0V-3.6V. Section 12.13 “Analog Comparator”, “Peripherals” on page 1, reference to “window function” removed. Section 9.1.3.8 “Unique Identifier”, Each device integrates its own 128-bit unique identifier.	7214 6981 7201 7243/rfo 7103 7307
6500AS	First issue	

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