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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	SCI
Peripherals	DMA, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvm16f1mkf

Table 1-8. Pin Summary For 64-Pin and 48-Pin Package Options (Sheet 3 of 4)

LQFP Option				Function (Priority and device dependencies specified in PIM chapter)					Power Supply	Internal Pull Resistor	
64 M/ ML	64 MC	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
36	36	26	HG0	—	—	—	—	—	—	—	—
37	37	27	HS0	—	—	—	—	—	—	—	—
38	38	28	HS2	—	—	—	—	—	—	—	—
39	39	29	HG2	—	—	—	—	—	—	—	—
40	40	30	VBS2	—	—	—	—	—	—	—	—
41	41	31	VLS2	—	—	—	—	—	—	—	—
42	42	32	LG2	—	—	—	—	—	—	—	—
43	43	33	LS2	—	—	—	—	—	—	—	—
44	44	34	LS1	—	—	—	—	—	—	—	—
45	45	35	LG1	—	—	—	—	—	—	—	—
46	46	—	VLS1	—	—	—	—	—	—	—	—
47	47	36	VBS1	—	—	—	—	—	—	—	—
48	48	37	HG1	—	—	—	—	—	—	—	—
49	49	38	HS1	—	—	—	—	—	—	—	—
50	50	39	PT0	IOC0_0	PWM1_3	MISO0	RXD0	—	V_{DDX}	PERT/ PPST	Off
51	51	—	PT1	IOC0_1	PWM1_4	MOSI0	TXD0	LP0DR1/ PTURE	V_{DDX}	PERT/ PPST	Off
52	52	—	PT2	IOC0_2	PWM1_5	SCK0	—	—	V_{DDX}	PERT/ PPST	Off
53	53	—	PT3	IOC0_3	SS0	—	—	—	V_{DDX}	PERT/ PPST	Off
54	54	40	RESET	—	—	—	—	—	V_{DDX}	TEST pin	Up
55	55	41	PE1	XTAL	—	—	—	—	V_{DDX}	PERE/ PPSE	Down
56	56	42	PE0	EXTAL	—	—	—	—	V_{DDX}	PERE/ PPSE	Down
57	57	43	VSS1	—	—	—	—	—	—	—	—
58	58	44	VDDF	—	—	—	—	—	V_{DDF}	—	—

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0284	DDRADH	R	DDRADH7[2]	DDRADH6[2]	DDRADH5[2]	DDRADH4[2]	DDRADH3[2]	DDRADH2[2]	DDRADL1[2]	DDRADH0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	PERADH	R	PERADH7[2]	PERADH6[2]	PERADH5[2]	PERADH4[2]	PERADH3[2]	PERADH2[2]	PERADH1[2]	PERADH0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	PPSADH	R	PPSADH7[2]	PPSADH6[2]	PPSADH5[2]	PPSADH4[2]	PPSADH3[2]	PPSADH2[2]	PPSADH1[2]	PPSADH0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	PIEADH	R	PIEADH7[2]	PIEADH6[2]	PIEADH5[2]	PIEADH4[2]	PIEADH3[2]	PIEADH2[2]	PIEADH1[2]	PIEADH0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	PIFADH	R	PIFADH7[2]	PIFADH6[2]	PIFADH5[2]	PIFADH4[2]	PIFADH3[2]	PIFADH2[2]	PIFADH1[2]	PIFADH0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0297	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0298	DIENADH	R	DIENADH7[2]	DIENADH6[2]	DIENADH5[2]	DIENADH4[2]	DIENADH3[2]	DIENADH2[2]	DIENADH1[2]	DIENADH0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								

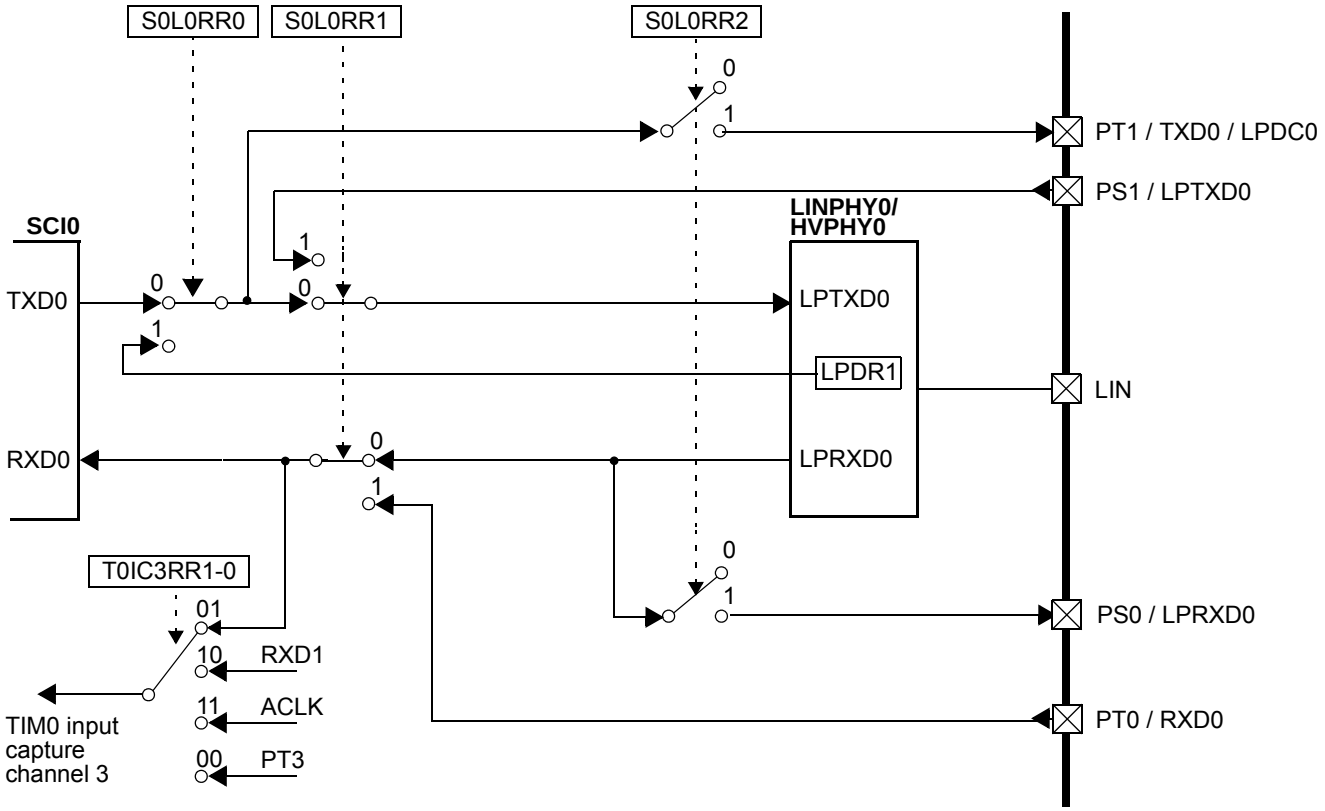


Figure 2-2. SCI0-to-LINPHY0 Routing Options Illustration

Table 2-10. Preferred Interface Configurations

S0L0RR[2:0]	Signal Routing	Description
000	TXD0 → LPTXD0 RXD0 ← LPRXD0	Default setting: SCI0 connects to LINPHY0/HVPHY0, interface internal only
001	LP0DR1 → LPTXD0 RXD0 ← LPRXD0	Direct control setting: LP0DR[LPDR1] register bit controls LPTXD0, interface internal only

Table 2-39. Bit Indices of Implemented Register Bits per Port

	Port Data Register	Port Input Register	Data Direction Register	Pull Device Enable Register	Polarity Select Register	Port Interrupt Enable Register	Port Interrupt Flag Register	Digital Input Enable Register	Reduced Drive Register	Wired-Or Mode Register
ADH	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	0[1]	-	-
ADL	7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
T	3-0	3-0	3-0	3-0	3-0	-	-	-	-	-
S	5-0[2]	5-0[2]	5-0[2]	5-0[2]	5-0[2]	5-0[2]	5-0[2]	-	-	5-0[2]
P	2-0[3]	2-0[3]	2-0[3]	2-0[3]	2-0[3]	2-0[3]	2-0[3]	-	0	-
L[4]	-	0	-	-	0	0	0	0	-	-

1. 7-0 for ZVMC256
2. 3-0 for ZVMC256
3. 1-0 for ZVMC256
4. Only available for ZVMC256

Table 2-40 shows the effect of enabled peripheral features on I/O state and enabled pull devices.

Table 2-40. Effect of Enabled Features

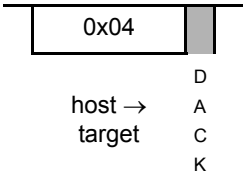
Enabled Feature[1]	Related Signal(s)	Effect on I/O state	Effect on enabled pull device
CPMU OSC	EXTAL, XTAL	CPMU takes control	Forced off
TIM0 output compare	IOC0_x	Forced output	Forced off
TIM0 input capture	IOC0_x	None[2]	None[3]
TIM1 output compare	IOC1_x	Forced output	Forced off
TIM1 input capture	IOC1_x	None[4]	None[5]
SPI0	MISO0, MOSI0, SCK0, $\overline{SS0}$	Controlled input/output	Forced off if output
SCIx transmitter	TXDx	Forced output	Forced off
SCIx receiver	RXDx	Forced input	None[3]
MSCAN0	TXCAN0	Forced output	Forced off
	RXCAN0	Forced input	Pulldown forced off
S12ZDBG	PDO, PDOCLK	Forced output	Forced off
	DBGEEV	None[2]	None[3]
PTU	PTURE, PTUT1-0	Forced output	Forced off
PWM channel	PWMx_x	Forced output	Forced off
PMF fault input	FAULT5	Forced input	None[3]

Enables the hardware handshake protocol in the serial communication. The hardware handshake is implemented by an acknowledge (ACK) pulse issued by the target MCU in response to a host command. The ACK_ENABLE command is interpreted and executed in the BDC logic without the need to interface with the CPU. An ACK pulse is issued by the target device after this command is executed. This command can be used by the host to evaluate if the target supports the hardware handshake protocol. If the target supports the hardware handshake protocol, subsequent commands are enabled to execute the hardware handshake protocol, otherwise this command is ignored by the target. Table 5-8 indicates which commands support the ACK hardware handshake protocol.

For additional information about the hardware handshake protocol, refer to Section 5.4.7," and Section 5.4.8."

5.4.4.4 BACKGROUND

Enter active background mode (if enabled) **Non-intrusive**



Provided ENBDC is set, the BACKGROUND command causes the target MCU to enter active BDM as soon as the current CPU instruction finishes. If ENBDC is cleared, the BACKGROUND command is ignored.

A delay of 16 BDCSI clock cycles is required after the BACKGROUND command to allow the target MCU to finish its current CPU instruction and enter active background mode before a new BDC command can be accepted.

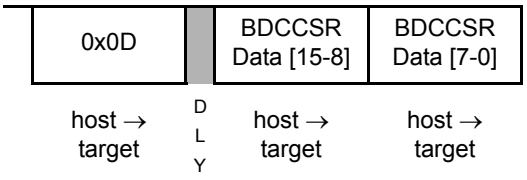
The host debugger must set ENBDC before attempting to send the BACKGROUND command the first time. Normally the host sets ENBDC once at the beginning of a debug session or after a target system reset. During debugging, the host uses GO commands to move from active BDM to application program execution and uses the BACKGROUND command or DBG breakpoints to return to active BDM.

A BACKGROUND command issued during stop or wait modes cannot immediately force active BDM because the WAI instruction does not end until an interrupt occurs. For the detailed mode dependency description refer to Section 5.1.3.3.

The host can recognize this pending BDM request condition because both NORESP and WAIT are set, but BDMACT is clear. Whilst in wait mode, with the pending BDM request, non-intrusive BDC commands are allowed.

5.4.4.18 WRITE_BDCCSR

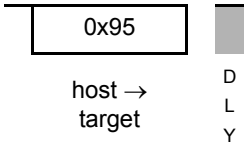
Write BDCCSR **Always Available**



16-bit write to the BDCCSR register. No ACK pulse is generated. Writing to this register can be used to configure control bits or clear flag bits. Refer to the register bit descriptions.

5.4.4.19 ERASE_FLASH

Erase FLASH **Always Available**



Mass erase the internal flash. This command can always be issued. On receiving this command twice in succession, the BDC sets the ERASE bit in BDCCSR and requests a flash mass erase. Any other BDC command following a single ERASE_FLASH initializes the sequence, such that thereafter the ERASE_FLASH must be applied twice in succession to request a mass erase. If 512 BDCSI clock cycles elapse between the consecutive ERASE_FLASH commands then a timeout occurs, which forces a soft reset and initializes the sequence. The ERASE bit is cleared when the mass erase sequence has been completed. No ACK is driven.

During the mass erase operation, which takes many clock cycles, the command status is indicated by the ERASE bit in BDCCSR. Whilst a mass erase operation is ongoing, Always-available commands can be issued. This allows the status of the erase operation to be polled by reading BDCCSR to determine when the operation is finished.

The status of the flash array can be verified by subsequently reading the flash error flags to determine if the erase completed successfully.

ERASE_FLASH can be aborted by a SYNC pulse forcing a soft reset.

NOTE: Device Bus Frequency Considerations

The ERASE_FLASH command requires the default device bus clock frequency after reset. Thus the bus clock frequency must not be changed following reset before issuing an ERASE_FLASH command.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0128-0x012F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0130	DBGCCTL	R	0	NDB	INST	0	RW	RWE	reserved	COMPE
		W								
0x0131-0x0134	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0135	DBGCAH	R	DBGCA[23:16]							
		W								
0x0136	DBGCAM	R	DBGCA[15:8]							
		W								
0x0137	DBGCAL	R	DBGCA[7:0]							
		W								
0x0138	DBGCD0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x0139	DBGCD1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013A	DBGCD2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013B	DBGCD3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x013C	DBGCDM0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x013D	DBGCDM1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013E	DBGCDM2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013F	DBGCDM3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								

Figure 6-2. Quick Reference to DBG Registers

Table 8-14. CPMUCOP Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period generates a COP reset. As long as all writes occur during this window, $55 can be written as often as desired. Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 8-15 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	COP and RTI Stop in Active BDM Mode Bit 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.
5 WRTMASK	**Write Mask for WCOP and CR[2:0] Bit** — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. 0 Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP 1 Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for “write once”.)
2–0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 8-15 and Table 8-16). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a System Reset. This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2^{24} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in Special Mode

Table 8-15. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

8.3.2.23 S12CPMU_UHV_V10_V6 IRC1M Trim Registers (CPMUIRCTRIMH / CPMUIRCTRIML)

Module Base + 0x0018

	15	14	13	12	11	10	9	8
R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
W								
Reset	F	F	F	F	F	0	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-31. S12CPMU_UHV_V10_V6 IRC1M Trim High Register (CPMUIRCTRIMH)

Module Base + 0x0019

	7	6	5	4	3	2	1	0
R	IRCTRIM[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-32. S12CPMU_UHV_V10_V6 IRC1M Trim Low Register (CPMUIRCTRIML)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register). Else write has no effect

NOTE

Writes to these registers while PLLSEL=1 clears the LOCK and UPOSC status bits.

Table 8-27. CPMUIRCTRIMH/L Field Descriptions

Field	Description
15-11 TCTRIM[4:0]	IRC1M temperature coefficient Trim Bits Trim bits for the Temperature Coefficient (TC) of the IRC1M frequency. Table 8-28 shows the influence of the bits TCTRIM[4:0] on the relationship between frequency and temperature. Figure 8-34 shows an approximate TC variation, relative to the nominal TC of the IRC1M (i.e. for TCTRIM[4:0]=0x00000 or 0x10000).
9-0 IRCTRIM[9:0]	**IRC1M Frequency Trim Bits** — Trim bits for Internal Reference Clock After System Reset the factory programmed trim value is automatically loaded into these registers, resulting in a Internal Reference Frequency f_{IRC1M_TRIM}.See device electrical characteristics for value of f_{IRC1M_TRIM}. The frequency trimming consists of two different trimming methods: A rough trimming controlled by bits IRCTRIM[9:6] can be done with frequency leaps of about 6% in average. A fine trimming controlled by bits IRCTRIM[5:0] can be done with frequency leaps of about 0.3% (this trimming determines the precision of the frequency setting of 0.15%, i.e. 0.3% is the distance between two trimming values). Figure 8-33 shows the relationship between the trim bits and the resulting IRC1M frequency.

9.5.2.6 ADC Conversion Flow Control Register (ADCFLWCTL)

Bit set and bit clear instructions should not be used to access this register.

When the ADC is enabled the bits of ADCFLWCTL register can be modified after a latency time of three Bus Clock cycles.
All bits are cleared if bit ADC_EN is clear or via ADC soft-reset.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. ADC Conversion Flow Control Register (ADCFLWCTL)

Read: Anytime

Write:

- Bits SEQA, TRIG, RSTA, LDOK can only be set if bit ADC_EN is set.
- Writing 1’b0 to any of these bits does not have an effect

Timing considerations (Trigger Event - channel sample start) depending on ADC mode configuration:

- Restart Mode
  When the Restart Event has been processed (initial command of current CSL is loaded) it takes two Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from the Trigger Event (bit TRIG set) until the select channel starts to sample.
  During a conversion sequence (back to back conversions) it takes five Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from current conversion period end until the newly selected channel is sampled in the following conversion period.
- Trigger Mode
  When a Restart Event occurs a Trigger Event is issued simultaneously. The time required to process the Restart Event is mainly defined by the internal read data bus availability and therefore can vary. In this mode the Trigger Event is processed immediately after the Restart Event is finished and both conversion flow control bits are cleared simultaneously. From de-assert of bit TRIG until sampling begins five Bus Clock cycles are required. Hence from occurrence of a Restart Event until channel sampling it takes five Bus Clock cycles plus an uncertainty of a few Bus Clock cycles.

For more details regarding the sample phase please refer to Section 9.6.2.2, “Sample and Hold Machine with Sample Buffer Amplifier.

Module Base + 0x00X2

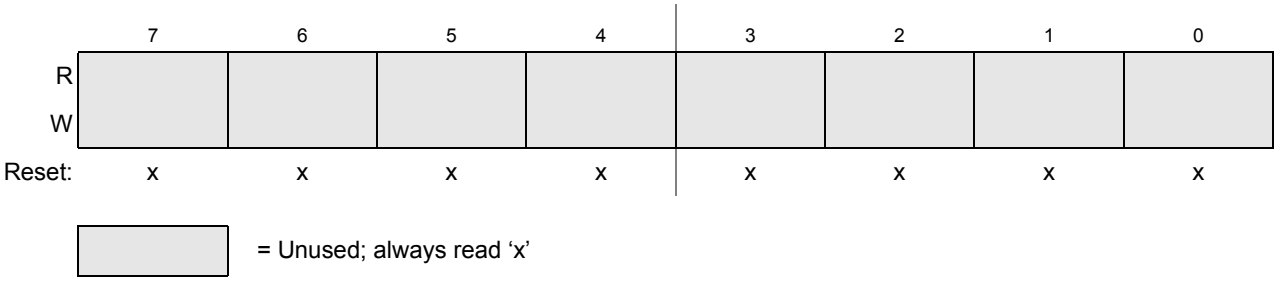


Figure 13-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

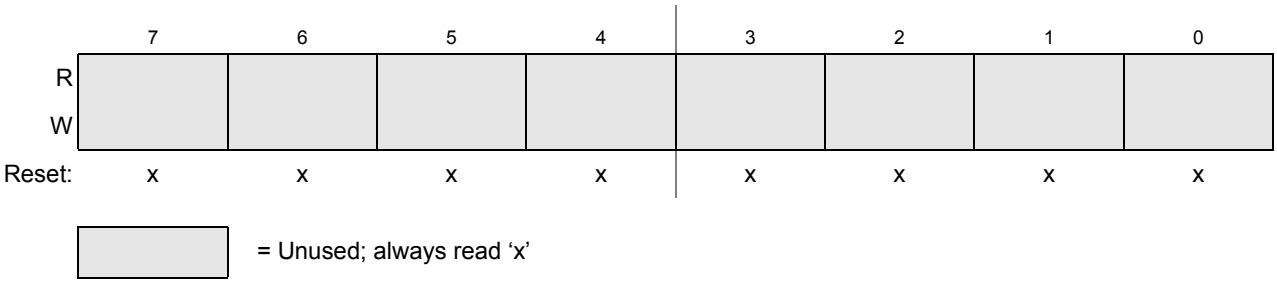


Figure 13-33. Identifier Register 3 — Standard Mapping

13.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

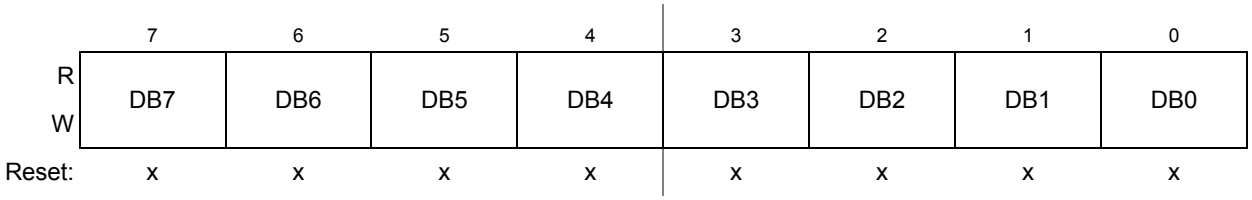


Figure 13-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 13-32. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

error condition the trigger generator reloads the new data from the trigger list and starts to generate the trigger. During an async reload event the TGxREIF interrupt flag is not set.

If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data is ignored and the trigger generator reload error flag (TGxREIF) is not set.

14.4.5.5 Trigger Generator Timing Error

The PTU module requires a defined number of bus clock cycle to load the next trigger value from the memory. This load time defines the minimum possible distance between consecutive trigger values within one trigger list or the distance between the reload event and the first trigger value. If a smaller distance is used then it is possible, depending on device conditions, that the TGxTEIF event is generated. To evaluate the TGxTEIF handling a distance of 1 should be used. This value will generate the TGxTEIF condition independent from the device conditions.

For the specification of this number, please see the Device Overview chapter.

The trigger generator timing error flag (TGxTEIF) is set if the loaded trigger value is smaller than the current counter value. The execution of this trigger list is stopped until the next reload event. There are different reasons for the trigger generator error condition:

- reload time exceeds time of next trigger event
- reload time exceeds the time between two consecutive trigger values
- a subsequent trigger value is smaller than the predecessor trigger value

If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data are ignored and the trigger generator timing error flag (TGxTEIF) is not set.

If enabled (TGxEIE is set) an interrupt will be generated.

14.4.5.6 Trigger Generator Done

The trigger generator done flag (TGxDIF) is set if the loaded trigger value contains 0x0000 or if the number of maximum trigger events (32) was reached. Please note, that the time which is required to load the next trigger value defines the delay between the generation of the last trigger and the assertion of the done flag. If enabled (TGxDIE is set) an interrupt is generated.If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data are ignored and the trigger generator done flag (TGxDIF) is not set.

14.4.6 Debugging

To see the internal status of the trigger generator the register TGxLIST, TGxTNUM, and TGxTV can be used. The TGxLIST register shows the number of currently used list. The TGxTNUM shows the number of generated triggers since the last reload event. If the maximum number of triggers was generated then this register shows zero. The trigger value loaded from the memory to generate the next trigger event is visible inside the TGxTV register. If the execution of the trigger list is done then these registers are unchanged until the next reload event. The next PWM reload event clears the TGxTNUM register and toggles the used trigger list if PTULDOK was set.

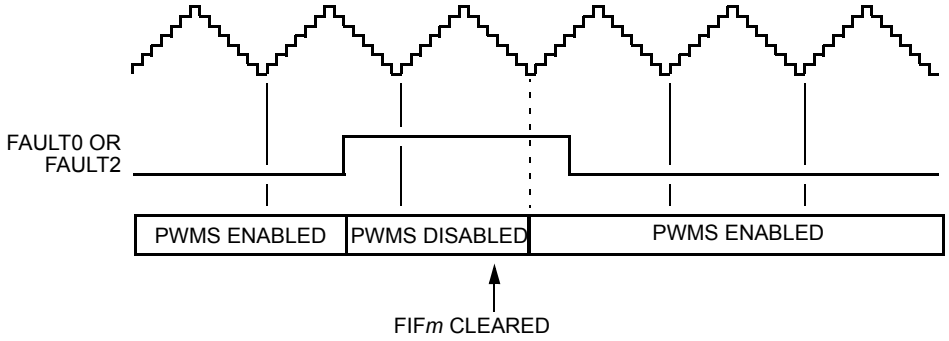


Figure 15-85. Manual Fault Recovery (Faults 0 and 2) — QSMP = 01, 10, or 11

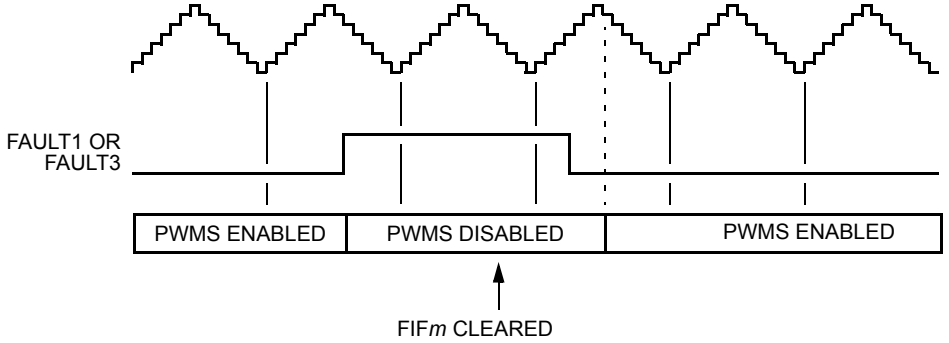


Figure 15-86. Manual Fault Recovery (Faults 1 and 3-5)

NOTE

PWM half-cycle boundaries occur at both the PWM cycle start and when the counter equals the modulus, so in edge-aligned operation full-cycles and half-cycles are equal.

NOTE

Fault protection also applies during software output control when the OUTCTL*n* bits are set. Fault recovery still occurs at half PWM cycle boundaries while the PWM generator is engaged, PWMEN equals one. But the OUT*n* bits can control the PWM outputs while the PWM generator is off, PWMEN equals zero. Thus, fault recovery occurs at IPbus cycles while the PWM generator is off and at the start of PWM cycles when the generator is engaged.

15.5 Resets

All PMF registers are reset to their default values upon any system reset.

15.6 Clocks

The gated system core clock is the clock source for all PWM generators. The system clock is used as a clock source for any other logic in this module. The system bus clock is used as clock for specific control registers and flags (LDOK*x*, PWMRF*x*, PMFOUTB).

16.3.2.8 SCI Status Register 2 (SCISR2)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-11. SCI Status Register 2 (SCISR2)

Read: Anytime

Write: Anytime

Table 16-12. SCISR2 Field Descriptions

Field	Description
7 AMAP	**Alternative Map** — This bit controls which registers sharing the same address space are accessible. In the reset condition the SCI behaves as previous versions. Setting AMAP=1 allows the access to another set of control and status registers and hides the baud rate and SCI control Register 1. 0 The registers labelled SCIBDH (0x0000),SCIBDL (0x0001), SCICR1 (0x0002) are accessible 1 The registers labelled SCIASR1 (0x0000),SCIACR1 (0x0001), SCIACR2 (0x00002) are accessible
4 TXPOL	**Transmit Polarity** — This bit control the polarity of the transmitted data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
3 RXPOL	**Receive Polarity** — This bit control the polarity of the received data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
2 BRK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode** — This bit determines whether the TXD pin is going to be used as an input or output, in the single-wire mode of operation. This bit is only relevant in the single-wire mode of operation. 0 TXD pin to be used as an input in single-wire mode 1 TXD pin to be used as an output in single-wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

Table 20-19. FPROT Field Descriptions (continued)

Field	Description
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0xFF_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 20-22. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 20-20. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

1. For range sizes, refer to Table 20-21 and Table 20-22.

Table 20-21. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0xFF_F800–0xFF_FFFF	2 KB
01	0xFF_F000–0xFF_FFFF	4 KB
10	0xFF_E000–0xFF_FFFF	8 KB
11	0xFF_C000–0xFF_FFFF	16 KB

Table 20-22. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0xFF_8000–0xFF_83FF	1 KB
01	0xFF_8000–0xFF_87FF	2 KB
10	0xFF_8000–0xFF_8FFF	4 KB
11	0xFF_8000–0xFF_9FFF	8 KB

All possible P-Flash protection scenarios are shown in Figure 20-14 . Although the protection scheme is loaded from the Flash memory at global address 0xFF_FE0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in normal single chip mode while providing as much protection as possible if reprogramming is not required.

Table 20-31. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x01	Erase Verify All Blocks	Verify that all EEPROM (and P-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that the EEPROM block is erased.
0x08	Erase All Blocks	Erase all EEPROM (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the DFPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a EEPROM (or P-Flash) block. An erase of the full EEPROM block is only possible when DPOPEN bit in the DFPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the EEPROM block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the EEPROM block (special modes only).
0x10	Erase Verify EEPROM Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program EEPROM	Program up to four words in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.
0x13	Protection Override	Supports a mode to temporarily override Protection configuration (for P-Flash and/or EEPROM) by verifying a key.

20.4.6 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 20-32 are permitted to be run simultaneously on Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality. Any attempt to access P-Flash and EEPROM simultaneously when it is not allowed will result in an illegal access that will trigger a machine exception in the CPU (see device information for details). Please note that during the execution of each command there is a period, before the operation in the Flash array actually starts, where reading is allowed and valid data is returned. Even if the simultaneous operation is marked as not allowed the Flash will report an illegal access only in the cycle the read collision actually happens, maximizing the time the array is available for reading.

If more than one hardblock exists on a device, then read operations on one hardblock are permitted whilst program or erase operations are executed on the other hardblock.

20.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0xFF_FE00-0xFF_FE07). If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the Verify Backdoor Access Key command (see Section 20.4.7.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 20-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 20.4.7.11
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0xFF_FE0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0xFF_FE00-0xFF_FE07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF_FE00-0xFF_FE07 in the Flash configuration field.

20.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode using an automated procedure described in Section 20.4.7.7.1, “Erase All Pin”.

20.5.3 Mode and Security Effects on Flash Command Availability

The availability of Flash module commands depends on the MCU operating mode and security state as shown in Table 20-29.

21.2.1 CANH — CAN Bus High Pin

The CANH signal either connects directly to CAN bus high line or through an optional external common mode choke.

21.2.2 CANL — CAN Bus Low Pin

The CANL signal either connects directly to CAN bus low line or through an optional external common mode choke.

21.2.3 SPLIT — CAN Bus Termination Pin

The SPLIT pin can drive a 2.5 V bias for bus termination purpose (CAN bus middle point). Usage of this pin is optional and depends on bus termination strategy for a given bus network.

21.2.4 VDDC — Supply Pin for CAN Physical Layer

The VDDC pin is used to supply the CAN Physical Layer with 5 V from an external source.

21.2.5 VSSC — Ground Pin for CAN Physical Layer

The VSSC pin is the return path for the 5 V supply (VDDC).

21.3 Internal Signal Description

21.3.1 CPTXD — TXD Input to CAN Physical Layer

CPTXD is the input signal to the CAN Physical Layer. A logic 1 on this input is considered CAN recessive and a logic 0 as dominant level.

Per default, CPTXD is connected device-internally to the TXCAN transmitter output of the MSCAN module. For optional routing options consult the device level documentation.

21.3.2 CPRXD — RXD Output of CAN Physical Layer

CPRXD is the output signal of the CAN Physical Layer. A logic 1 on this output represents CAN recessive and a logic 0 a dominant level.

In stand-by mode the wake-up receiver is routed to this output. A dominant pulse filter can optionally be enabled to increase robustness against false wake-up pulses. In any other mode this signal defaults to the precision receiver without a pulse filter.

Per default, CPRXD is connected device-internally to the RXCAN receiver input of the MSCAN module. For optional routing options consult the device level documentation.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low order CAEx bit. The high order CAEx bit has no effect.

Table 22-13 is used to summarize which channels are used to set the various control bits when in 16-bit mode.

Table 22-13. 16-bit Concatenation Mode Summary

Note: Bits related to available channels have functional significance.

CONxx	PWMEx	PPOLx	PCLKx	CAEx	PWMx Output
CON67	PWME7	PPOL7	PCLK7	CAE7	PWM7
CON45	PWME5	PPOL5	PCLK5	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	CAE1	PWM1

22.4.2.8 PWM Boundary Cases

Table 22-14 summarizes the boundary conditions for the PWM regardless of the output mode (left aligned or center aligned) and 8-bit (normal) or 16-bit (concatenation).

Table 22-14. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
$00 (indicates no duty)	>$00	1	Always low
$00 (indicates no duty)	>$00	0	Always high
XX	$00[1] (indicates no period)	1	Always high
XX	$00[1] (indicates no period)	0	Always low
>= PWMPERx	XX	1	Always high
>= PWMPERx	XX	0	Always low

1. Counter = $00 and does not count.

22.5 Resets

The reset state of each individual bit is listed within the Section 22.3.2, “Register Descriptions” which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters do not count.

Appendix K
Package Information

The Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C.
For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number and review parametrics.

Table K-1. Package To Mask Set Mapping

Product	S12ZVM16, S12ZVM32, S12ZVML31			S12ZVML32, S12ZVML64, S12ZVML128, S12ZVMC64, S12ZVMC128			S12ZVMC256	
Mask-rev	1.0(1)	1.1		3.1	3.2	3.3	1.0[1]	1.1
Maskset-No	0-N14N	1-N14N		1-N95G	2-N95G	3-N95G	0-N00R	1-N00R
Package option	64LQFP-EP	48LQFP-EP	64LQFP-EP	64LQFP-EP	64LQFP-EP	64LQFP-EP	80LQFP-EP	80LQFP-EP
Typ. Exposed pad size (mm)	4.9 x 4.9	4.4x 4.4	6.1 x 6.1	4.9 x 4.9	4.9 x 4.9	6.1 x 6.1	5.6 x 5.6	5.6 x 5.6
Min. Solderable area (mm)	4.0 x 4.0	3.5 x 3.5	5.2 x 5.2	4.0 x 4.0	4.0 x 4.0	5.2 x 5.2	4.9 x 4.9	4.9 x 4.9
Max. Solderable area (mm)	5.7 x 5.7	5.2 x 5.2	7.0 x 7.0	5.7 x 5.7	5.7 x 5.7	7.0 x 7.0	6.2 x 6.2	6.2 x 6.2

1. These mask revisions were used during prototyping only, they are not supported for production