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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	SCI
Peripherals	DMA, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvm16f1mkfr

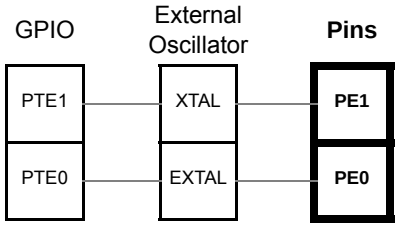
2.1 Introduction

2.1.1 Overview

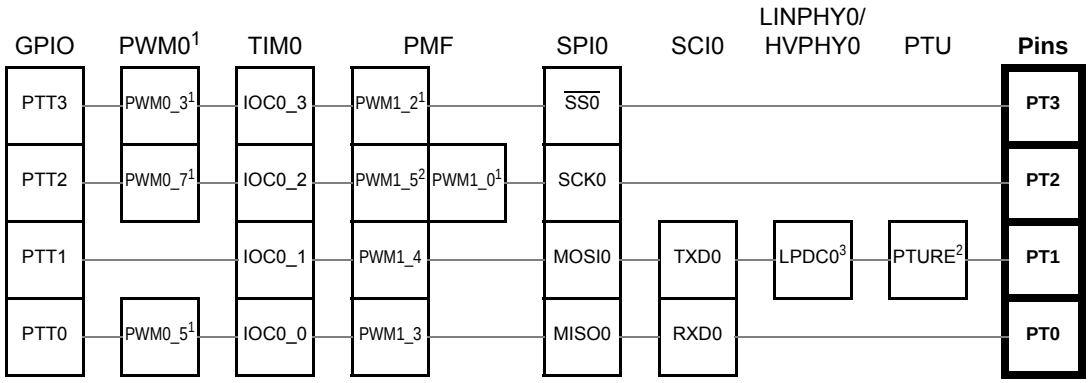
The S12ZVM-family port integration module establishes the interface between the peripheral modules and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers:

- Port E



- Port T



1. Only available for ZVMC256
2. Not available for ZVMC256
3. Only available for ZVML128, ZVML64, ZVML32, ZVML31, ZVM32, and ZVM16

3.4.2 Illegal Accesses

The S12ZMMC module monitors all memory traffic for illegal accesses. See Table 3-9 for a complete list of all illegal accesses.

Table 3-9. Illegal memory accesses

		S12ZCPU	S12ZBDC	ADCs and PTU
Register space	Read access	ok	ok	illegal access
	Write access	ok	ok	illegal access
	Code execution	illegal access		
RAM	Read access	ok	ok	ok
	Write access	ok	ok	ok
	Code execution	ok		
EEPROM	Read access	ok(1)	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Reserved Space	Read access	ok	ok	illegal access
	Write access	only permitted in SS mode	ok	illegal access
	Code execution	illegal access		
Reserved Read-only Space	Read access	ok	ok	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
NVM IFR	Read access	ok[1]	ok[1]	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
Program NVM	Read access	ok[1]	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Unmapped Space	Read access	illegal access	illegal access	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		

1. Unsupported NVM accesses during NVM command execution (“collisions”), are treated as illegal accesses.

Illegal accesses are reported in several ways:

- All illegal accesses performed by the S12ZCPU trigger machine exceptions.
- All illegal accesses performed through the S12ZBDC interface, are captured in the ILLACC bit of the BDCCSRL register.

Table 6-15. DBGCNT Field Descriptions

Field	Description
6–0 CNT[6:0]	**Count Value** — The CNT bits [6:0] indicate the number of valid data lines stored in the trace buffer. Table 6-16 shows the correlation between the CNT bits and the number of valid data lines in the trace buffer. When the CNT rolls over to zero, the TBF bit in DBGSR is set. Thereafter incrementing of CNT continues if configured for end-alignment or mid-alignment. The DBGCNT register is cleared when ARM in DBGC1 is written to a one. The DBGCNT register is cleared by power-on-reset initialization but is not cleared by other system resets. If a reset occurs during a debug session, the DBGCNT register still indicates after the reset, the number of valid trace buffer entries stored before the reset occurred. The DBGCNT register is not decremented when reading from the trace buffer.

Table 6-16. CNT Decoding Table

TBF (DBGSR)	CNT[6:0]	Description
0	0000000	No data valid
0	0000001	32 bits of one line valid
0	0000010 0000100 0000110 .. 1111100	1 line valid 2 lines valid 3 lines valid .. 62 lines valid
0	1111110	63 lines valid
1	0000000	64 lines valid; if using Begin trigger alignment, ARM bit is cleared and the tracing session ends.
1	0000010 .. 1111110	64 lines valid, oldest data has been overwritten by most recent data

6.3.2.7 Debug State Control Register 1 (DBGSCR1)

Address: 0x0107

	7	6	5	4	3	2	1	0
R W	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
Reset	0	0	0	0	0	0	0	0

Figure 6-9. Debug State Control Register 1 (DBGSCR1)

Read: Anytime.

Write: If DBG is not armed and PTACT is clear.

The state control register 1 selects the targeted next state whilst in State1. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.12”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 8-13. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$
0010 (÷3)	$3x10^3$	$6x10^3$	$15x10^3$	$30x10^3$	$60x10^3$	$150x10^3$	$300x10^3$	$600x10^3$
0011 (÷4)	$4x10^3$	$8x10^3$	$20x10^3$	$40x10^3$	$80x10^3$	$200x10^3$	$400x10^3$	$800x10^3$
0100 (÷5)	$5x10^3$	$10x10^3$	$25x10^3$	$50x10^3$	$100x10^3$	$250x10^3$	$500x10^3$	$1x10^6$
0101 (÷6)	$6x10^3$	$12x10^3$	$30x10^3$	$60x10^3$	$120x10^3$	$300x10^3$	$600x10^3$	$1.2x10^6$
0110 (÷7)	$7x10^3$	$14x10^3$	$35x10^3$	$70x10^3$	$140x10^3$	$350x10^3$	$700x10^3$	$1.4x10^6$
0111 (÷8)	$8x10^3$	$16x10^3$	$40x10^3$	$80x10^3$	$160x10^3$	$400x10^3$	$800x10^3$	$1.6x10^6$
1000 (÷9)	$9x10^3$	$18x10^3$	$45x10^3$	$90x10^3$	$180x10^3$	$450x10^3$	$900x10^3$	$1.8x10^6$
1001 (÷10)	$10\ x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$	$500x10^3$	$1x10^6$	$2x10^6$
1010 (÷11)	$11\ x10^3$	$22x10^3$	$55x10^3$	$110x10^3$	$220x10^3$	$550x10^3$	$1.1x10^6$	$2.2x10^6$
1011 (÷12)	$12x10^3$	$24x10^3$	$60x10^3$	$120x10^3$	$240x10^3$	$600x10^3$	$1.2x10^6$	$2.4x10^6$
1100 (÷13)	$13x10^3$	$26x10^3$	$65x10^3$	$130x10^3$	$260x10^3$	$650x10^3$	$1.3x10^6$	$2.6x10^6$
1101 (÷14)	$14x10^3$	$28x10^3$	$70x10^3$	$140x10^3$	$280x10^3$	$700x10^3$	$1.4x10^6$	$2.8x10^6$
1110 (÷15)	$15x10^3$	$30x10^3$	$75x10^3$	$150x10^3$	$300x10^3$	$750x10^3$	$1.5x10^6$	$3x10^6$
1111 (÷16)	$16x10^3$	$32x10^3$	$80x10^3$	$160x10^3$	$320x10^3$	$800x10^3$	$1.6x10^6$	$3.2x10^6$

8.3.2.29 VDDS Status Register (CPMUVDDS)

This register is only available in V10.

The CPMUVDDS register contains the status and flag bits for VDDS1 and VDDS2 to indicate integrity fails. Monitoring of VDDS1 and VDDS2 domain is only active in full performance mode (FPM) and if the respective supply is enabled in CPMUVREGCTL register. It is disabled in reduced performance mode (RPM).

Module Base + 0x001F

	7	6	5	4	3	2	1	0
R	SCS2	SCS1	LVDS2	LVDS1	SCS2IF	SCS1IF	LVS2IF	LVS1IF
W								
Reset	0	0	U	U	0	0	U	U

The Reset state of LVDS and LVIF depends on the external supplied VDDA level
"U" = Unknown, either 0 or 1

= Unimplemented or Reserved

Figure 8-40. VDDS Status Register (CPMUVDDS)

Read: Anytime

Write: SCS2IF, SCS1IF, LVS2IF and LVS1IF are write anytime,
SCS2, SCS, LVS2 and LVS1 are read only

Table 8-33. CPMUVDDS Field Descriptions

Field	Description
7 SCS2	Short circuit on VDDS2 Status Bit —This read-only status bit reflects short circuit status on VDDS2 supply. This feature only makes sense if the VDDS2 supply is enabled (EXT2SON=1). 0 VRH2EN=0 or RPM or VDDS2 voltage level is less than or equal to VDDA supply. 1 VRH2EN=1and FPM and the voltage level on VDDS2 is greater than on VDDA supply.
6 SCS1	Short circuit on VDDS1 Status Bit —This read-only status bit reflects short circuit status on VDDS1 supply. This feature only makes sense if the VDDS1 supply is enabled (EXT1SON=1). 0 VRH1EN=0 or RPM or VDDS1 voltage level is less than or equal to VDDA supply. 1 VRH1EN=1and FPM and the voltage level on VDDS1 is greater than on VDDA supply.
5 LVDS2	Low Voltage on VDDS2 Status Bit —This read-only status bit reflects the voltage level on VDDS2 supply. If VDDS2 is enabled (EXTS2ON=1 in CPMUVREGCTL register), it is monitored that VDDS2 does not drop below a voltage threshold V_{DDSM}. 0 VDDS2 voltage is above V_{DDSM} threshold or VDDS2 is disabled or RPM. 1 EXTS2ON =1 and VDDS2 voltage is below V_{DDSM} threshold and FPM.
4 LVDS1	Low Voltage on VDDS1 Status Bit —This read-only status bit reflects the voltage level on VDDS1 supply. If VDDS1 is enabled (EXTS1ON=1 in CPMUVREGCTL register), it is monitored that VDDS1 does not drop below a voltage threshold V_{DDSM}. 0 VDDS1 voltage is above V_{DDSM} threshold or VDDS1 is disabled or RPM. 1 EXTS1ON =1 and VDDS1 voltage is below V_{DDSM} threshold and FPM.

9.6.3.2.1 Introduction of The Command Sequence List (CSL) Format

A Command Sequence List (CSL) contains up to 64 conversion commands. A user selectable number of successive conversion commands in the CSL can be grouped as a command sequence. This sequence of conversion commands is successively executed by the ADC at the occurrence of a Trigger Event. The commands of a sequence are successively executed until an “End Of Sequence” or “End Of List” command type identifier in a command is detected (command type is coded via bits CMD_SEL[1:0]). The number of successive conversion commands that belong to a command sequence and the number of command sequences inside the CSL can be freely defined by the user and is limited by the 64 conversion commands a CSL can contain. A CSL must contain at least one conversion command and one “end of list” command type identifier. The minimum number of command sequences inside a CSL is zero and the maximum number of command sequences is 63. A command sequence is defined with bits CMD_SEL[1:0] in the register ADCCMD_M by defining the end of a conversion sequence. The Figure 9-29 and Figure 9-30 provides examples of a CSL.

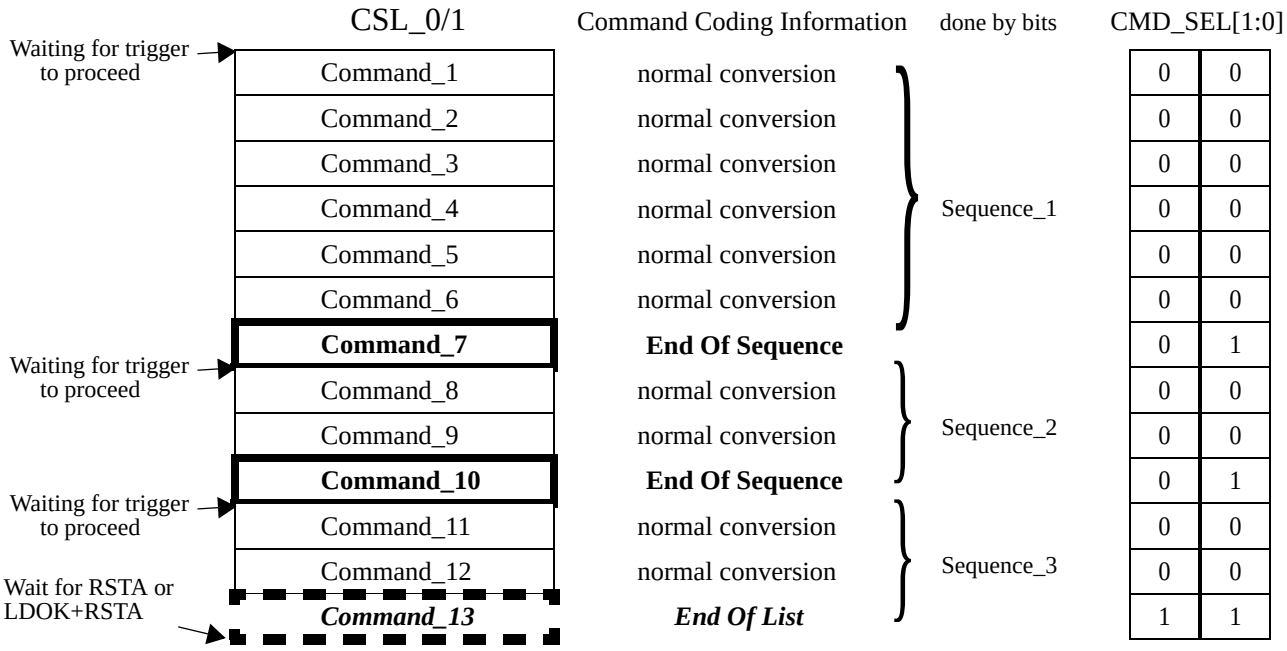


Figure 9-29. Example CSL with sequences and an “End Of List” command type identifier

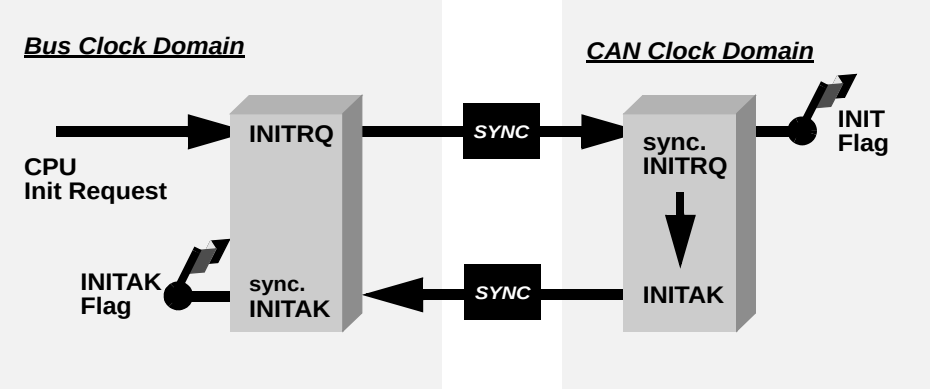


Figure 13-45. Initialization Request/Acknowledge Cycle

Due to independent clock domains within the MSCAN, INITRQ must be synchronized to all domains by using a special handshake mechanism. This handshake causes additional synchronization delay (see Figure 13-45).

If there is no message transfer ongoing on the CAN bus, the minimum delay will be two additional bus clocks and three additional CAN clocks. When all parts of the MSCAN are in initialization mode, the INITAK flag is set. The application software must use INITAK as a handshake indication for the request (INITRQ) to go into initialization mode.

NOTE

The CPU cannot clear INITRQ before initialization mode (INITRQ = 1 and INITAK = 1) is active.

13.4.5 Low-Power Options

If the MSCAN is disabled (CANE = 0), the MSCAN clocks are stopped for power saving.

If the MSCAN is enabled (CANE = 1), the MSCAN has two additional modes with reduced power consumption, compared to normal mode: sleep and power down mode. In sleep mode, power consumption is reduced by stopping all clocks except those to access the registers from the CPU side. In power down mode, all clocks are stopped and no power is consumed.

Table 13-37 summarizes the combinations of MSCAN and CPU modes. A particular combination of modes is entered by the given settings on the CSWAI and SLPRQ/SLPAK bits.

Table 15-6. PMFCFG0 Field Descriptions (continued)

Field	Description
1 INDEPB	**Independent or Complementary Operation for Pair B**— This bit determines if the PWM channels 2 and 3 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are complementary PWM pair 1 PWM2 and PWM3 are independent PWMs
0 INDEPA	**Independent or Complementary Operation for Pair A**— This bit determines if the PWM channels 0 and 1 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are complementary PWM pair 1 PWM0 and PWM1 are independent PWMs

15.3.2.2 PMF Configure 1 Register (PMFCFG1)

Address: Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-4. PMF Configure 1 Register (PMFCFG1)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

A normal PWM output or positive polarity means that the PWM channel outputs high when the counter value is smaller than or equal to the pulse width value and outputs low otherwise. An inverted output or negative polarity means that the PWM channel outputs low when the counter value is smaller than or equal to the pulse width value and outputs high otherwise.

NOTE

The TOPNEGx and BOTNEGx are intended for adapting to the polarity of external predrivers on devices driving the PWM output directly to pins. If an integrated GDU is driven it must be made sure to keep the reset values of these bits in order not to violate the deadtime insertion.

Table 15-7. PMFCFG1 Field Descriptions

Field	Description
6 ENCE	**Enable Commutation Event —** This bit enables the commutation event input and activates buffering of registers PMFOUTC and PMFOUTB and MSKx bits.This bit cannot be modified after the WP bit is set.If set to zero the commutation event input is ignored and writes to the above registers and bits will take effect immediately. If set to one, the commutation event input is enabled and the value written to the above registers and bits does not take effect until the next commutation event occurs. 0 Commutation event input disabled and PMFOUTC, PMFOUTB and MSK*n* not buffered 1 Commutation event input enabled and PMFOUTC, PMFOUTB and MSK*n* buffered
5 BOTNEGC	**Pair C Bottom-Side PWM Polarity** — This bit determines the polarity for Pair C bottom-side PWM (PWM5). This bit cannot be modified after the WP bit is set. 0 Positive PWM5 polarity 1 Negative PWM5 polarity

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD\_C} = PMFDTMC / f_{PWM\_C} = PMFDTMC \times P_C \times T_{core} \qquad \textit{Eqn. 15-3}$$

15.3.2.34 PMF Disable Mapping Registers (PMFDMP0-5)

Address: Module Base + 0x0038 PMFDMP0
Module Base + 0x0039 PMFDMP1
Module Base + 0x003A PMFDMP2
Module Base + 0x003B PMFDMP3
Module Base + 0x003C PMFDMP4
Module Base + 0x003D PMFDMP5

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DMP*n*5		DMP*n*4		DMP*n*3	DMP*n*2	DMP*n*1	DMP*n*0
Reset	0	0	0	0	0	0	0	0

Figure 15-39. PMF Disable Mapping Register (PMFDMP0-5)

1. Read: Anytime
Write: This register cannot be modified after the WP bit is set.

Table 15-37. PMFDMP0-5 Field Descriptions

Field	Description
7-6 DMP*n*5	**PWM Disable Mapping Channel *n* FAULT5** — This bit selects for PWM*n* whether the output is disabled or forced to OUTF*n* at a FAULT5 event. Disabling PWM*n* has priority over forcing PWM*n* to OUTF*n*. This register cannot be modified after the WP bit is set. This setting takes effect at the next cycle start. 00 PWM*n* unaffected by FAULT5 event (interrupt flag setting only) 01 PWM*n* unaffected by FAULT5 event (interrupt flag setting only) 10 PWM*n* disabled on FAULT5 event 11 PWM*n* forced to OUTF*n* on FAULT5 event *n* is 0, 1, 2, 3, 4 and 5.
5-4 DMP*n*4	**PWM Disable Mapping Channel *n* FAULT4** — This bit selects for PWM*n* whether the output is disabled or forced to OUTF*n* at a FAULT4 event. Disabling PWM*n* has priority over forcing PWM*n* to OUTF*n*. This register cannot be modified after the WP bit is set. This setting takes effect at the next cycle start. 00 PWM*n* unaffected by FAULT4 event (interrupt flag setting only) 01 PWM*n* unaffected by FAULT4 event (interrupt flag setting only) 10 PWM*n* disabled on FAULT4 event 11 PWM*n* forced to OUTF*n* on FAULT4 event *n* is 0, 1, 2, 3, 4 and 5.
3-0 DMP*n*	**PWM Disable Mapping Channel *n* FAULT3-0** — This bit selects for PWM*n* if the output is disabled at a FAULT3-0 event. Disabling PWM*n* has priority over forcing PWM*n* to OUTF*n*. This bit cannot be modified after the WP bit is set. FAULT3-0 have priority over FAULT5-4.This setting takes effect at the next cycle start. 0 PWM*n* unaffected by FAULT3-0 event 1 PWM*n* disabled on FAULT3-0 event *n* is 0, 1, 2, 3, 4 and 5.

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

16.4.6.3 Data Sampling

The RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 16-21) is re-synchronized immediatelly at bus clock edge:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

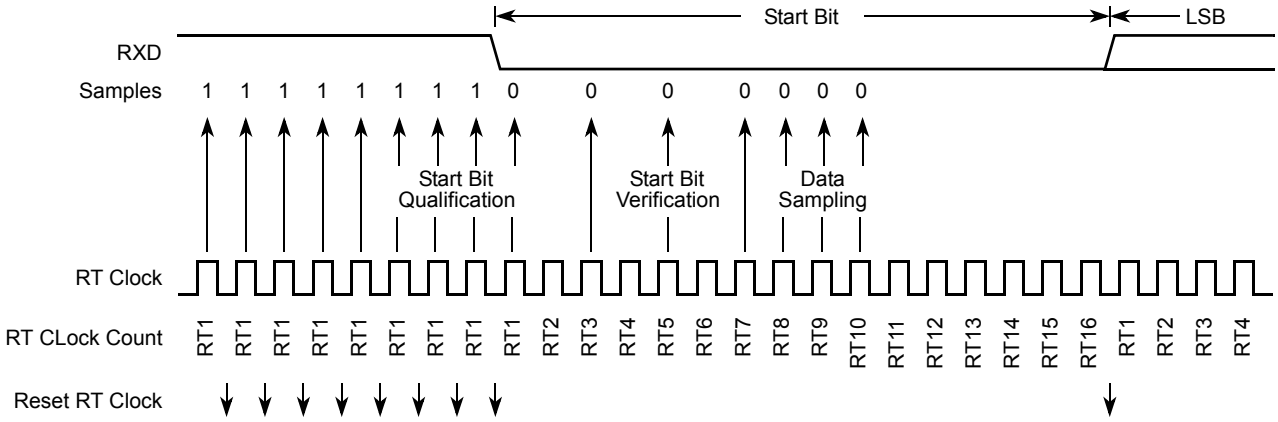


Figure 16-21. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Figure 16-17 summarizes the results of the start bit verification samples.

Table 16-17. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

drive the MOSI and SCK lines. In this case, the SPI immediately switches to slave mode, by clearing the MSTR bit and also disables the slave output buffer MISO (or SISO in bidirectional mode). So the result is that all outputs are disabled and SCK, MOSI, and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state.

This mode fault error also sets the mode fault (MODF) flag in the SPI status register (SPISR). If the SPI interrupt enable bit (SPIE) is set when the MODF flag becomes set, then an SPI interrupt sequence is also requested.

When a write to the SPI data register in the master occurs, there is a half SCK-cycle delay. After the delay, SCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI control register 1 (see Section 17.4.3, “Transmission Formats”).

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, XFRW, MODFEN, SPC0, or BIDIROE with SPC0 set, SPPR2-SPPR0 and SPR2-SPR0 in master mode will abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master must ensure that the remote slave is returned to idle state.

17.4.2 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI control register 1 is clear.

- Serial clock

  In slave mode, SCK is the SPI clock input from the master.

- MISO, MOSI pin

  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI control register 2.

- $\overline{SS}$ pin

  The $\overline{SS}$ pin is the slave select input. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be low. $\overline{SS}$ must remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state.

  The $\overline{SS}$ input also controls the serial data output pin, if $\overline{SS}$ is high (not selected), the serial data output pin is high impedance, and, if $\overline{SS}$ is low, the first bit in the SPI data register is driven out of the serial data output pin. Also, if the slave is not selected ($\overline{SS}$ is high), then the SCK input is ignored and no internal shifting of the SPI shift register occurs.

  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

NOTE

When peripherals with duplex capability are used, take care not to simultaneously enable two receivers whose serial outputs drive the same system slave’s serial data output line.

18.3.2.9 GDU Boost Current Limit Register (GDUBCL)

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GBCL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-11. GDU Boost Current Limit Register (GDUBCL)

1. Read: Anytime
   Write: Anytime if GWP=0

Table 18-12. GDU Boost Current Limit Register Field Descriptions

Field	Description
GBCL[3:0]	GDU Boost Current Limit Register— These bits are used to adjust the boost coil current limit $I_{COIL0,16}$ on the BST pin. These bits cannot be modified after GWP bit is set. See GDU electrical parameters.

18.3.2.10 GDU Phase Mux Register (GDUPHMUX)

Module Base + 0x0009 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	GPHMX[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-12. GDU Phase Mux Register (GDUPHMUX)

1. Read: Anytime
   Write: Anytime

Table 18-13. GDU Phase Mux Register Field Descriptions

Field	Description
[1:0] GPHMUX	GDU Phase Multiplexer — These buffered bits are used to select the voltage which is routed to internal ADC channel.The value written to the GDUPHMUX register does not take effect until the LDOK bit is set and the next PWM reload cycle begins. Reading GDUPHMUX register reads the value in the buffer. It is not necessary the value which is currently used. 00 Pin HD selected , V_{HD} / 12 connected to ADC channel 01 Pin HS0 selected , V_{HS0} / 6 connected to ADC channel 10 Pin HS1 selected , V_{HS1} / 6 connected to ADC channel 11 Pin HS2 selected, V_{HS2} / 6 connected to ADC channel

NOTE

Optional RC filter to VBS pin should be used to avoid overshoot above maximum voltage on VBS pin. The RC filter needs to be carefully designed in order not to influence the charging time of the bootstrap capacitor C_{BS}.

NOTE

GDUV4 and V6 does not include Bootstrap Transistor P1. It is only available on GDUV5. An external bootstrap diode is required for GDUV4 and V6.

On GDUV5 the bootstrap transistor P1 is turned on when the corresponding low-side driver is turned on and no high voltage condition on HD pin and no desaturation error is flagged.

18.4.4 Charge Pump

The GDU module integrates the necessary hardware to build a charge pump with external components.The charge pump is used to maintain the high-side driver gate source voltage V_{GS} when PWM is running at 100% duty cycle. The external components needed are capacitors and diodes The supply voltage of the charge pump driver on pin CP is $V_{VLS.}$ The output voltage on pin CP typically switches between 0 and 11V. The charge pump clock frequency depends on the setting of GCPCD bits.

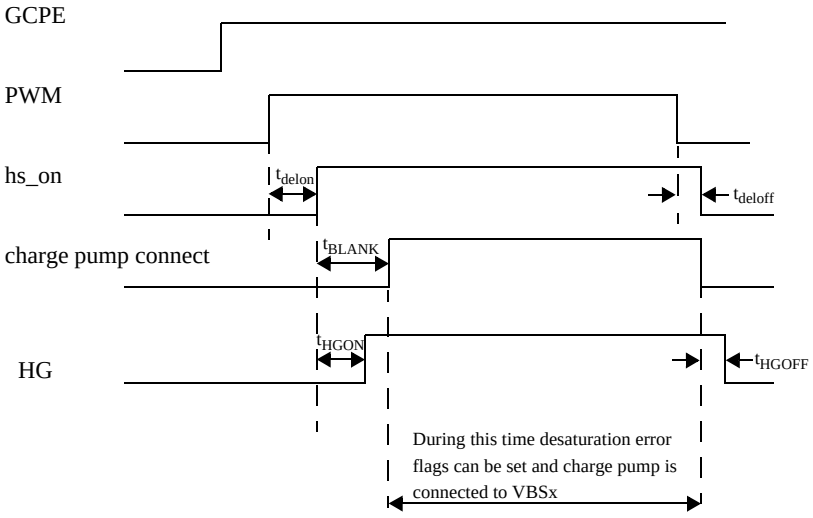
The transistor P2 shown in Figure 18-20 connects VCP pin to VBSx pin. Figure 18-21 shows the timing diagram when transistor P2 connects VCP to VBSx.

Figure 18-21. Timing Diagram Charge Pump Connect

t_{delon} / t_{deloff} : GDU propagation delay

t_{HGON} / t_{HGOFF} : HS driver turn on/off time

t_{BLANK}: Blanking Time (see GDUCTR register)



4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 20-54. Verify Backdoor Access Key Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0C	Not required
FCCOB1	Key 0	
FCCOB2	Key 1	
FCCOB3	Key 2	
FCCOB4	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0xFF_FE00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 20-55. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 20.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

20.4.7.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 20-56. Set User Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0D	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	

22.4 Functional Description

22.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of four clocks, clock A, Clock B, clock SA or clock SB.

The block diagram in Figure 22-15 shows the four different clocks and how the scaled clocks are created.

22.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode (freeze mode signal active) the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all available PWM channels are disabled (PWMEx-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

22.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

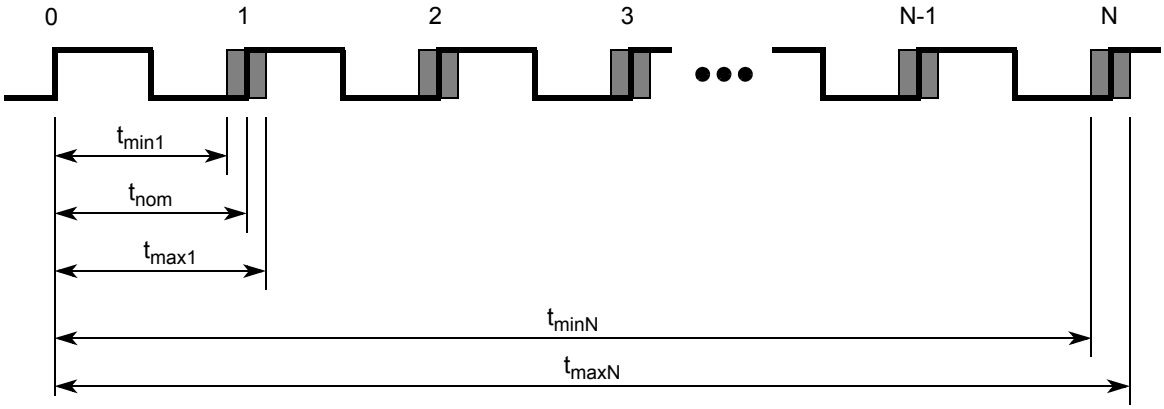


Figure B-1. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

The following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N(POSTDIV + 1)}}$$

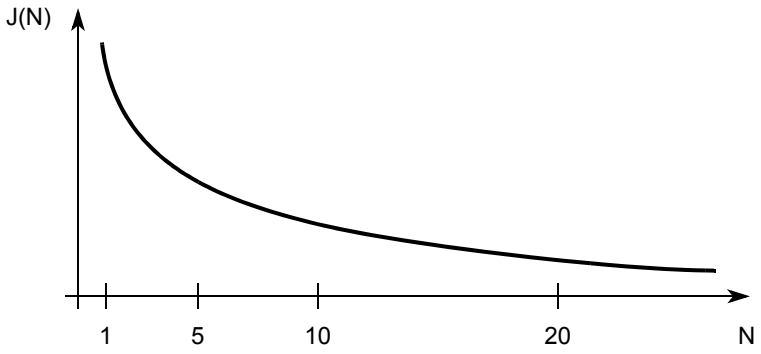


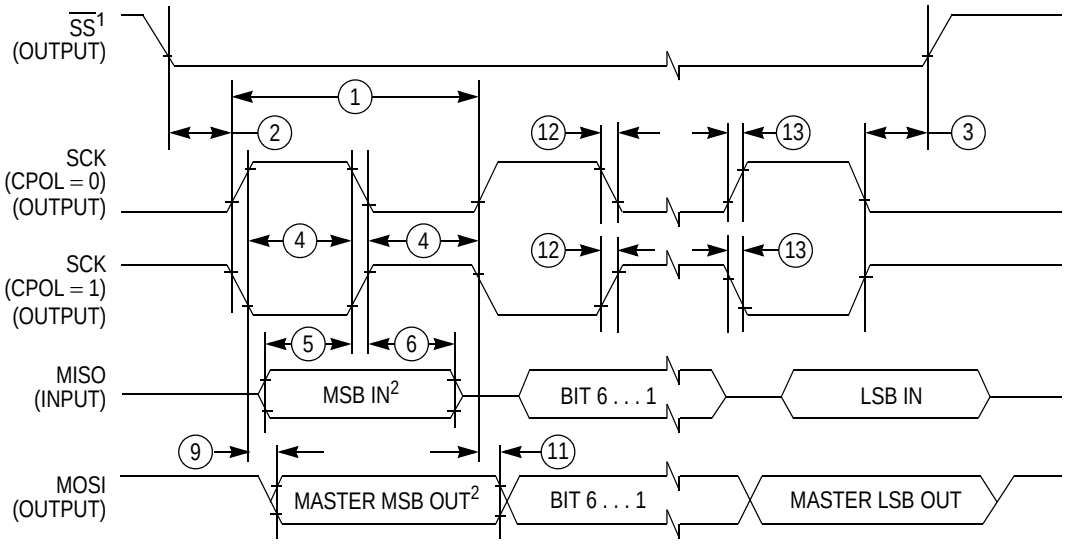
Figure B-2. Maximum Bus Clock Jitter Approximation (N = number of bus cycles)

3. For high side, the performance of external diodes may influence this parameter.
4. If VSUP is lower than 11.2V, external FET gate drive will diminish and roughly follow VSUP - 2* Vbe
5. Total gate charge spec is only a recommendation. FETs with higher gate charge can be used when resulting slew rates are tolerable by the application and resulting power dissipation does not lead to thermal overload.
6. Blanking time for assert (see device level mask set dependencies)
7. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 1V to 9V HGx/LGx vs HSx/LSx
8. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 9V to 1V HGx/LGx vs HSx/LSx
9. The delay is dependent on slew rate configuration. The variation on a given device for a given slew setting is much less than the specified range.
10. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V
11. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V, nmos branch only
12. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V, pmos branch only
13. Not tested on the mask set 2N95G, which does not feature the BST pin function
14. VLS > 6V
15. Output current range for which the effective output resistance specification applies
16. Input resistance can be calculated from the pin input leakage because the sense amp has high impedance MOS inputs
17. Av=10, no frequency compensation in feedback network, 90% output swing
18. Low side desaturation comparator range extends to LSx <= 2.35V - $V_{desatls}$

E.2 Preliminary GDU specifications for devices featuring GDU V5

Table E-2. GDUV5 Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
Num	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VSUP Supply range	V_{VSUP}	-0.3	—	40	V
2a	VSUP, HD Supply range FETs can be turned on(1) (normal range)	V_{VSUP}/V_{HD}	7	14	20	V
2b	VSUP, HD Supply range FETs can be turned on(2) (extended range)	V_{VSUP}/V_{HD}	7	14	26.6	V
3	External FET Vgs drive with boost(3) (7V < V_{RBATP} < 20V)	V_{VGS}	9	9.6	12	V
4	External FET Vgs drive without boost(4)	V_{VGS}	5	9.6	12	V
5	External FET total gate charge @ 10V(5)	QG	—	50	—	nC
6	Pull resistance between HGx and HSx	R_{HSpul}	60	80	120	KΩ
7	Pull resistance between LGx and LSx	R_{LSpul}	60	80	120	KΩ
8a	VLS output voltage for Vsup >=12.5V, Iout=30mA -40°C < T_j < 150°C	V_{VLS_OUT}	10.5	11	11.5	V
8b	VLS output voltage for Vsup >=12.5V, Iout=30mA 150°C < T_j < 175°C	V_{VLS_OUT}	10.0	10.6	11.5	V
9	VLS current limit threshold	I_{LIMVLS}	60	77	112	mA
10a	VLS low voltage monitor trippoint assert (GVLSLVL=1)	V_{LVLSHA}	6.2	6.5	7	V
10b	VLS low voltage monitor trippoint deassert (GVLSLVL=1)	V_{LVLSHD}	6.2	6.58	7	V
10c	VLS low voltage monitor trippoint assert (GVLSLVL=0)	V_{LVLSLA}	5.2	5.5	6	V
10d	VLS low voltage monitor trippoint deassert (GVLSLVL=0)	V_{LVLSLD}	5.2	5.55	6	V
11a	HD high voltage monitor assert trippoint low	V_{HVHDLA}	20	21	22	V
11b	HD high voltage monitor deassert trippoint low	V_{HVHDLD}	19.5	20.5	21.6	V
12a	HD high voltage monitor assert trippoint high	V_{HVHDHA}	26.6	28.3	29.4	V
12b	HD high voltage monitor deassert trippoint high	V_{HVHDHD}	26.2	27.9	29	V



1. If enabled.

2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-3. SPI Master Timing (CPHA=1)

Table I-1. SPI Master Mode Timing Characteristics (Junction Temperature From -40°C To +175°C)

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1		SCK Frequency	f_{sck}	1/2048	—	$1/2^{(1)(2)}$	f_{bus}
1		SCK Period	t_{sck}	2	—	2048	t_{bus}
2		Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3		Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4		Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5		Data Setup Time (Inputs)	t_{su}	4	—	—	ns
6		Data Hold Time (Inputs)	t_{hi}	5	—	—	ns
9		Data Valid after SCK Edge	t_{vsck}	—	—	10	ns
10		Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	9	ns
11		Data Hold Time (Outputs)	t_{ho}	-1.2	—	—	ns
12		Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13		Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1. See **Figure I-4.**

2. f_{bus} max is 40MHz at temperatures above 150°C

M.8 0x0400-0x042F TIM1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0400	TIM1TIOS	R W							IOS1	IOS0
0x0401	TIM1CFORC	R W							0 FOC1	0 FOC0
0x0402	Reserved	R W								
0x0403	Reserved	R W								
0x0404	TIM1TCNTH	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x0405	TIM1TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x0406	TIM1TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
0x0407	TIM1TTOV	R W							TOV1	TOV0
0x0408	TIM1TCTL1	R W								
0x0409	TIM1TCTL2	R W					OM1	OL1	OM0	OL0
0x040A	TIM1TCTL3	R W								
0x040B	TIM1TCTL4	R W					EDG1B	EDG1A	EDG0B	EDG0A
0x040C	TIM1TIE	R W							C1I	C0I
0x040D	TIM1TSCR2	R W	TOI	0	0	0		PR2	PR1	PR0
0x040E	TIM1TFLG1	R W							C1F	C0F
0x040F	TIM1TFLG2	R W	TOF	0	0	0	0	0	0	0
0x0410	TIM1TC0H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0411	TIM1TC0L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0