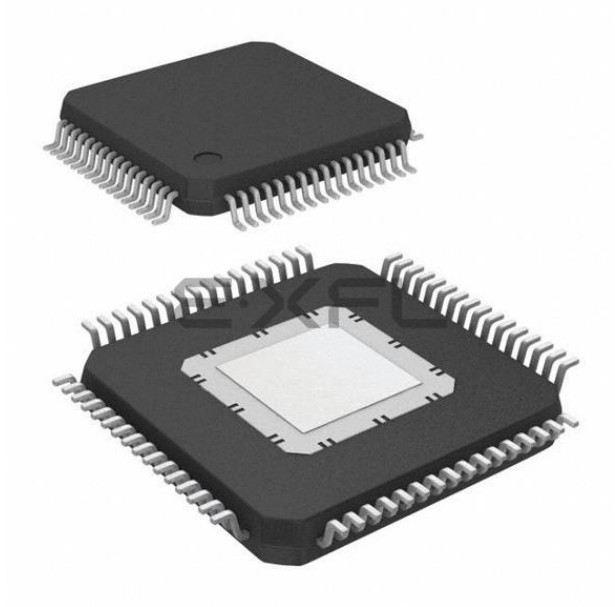

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Details	
Product Status	Active
Core Processor	S12Z
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Speed	50MHz
Connectivity	SCI, SPI
Peripherals	DMA, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvm16f1mkh

Chapter 11
Timer Module (TIM16B4CV3) Block Description

Chapter 12
Timer Module (TIM16B2CV3) Block Description

Chapter 13
Scalable Controller Area Network (S12MSCANV3)

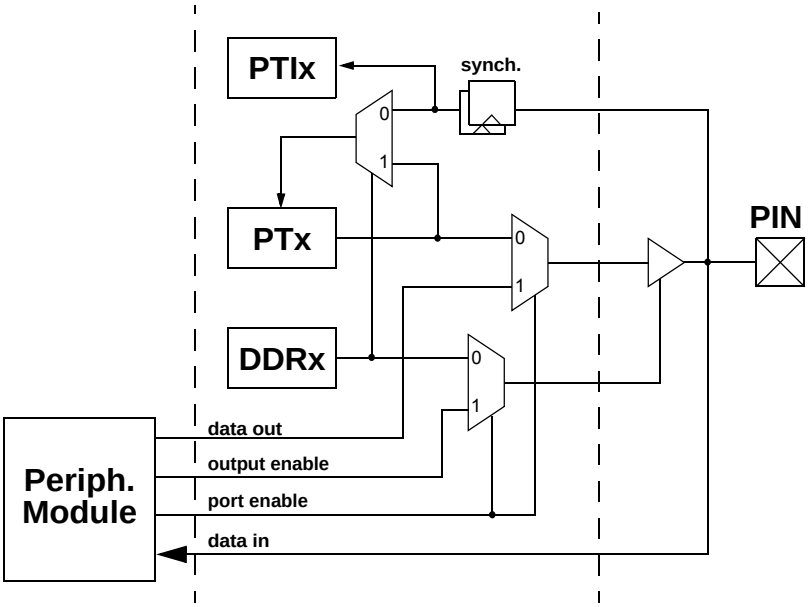

Figure 2-35. Illustration of I/O pin functionality

This section describes the interrupts generated by the PIM and their individual sources. Vector addresses and interrupt priorities are defined at MCU level.

Table 2-41. PIM Interrupt Sources

Module Interrupt Sources	Local Enable
$\overline{\text{XIRQ}}$	None
$\overline{\text{IRQ}}$	IRQCR[IRQEN]
Port AD pin interrupt	PIEADH[PIEADH7-PIEADH0] PIEADL[PIEADL7-PIEADL0]
Port S pin interrupt	PIES[PIES5-PIES0]
Port P pin interrupt	PIEP[PIEP2-PIEP0]
Port L pin interrupt	PIEL[PIEL0]
PP0 over-current interrupt	PIEP[OCIE1]

2.4.3.1 XIRQ, IRQ Interrupts

The $\overline{\text{XIRQ}}$ pin allows requesting non-maskable interrupts after reset initialization. During reset, the X bit in the condition code register is set and any interrupts are masked until software enables them.

The $\overline{\text{IRQ}}$ pin allows requesting asynchronous interrupts. The interrupt input is disabled out of reset. To enable the interrupt the IRQCR[IRQEN] bit must be set and the I bit cleared in the condition code register. The interrupt can be configured for level-sensitive or falling-edge-sensitive triggering. If IRQCR[IRQEN] is cleared while an interrupt is pending, the request will deassert.

NOTE

When a CPU indexed jump instruction is executed, the destination address is stored to the trace buffer on instruction completion, indicating the COF has taken place. If an interrupt occurs simultaneously then the next instruction carried out is actually from the interrupt service routine. The instruction at the destination address of the original program flow gets executed after the interrupt service routine.

In the following example an IRQ interrupt occurs during execution of the indexed JMP at address MARK1. The NOP at the destination (SUB_1) is not executed until after the IRQ service routine but the destination address is entered into the trace buffer to indicate that the indexed JMP COF has taken place.

```
         LD      X,#SUB_1
MARK1:   JMP     (0,X)                    ; IRQ interrupt occurs during execution of this
MARK2:   NOP                              ;

SUB_1:   NOP                              ; JMP Destination address TRACE BUFFER ENTRY 1
                                          ; RTI Destination address TRACE BUFFER ENTRY 3
         NOP                              ;
ADDR1:   DBNE    D0,PART5                 ; Source address TRACE BUFFER ENTRY 4

IRQ_ISR: LD      D1,#$F0                  ; IRQ Vector $FFF2 = TRACE BUFFER ENTRY 2
         ST      D1,VAR_C1
         RTI                              ;
```

The execution flow taking into account the IRQ is as follows

```
         LD      X,#SUB_1
MARK1:   JMP     (0,X)                    ;
IRQ_ISR: LD      D1,#$F0                  ;
         ST      D1,VAR_C1
         RTI                              ;
SUB_1:   NOP
         NOP                              ;
ADDR1:   DBNE    D0,PART5                 ;
```

The Normal Mode trace buffer format is shown in the following tables. Whilst tracing in Normal or Loop1 modes each array line contains 2 data entries, thus in this case the DBGCNT[0] is incremented after each separate entry. Information byte bits indicate if an entry is a source, destination or vector address.

The external event input can force trace buffer entries independent of COF occurrences, in which case the EEVI bit is set and the PC value of the last instruction is stored to the trace buffer. If the external event coincides with a COF buffer entry a single entry is made with the EEVI bit set.

Normal mode profiling with timestamp is possible when tracing from a single source by setting the STAMP bit in DBGTCRL. This results in a different format (see Table 6-49).

Table 6-48. Normal and Loop1 Mode Trace Buffer Format without Timestamp

Mode	8-Byte Wide Trace Buffer Line							
	7	6	5	4	3	2	1	0

7.2.2.5 ECC Debug Data (ECCDDH, ECCDDL)

Module Base + 0x000C — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DDATA[15:8]							
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read/write

	7	6	5	4	3	2	1	0
R W	DDATA[7:0]							
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-6. ECC Debug Data (ECCDDH, ECCDDL)

1. Read: Anytime
   Write: Anytime

Table 7-6. ECCDD Register Field Descriptions

Field	Description
DDATA [23:0]	ECC Debug Raw Data — This register contains the raw data which will be written into the system memory during a debug write command or the read data from the debug read command.

7.2.2.6 ECC Debug ECC (ECCDE)

Module Base + 0x000E — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	DECC[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime

Figure 7-7. ECC Debug ECC (ECCDE)

Table 7-7. ECCDE Field Description

Field	Description
5:0 DECC[5:0]	ECC Debug ECC — This register contains the raw ECC value which will be written into the system memory during a debug write command or the ECC read value from the debug read command.

Table 8-13. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$
0010 (÷3)	$3x10^3$	$6x10^3$	$15x10^3$	$30x10^3$	$60x10^3$	$150x10^3$	$300x10^3$	$600x10^3$
0011 (÷4)	$4x10^3$	$8x10^3$	$20x10^3$	$40x10^3$	$80x10^3$	$200x10^3$	$400x10^3$	$800x10^3$
0100 (÷5)	$5x10^3$	$10x10^3$	$25x10^3$	$50x10^3$	$100x10^3$	$250x10^3$	$500x10^3$	$1x10^6$
0101 (÷6)	$6x10^3$	$12x10^3$	$30x10^3$	$60x10^3$	$120x10^3$	$300x10^3$	$600x10^3$	$1.2x10^6$
0110 (÷7)	$7x10^3$	$14x10^3$	$35x10^3$	$70x10^3$	$140x10^3$	$350x10^3$	$700x10^3$	$1.4x10^6$
0111 (÷8)	$8x10^3$	$16x10^3$	$40x10^3$	$80x10^3$	$160x10^3$	$400x10^3$	$800x10^3$	$1.6x10^6$
1000 (÷9)	$9x10^3$	$18x10^3$	$45x10^3$	$90x10^3$	$180x10^3$	$450x10^3$	$900x10^3$	$1.8x10^6$
1001 (÷10)	$10\ x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$	$500x10^3$	$1x10^6$	$2x10^6$
1010 (÷11)	$11\ x10^3$	$22x10^3$	$55x10^3$	$110x10^3$	$220x10^3$	$550x10^3$	$1.1x10^6$	$2.2x10^6$
1011 (÷12)	$12x10^3$	$24x10^3$	$60x10^3$	$120x10^3$	$240x10^3$	$600x10^3$	$1.2x10^6$	$2.4x10^6$
1100 (÷13)	$13x10^3$	$26x10^3$	$65x10^3$	$130x10^3$	$260x10^3$	$650x10^3$	$1.3x10^6$	$2.6x10^6$
1101 (÷14)	$14x10^3$	$28x10^3$	$70x10^3$	$140x10^3$	$280x10^3$	$700x10^3$	$1.4x10^6$	$2.8x10^6$
1110 (÷15)	$15x10^3$	$30x10^3$	$75x10^3$	$150x10^3$	$300x10^3$	$750x10^3$	$1.5x10^6$	$3x10^6$
1111 (÷16)	$16x10^3$	$32x10^3$	$80x10^3$	$160x10^3$	$320x10^3$	$800x10^3$	$1.6x10^6$	$3.2x10^6$

Table 8-16. COP Watchdog Rates if COPOSCSEL1=1.

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is ACLK divided by 2)
0	0	0	COP disabled
0	0	1	2^{7}
0	1	0	2^{9}
0	1	1	2^{11}
1	0	0	2^{13}
1	0	1	2^{15}
1	1	0	2^{16}
1	1	1	2^{17}

8.3.2.26 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-37. Reserved Register CPMUTEST2

Read: Anytime

Write: Only in Special Mode

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ADCEOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0011	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	Reserved	Reserved					0	0
		W								
0x0014	ADCCMD_0 (V1)	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0014	ADCCMD_0 (V2, V3)	R	CMD_SEL		OPT[1:0]		INTFLG_SEL[3:0]			
		W								
0x0015	ADCCMD_1 (V1, V2)	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0015	ADCCMD_1 (V3)	R	VRH_SEL[1:0]		CH_SEL[5:0]					
		W								
0x0016	ADCCMD_2 (V1)	R	SMP[4:0]					0	0	Reserved
		W								
0x0016	ADCCMD_2 (V2, V3)	R	SMP[4:0]					OPT[3:2]		Reserved
		W								
0x0017	ADCCMD_3	R	Reserved	Reserved	Reserved					
		W								
0x0018	Reserved	R	Reserved							
		W								
0x0019	Reserved	R	Reserved							
		W								
0x001A	Reserved	R	Reserved							
		W								
0x001B	Reserved	R	Reserved							
		W								
0x001C	ADCCIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x001D	ADCCBP_0	R	CMD_PTR[23:16]							
		W								
0x001E	ADCCBP_1	R	CMD_PTR[15:8]							
		W								
0x001F	ADCCBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0020	ADCRIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0021	ADCRBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0022	ADCRBP_1	R	RES_PTR[15:8]							
		W								
0x0023	ADCRBP_2	R	RES_PTR[7:2]						0	0
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 2 of 3)

- Three complementary pairs and zero independent PWM outputs
- Zero complementary pairs and six independent PWM outputs

All PWM outputs can be generated from the same counter, or each pair can have its own counter for three independent PWM frequencies. Complementary operation permits programmable deadtime insertion, distortion correction through current sensing by software, and separate top and bottom output polarity control. Each counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width-control and full range modulation from 0 percent to 100 percent, are supported. The PMF is capable of controlling most motor types: AC induction motors (ACIM), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

15.1.1 Features

- Three complementary PWM signal pairs, or six independent PWM signals
- Edge-aligned or center-aligned mode
- Features of complementary channel operation:
  - — Deadtime insertion
  - — Separate top and bottom pulse width correction via current status inputs or software
  - — Three variants of PWM output:
    - – Asymmetric in center-aligned mode
    - – Variable edge placement in edge-aligned mode
    - – Double switching in center-aligned mode
- Three 15-bit counters based on core clock
- Separate top and bottom polarity control
- Half-cycle reload capability
- Integral reload rates from 1 to 16
- Programmable fault protection
- Link to timer output compare for 6-step BLDC commutation support with optional counter restart Reload overrun interrupt
- PWM compare output polarity control Software-controlled PWM outputs, complementary or independent

15.1.2 Modes of Operation

Care must be exercised when using this module in the modes listed in Table 15-4. Some applications require regular software updates for proper operation. Failure to do so could result in destroying the hardware setup. Because of this, PWM outputs are placed in their inactive states in STOP mode, and optionally under WAIT and FREEZE modes. PWM outputs will be reactivated (assuming they were active to begin with) when these modes are exited.

15.4.2 Prescaler

To permit lower PWM frequencies, the prescaler produces the PWM clock frequency by dividing the core clock frequency by one, two, four, and eight. Each PWM generator has its own prescaler divisor. Each prescaler is buffered and will not be used by its PWM generator until the corresponding Load OK bit is set and a new PWM reload cycle begins.

15.4.3 PWM Generator

Each PWM generator contains a 15-bit up/down PWM counter producing output signals with software-selectable

- Alignment — The logic state of each pair EDGE bit determines whether the PWM pair outputs are edge-aligned or center-aligned
- Period — The value written to each pair PWM counter modulo register is used to determine the PWM pair period. The period can also be varied by using the prescaler
- With edge-aligned output, the modulus is the period of the PWM output in clock cycles
- With center-aligned output, the modulus is one-half of the PWM output period in clock cycles
- Pulse width — The number written to the PWM value register determines the pulse width duty cycle of the PWM output in clock cycles
  - — With center-aligned output, the pulse width is twice the value written to the PWM value register
  - — With edge-aligned output, the pulse width is the value written to the PWM value register

15.4.3.1 Alignment and Compare Output Polarity

Each edge-align bit, EDGEx, selects either center-aligned or edge-aligned PWM generator outputs.

PWM compare output polarity is selected by the CINV*n* bit field in the source control (PMFCINV) register. Please see the output operations in Figure 15-42 and Figure 15-43.

The PWM compare output is driven to a high state when the value of PWM value (PMFVAL*n*) register is greater than the value of PWM counter, and PWM compare is counting downwards if the corresponding channel CINV*n*=0. Or, the PWM compare output is driven to low state if the corresponding channel CINV*n*=1.

The PWM compare output is driven to low state when the value of PWM value (PMFVAL*n*) register matches the value of PWM counter, and PWM counter is counting upwards if the corresponding channel CINV*n*=0. Or, the PWM compare output is driven to high state if the corresponding channel CINV*n*=1.

Table 16-11. SCISR1 Field Descriptions (continued)

Field	Description
3 OR	**Overrun Flag** — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL). 0 No overrun 1 Overrun **Note:** OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs: 1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear); 2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set); 3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register); 4. Read status register SCISR1 (returns RDRF clear and OR set). Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received.
2 NF	**Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL). 0 No noise 1 Noise
1 FE	**Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	**Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

16.5.3.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI Interrupt Signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

16.5.3.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

16.5.3.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. Transmission is completed when all bits including the stop bit (if transmitted) have been shifted out and no data is queued to be transmitted. No stop bit is transmitted when sending a break character and the TC flag is set (providing there is no more data queued for transmission) when the break character has been shifted out. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

16.5.3.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. Once the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0007 Reserved	R								
	W								

= Unimplemented or Reserved

Figure 17-2. SPI Register Summary

17.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

17.3.2.1 SPI Control Register 1 (SPICR1)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R W	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

Figure 17-3. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

Table 17-2. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.

Chapter 18
Gate Drive Unit (GDU)

Table 18-1. Revision History Table

Version Number	Revision Date	Description of Changes
V6 Initial Draft	25-January-2015	Initial Draft based on GDUV4/V5 with following changes for SR Motor support: • additional drain connections LD[2:0] for SR motor drive • GDUCTR1 register with control bits for SR motor drive • Removed EPRES control bit functionality for V5 and V6 • Changed GSUF startup flag functionality for V6
V6	28-January-2016	• Removed EPRES Functionality • Common specification for GSUF with reference to device overview • Common specification for GDUCTR1 with reference to device overview
V6.1	4-February-2016	• Corrected Table 1-2 TDEL availability and low-side driver on or off out of reset dependent on NVM option for GDU V4
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation comparator filter time constant (relocated in electrical spec.)
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation

18.1 Differences GDUV4 vs GDUV5 vs GDUV6

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
TDEL control bit for t_{delon}/t_{deloff}	available[1.]	not available	available
Number of Overcurrent threshold bits for overcurrent comparator 0/1	GOCT0[3:0] , GOCT1[3:0]	GOCT0[4:0] , GOCT1[4:0]	GOCT0[4:0], GOCT1[4:0]
VLS level select control bit GVLSLVL	not available	available	available
Current sense amplifier offset	adjustable in 5mV steps	adjustable in 3mV steps	adjustable in 3mV steps

Table 18-15. GDU Desaturation Level Register Field Descriptions

Field	Description
7 GDSFHS (Not featured on GDUV4)	GDU Desaturation Filter Characteristic for High-Side Drivers — This bit adjusts the desaturation filter characteristic of the three high-side FET pre-drivers. These bits cannot be modified after GWP bit is set. See Section 18.4.5, “Desaturation Error.
6:4 GDSLHS	GDU Desaturation Level for High-Side Drivers — These bits adjust the desaturation levels of the three high-side FET pre-drivers. These bits cannot be modified after GWP bit is set. See Section 18.4.5, “Desaturation Error 000 $V_{desaths} = V_{HD}$ - 0.35V (typical value) 001 to 110 see device electrical specification 111 $V_{desaths} = V_{HD}$ - 1.40V (typical value)
3 GDSFLS (Not featured on GDUV4)	GDU Desaturation Filter Characteristic for Low-Side Drivers — This bit adjusts the desaturation filter characteristic of the three low-side FET pre-drivers. These bits cannot be modified after GWP bit is set. See Section 18.4.5, “Desaturation Error.
2:0 GDSLLS	GDU Desaturation Level for Low-Side Drivers — These bits adjust the desaturation level of the three low-side FET pre-drivers. These bits cannot be modified after GWP bit is set. See Section 18.4.5, “Desaturation Error 000 $V_{desatls}$ = 0.35V (typical value) 001 to 110 see device electrical specification 111 $V_{desatls}$ = 1.40V (typical value)

19.2 External Signal Description

This section lists and describes the signals that connect off chip as well as internal supply nodes and special signals.

19.2.1 LIN — LIN Bus Pin

This pad is connected to the single-wire LIN data bus.

19.2.2 LGND — LIN Ground Pin

This pin is the device LIN ground connection. It is used to sink currents related to the LIN Bus pin. A de-coupling capacitor external to the device (typically 220 pF, X7R ceramic) between LIN and LGND can further improve the quality of this ground and filter noise.

19.2.3 VLINSUP — Positive Power Supply

External power supply to the chip. The VLINSUP supply mapping is described in device level documentation.

19.2.4 LPTxD — LIN Transmit Pin

This pin can be routed to the SCI, LPDR1 register bit, an external pin, or other options. Please refer to the PIM chapter of the device specification for the available routing options.

In the HV Phy version, LPTxD can be used to send diagnostic feedback.

This input is only used in normal mode; in other modes the value of this pin is ignored.

19.2.5 LPRxD — LIN Receive Pin

This pin can be routed to the SCI, an external pin, or other options like a timer. Please refer to the PIM chapter of the device specification for the available routing options.

In the HV Phy version, LPRxD can be used to receive control information since it can be connected to an internal timer channel.

In standby mode this output is disabled, and sends only a short pulse in case the wake-up functionality is enabled and a valid wake-up pulse was received in the LIN Bus.

19.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the LIN/HV Physical Layer.

19.3.1 Module Memory Map

A summary of the registers associated with the LIN/HV Physical Layer module is shown in Table 19-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Appendix A
MCU Electrical Specifications

A.1 General

This section contains the most accurate electrical information available at the time of publication.

A.1.1 Parameter Classification

The electrical parameters shown in the appendices are guaranteed by various methods.

The parameter classification is documented in the PPAP.

The parameter classification columns are for NXP internal use only.

Table A-10. 64LQFP-EP Typical Thermal Package Characteristics (All other devices)

Num	C[1]	Rating	Symbol	masksets 1N95G, 2N95G	maskset 3N95G	Unit
1		Thermal resistance 64LQFP-EP, single sided PCB[2] Natural Convection	θ_{JA}	69	58	°C/W
2		Thermal resistance 64LQFP-EP, double sided PCB[2] with 2 internal planes. Natural Convection.	θ_{JA}	31	28	°C/W
3		Thermal resistance 64LQFP-EP, single sided PCB[3] (@200 ft./min)	θ_{JA}	56	46	°C/W
4		Thermal resistance 64LQFP-EP, double sided PCB[3] with 2 internal planes (@200 ft./min).	θ_{JA}	26	22	°C/W
5		Junction to Board 64LQFP-EP[4]	θ_{JB}	15	11	°C/W
6		Junction to Case Top 64LQFP-EP[5]	θ_{JCtop}	18	14	°C/W
7		Junction to Case Bottom 64LQFP-EP[6]	$\theta_{JCbottom}$	1.7	1.4	°C/W
8		Junction to Package Top 64LQFP-EP[7]	Ψ_{JT}	4	3	°C/W

1. The values for thermal resistance are achieved by package simulations
2. Junction to ambient thermal resistance. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively
3. Junction to ambient thermal resistance. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. A single layer board is used for this simulation.

Table H-2. Static Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
5	Input Resistance	R_{IN}	5	32.5	50	kΩ
6	Differential Input Resistance	R_{IND}	10	65	100	kΩ
7	Common mode input resistance matching	R_{INM}	-3	0	+3	%
8	CANH Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{CANH}	 2.75 2.0	 3.5 2.5	 4.5 3.0	 V V
9	CANL Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{CANL}	 0.5 2.0	 1.5 2.5	 2.25 3.0	 V V
10	Differential Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{OH} - V_{OL}	 1.5 -0.5	 2.0 0	 3.0 0.05	 V V
11	CANH, CANL driver symmetry (Normal mode) (V_{CANH} + V_{CANL}) / VDDC	V_{SYM}	0.9	1	1.1	—
12	Output Current Capability (Dominant State) CANH CANL	 I_{CANH} I_{CANL}	 —	 55 55	 —	 mA mA
13	CANH, CANL Overcurrent Detection (Tj >=25^{O}C) CANH CANL	 I_{CANHOC} I_{CANLOC}	 70 70	 85 85	 100 100	 mA mA
14	CANH, CANL Output Voltage (no load, Standby mode) CANH CANL	 V_{CANH} V_{CANL}	 -0.1 -0.1	 0 0	 0.1 0.1	 V V
15	CANH and CANL Input Current (Standby mode) V_{CANH}, V_{CANL} from 0 V to 5.0 V V_{CANH}, V_{CANL} = - 2.0 V V_{CANH}, V_{CANL} = 7.0 V	I_{CAN1}	—	—	20 -75 250	uA uA uA
16	CANH and CANL Input Current (Device unsupplied) (VSUP tied to ground or left open) V_{CANH}, V_{CANL} from 0V to 5 V V_{CANH}, V_{CANL} = - 2.0 V V_{CANH}, V_{CANL} = 7.0 V	I_{CAN2}	—	—	10 -75 250	uA uA uA
17	CANH, CANL Input capacitance (Normal mode) CANH CANL	 C_{CANH} C_{CANL}	 —	 14 16	 —	 pF pF
18	CANH to CANL differential capacitance (Normal mode)	C_{HLDIFF}	—	6	—	pF
DIAGNOSTIC INFORMATION (CANH AND CANL)						
15	CANL to 0 V Threshold	V_{L0}	-0.75	-0.15	0	V
16	CANH to 0 V Threshold	V_{H0}	-0.75	-0.15	0	V

M.12 0x05C0-0x05FF TIM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05D2	TIM0TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D3	TIM0TC1L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D4	TIM0TC2H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D5	TIM0TC2L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D6	TIM0TC3H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D7	TIM0TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D8– 0x05DF	Reserved	R W								
0x05E0	Reserved	R W								
0x05E1	Reserved	R W								
0x05E2	Reserved	R W								
0x05E3	Reserved	R W								
0x05E4– 0x05EB	Reserved	R W								
0x05EC	TIM0OCPD	R W					OCPD3	OCPD2	OCPD1	OCPD0
0x05ED	Reserved	R W								
0x05EE	TIM0PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x05EF	Reserved	R W								