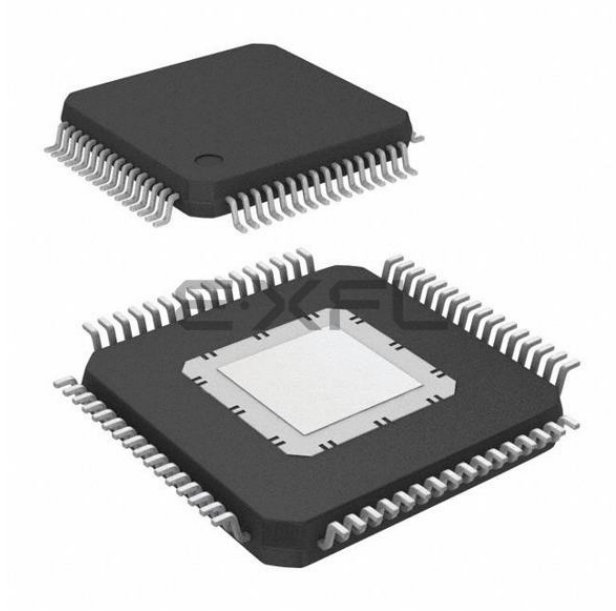

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	SCI, SPI
Peripherals	DMA, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvm16f1mkhr

Table 0-1. Revision History

Date	Revision	Description
20 NOV 2015	2.3	Added devices to Part ID list Table 1-6 Added explanation of GSUF dependency on xN14N mask set Table 1-19 Minor corrections to reset source and interrupt vector tables Table 1-15 Added device level POR information Figure 1-8 Minor correction to PIM chapter Added constraints to EXTCON, SCS2 and SCS1 bits in CPMU chapter Added PMF version difference table Table 15-3 Corrected footnotes and parameter spelling in GDU register summary Noted GDU sense amplifier dependence on GFDE bit Documented that flash option (FOPT) register can be written in special mode Added pulsed absolute maximum rating for HSx pins Table A-2 Extended VDDS1 and VDDS2 maximum ratings Table A-2 Added thermal resistance parameter values for 80LQFP-EP package Added VREG configuration to Run/Wait/Stop current measurement configurationTable A-16 Removed de-saturation thresholds from electrical spec. tables Added footnote for GDU tdelon/tdeloff electrical parameters Added max. and min. values for GDU HD signal division through phase mux. Removed incorrect limit from BATS electrical parameter table headers Extended CANPHY maximum ratings to 175°C Updated SRAM_ECC chapter to cover ZVMC256 Minor correction to PMF chapter Updated typical Stop IDD and Pseudo Stop IDD values for ZVMC256 based on validation data Added ZVMC256 parameter for Stop IDD with CANPHY and API enabled Table A-19 Renamed bit GSLEWMOD to TDEL (GDU V6). Removed GSLEWMOD bit (GDU V5) Noted temperature sensor slope is subject to further characterization
14 DEC 2015	2.4	Added T1IC0RR to PIM MODRR2 register Updated temperature sensor electrical specification, Table B-1 Added GDU current sense amp unity bandwidth parameter Table E-1, Table E-2 Added GDU current sense input resistance footnote Table E-1, Table E-2
14 JAN 2016	2.5	Clarified non production mask sets Table 1-4, Table 1-6 Updated ordering information in Appendix L Changed RESET pin input pulse passed parameter minimum specification value.Table A-13 Replaced Freescale with NXP in logo and page footers Added maximum value for GDU parameter VBSx current whilst high side inactive Table E-2
07 MAR 2016	2.6	Added 3N95G mask set information Table 1-19, Table 1-4, Table 1-6 Added list of ISO26262 compliant devices Moved GDU mask set dependent features to device overview section Table 1-19 Added new 64LQFP-EP package diagrams Table K.2 Added minimum value for GDU parameter VBSx current whilst high side inactive Table E-2 Updated V_{CSAoff} parameter limits for GDU V5 and GDU V6 Table E-1, Table E-2 Added ADCCMD1[7:6] device dependencies in register listing Section M.13, Section M.14 Simplified GDU device dependencies in register listing Section M.15 Corrected High Temperature Interrupt spec. (cannot wake up from STOP) Table 1-16 Added footnote to Table A-14 ZVMC256: added typical Run/Wait IDD values, updated 85°C Stop IDD Table A-18, Table A-19 Added bootstrap diode resistance parameter Table E-2 Updated GDU boost coil current limit specification Table E-2, Table E-1 Reverted to original current sense amp. offset values Table E-2, Table E-1 Added package to mask set mapping table Table K-1
08 MAR 2016	2.7	Changed maximum value of V_{BSTOFF} Table E-2, Table E-1 Updated 48LQFP-EP Mechanical Information Diagram Section K.1

Table 2-11. MODRR1 Routing Register Field Descriptions

Field	Description
7-5 M0C0RR2-0	**Module Routing Register** — MSCAN0-CANPHY0 routing Selection of MSCAN0-CANPHY0 interface routing options to support probing and conformance testing. Refer to Figure 2-4 for an illustration and Table 2-12 for preferred settings. MSCAN0 must be enabled for TXCAN0 routing to take effect on pin. CANPHY0 must be enabled for CPRXD0 and CP0DR[CPDR1] routings to take effect on pins.
4-3 PWMPRR1-0	**Module Routing Register** — PMF probe Internal PMF outputs can be probed on related external pins. Probing can be enabled independent of the PWM54RR, PWM32RR, and PWM10RR settings. 11 PMF channels 1, 3, 5 connected to related PWM1_x pins (only available for ZVMC256) 10 PMF channels 0, 2, 4 connected to related PWM1_x pins (only available for ZVMC256) 01 All PMF channels connected to related PWM1_x pins 00 No PMF channels connected to related PWM1_x pins
2 PWM54RR	**Module Routing Register** — PWM1_4 and PWM1_5 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_4 to PT1; PWM1_5 to PT2 (PP0 for S12ZVMC256) 0 PWM1_4 to GDU; PWM1_5 to GDU
1 PWM32RR	**Module Routing Register** — PWM1_2 and PWM1_3 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_2 to PP2 (PT3 for S12ZVMC256); PWM1_3 to PT0 0 PWM1_2 to GDU; PWM1_3 to GDU
0 PWM10RR	**Module Routing Register** — PWM1_0 and PWM1_1 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_0 to PP0 (PT2 for S12ZVMC256); PWM1_1 to PP1 0 PWM1_0 to GDU; PWM1_1 to GDU

2.3.3.2 Port Input Register

Address 0x0262 PTIE
0x0282 PTIADH
0x0283 PTIADL
0x02C1 PTIT
0x02D1 PTIS
0x02F1 PTIP

Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIx7	PTIx6	PTIx5	PTIx4	PTIx3	PTIx2	PTIx1	PTIx0
W								
Reset	-	-	-	-	-	-	-	-

Figure 2-13. Port Input Register

1. Read: Anytime
Write:Never

This is a generic description of the standard port input registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-18. Port Input Register Field Descriptions

Field	Description
7-0 PTIx7-0	**Port Input** — Data input A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.3.3 Data Direction Register

Address 0x0264 DDRE
0x0284 DDRADH
0x0285 DDRADL
0x02C2 DDRT
0x02D2 DDRS
0x02F2 DDRP

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRx7	DDRx6	DDRx5	DDRx4	DDRx3	DDRx2	DDRx1	DDRx0
Reset	0	0	0	0	0	0	0	0

Figure 2-14. Data Direction Register

1. Read: Anytime
Write: Anytime

This is a generic description of the standard data direction registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

2.3.3.9 Reduced Drive Register

Address 0x02FD RDRP — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	RDRx7	RDRx6	RDRx5	RDRx4	RDRx3	RDRx2	RDRx1	RDRx0
Reset	0	0	0	0	0	0	0	0

Figure 2-20. Reduced Drive Register

1. Read: Anytime
   Write: Anytime

This is a generic description of the standard reduced drive registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-25. Reduced Drive Register Field Descriptions

Field	Description
7-0 RDRx7-0	**Reduced Drive Register** — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/10 of the full drive strength) 0 Full drive strength enabled

2.3.3.10 Wired-Or Mode Register

Address 0x02DF WOMS — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	WOMx7	WOMx6	WOMx5	WOMx4	WOMx3	WOMx2	WOMx1	WOMx0
Reset	0	0	0	0	0	0	0	0

Figure 2-21. Wired-Or Mode Register

1. Read: Anytime
   Write: Anytime

This is a generic description of the standard wired-or registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

the BDCCSRL status byte is returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted. The effect of the access size and alignment on the next address to be accessed is explained in more detail in Section 5.4.5.2”.

NOTE

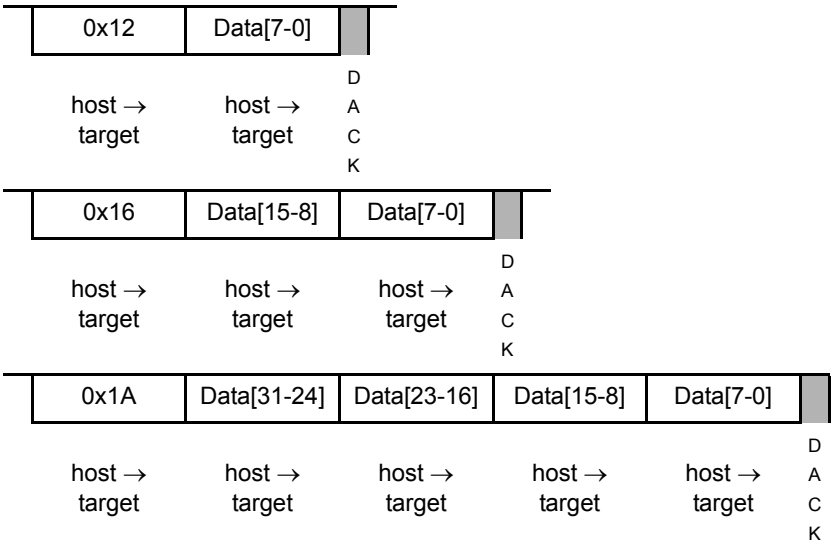
DUMP_MEM{_WS} is a valid command only when preceded by SYNC, NOP, READ_MEM{_WS}, or another DUMP_MEM{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter-command padding without corrupting the address pointer.

The size field (sz) is examined each time a DUMP_MEM{_WS} command is processed, allowing the operand size to be dynamically altered. The examples show the DUMP_MEM.B{_WS}, DUMP_MEM.W{_WS} and DUMP_MEM.L{_WS} commands.

5.4.4.6 FILL_MEM.sz, FILL_MEM.sz_WS

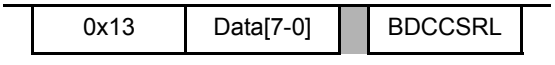
FILL_MEM.sz

Write memory specified by debug address register, then increment address — **Non-intrusive**



FILL_MEM.sz_WS

Write memory specified by debug address register with status, then increment address — **Non-intrusive**



The number of core clock cycles since the last entry equals the timestamp + 1. The core clock runs at twice the frequency of the bus clock. The timestamp of the first trace buffer entry is 0x0000. With timestamps enabled trace buffer entries are initiated in the following ways:

- according to the trace mode specification, for example COF PC addresses in Normal mode
- on a timestamp counter overflow
  If the timestamp counter reaches 0xFFFF then a trace buffer entry is made, with timestamp= 0xFFFF and the timestamp overflow bit TOVF is set.
- on a match of comparator D
  If STAMP and DSTAMP are set then comparator D is used for forcing trace buffer entries with timestamps. The state control register settings determine if comparator D is also used to trigger the state sequencer. Thus if the state control register configuration does not use comparator D, then it is used solely for the timestamp function. If comparator D initiates a timestamp then the CTI bit is set in the INFO byte. This can be used in Normal/Loop1 mode to indicate when a particular data access occurs relative to the PC flow. For example when the timing of an access may be unclear due to the use of indexes.

NOTE

If comparator D is configured to match a PC address then associated timestamps trigger a trace buffer entry during execution of the previous instruction. Thus the PC stored to the trace buffer is that of the previous instruction.The comparator must contain the PC address of the instruction's first opcode byte

Timestamps are disabled in Pure PC mode.

6.4.5.4 Reading Data from Trace Buffer

The data stored in the trace buffer can be read using either the background debug controller (BDC) module or the CPU provided the DBG module is not armed and is configured for tracing by TSOURCE. When the ARM bit is set the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by an aligned word write to DBGTB when the module is disarmed. The trace buffer can only be read through the DBGTB register using aligned word reads. Reading the trace buffer while the DBG module is armed, or trace buffer locked returns 0xEE and no shifting of the RAM pointer occurs. Any byte or misaligned reads return 0xEE and do not cause the trace buffer pointer to increment to the next trace buffer address.

Reading the trace buffer is prevented by internal hardware whilst profiling is active because the RAM pointer is used to indicate the next row to be transmitted. Thus attempted reads of DBGTB do not return valid data when the PTACT bit is set. To initialize the pointer and read profiling data, the PTACT bit must be cleared and remain cleared.

The trace buffer data is read out first-in first-out. By reading CNT in DBGCNT the number of valid 64-bit lines can be determined. DBGCNT does not decrement as data is read.

Whilst reading, an internal pointer is used to determine the next line to be read. After a tracing session, the pointer points to the oldest data entry, thus if no overflow has occurred, the pointer points to line0. The

8.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V10_V6.

8.3.1 Module Memory Map

The S12CPMU_UHV_V10_V6 registers are shown in Figure 8-5.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPMU RESERVED00	R	0	0	0	0	0	0	0	0
		W								
0x0001	RESERVED	R	0	0	0	0	U	U	U	U
	CPMU VREGTRIM0	W								
0x0002	RESERVED	R	0	0	U	U	U	0	0	0
	CPMU VREGTRIM1	W								
0x0003	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x0004	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0005	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0006	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0007	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x0008	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0009	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x000A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x000B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x000C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x000D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 8-5. CPMU Register Summary

9.5.2.23 ADC Command and Result Offset Register 0 (ADCCROFF0)

Module Base + 0x0024

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF0[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-26. ADC Command and Result Offset Register 0 (ADCCROFF0)

Read: Anytime

Write: NA

Table 9-31. ADCCROFF0 Field Descriptions

Field	Description
6-0 CMDRES_OFF0[6:0]	**ADC Command and Result Offset Value** — These read only bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_0 and RVL_0. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. This is a zero offset (null offset) which can not be modified. These bits do not represent absolute addresses instead it is a sample offset (object size 16bit for RVL, object size 32bit for CSL). See also Section 9.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

– *Function:*
Start the first conversion of a conversion sequence which is defined in the active Command Sequence List

– *Requested by:*
- Positive edge of internal interface signal Trigger
- Write Access via data bus to set control bit TRIG

– *When finished:*
This bit is cleared by the ADC when the first conversion of the sequence is beginning to sample

– *Mandatory Requirements:*
- In all ADC conversion flow control modes bit TRIG is only set (Trigger Event executed) if the Trigger Event occurs while no conversion or conversion sequence is ongoing (ADC idle)
- In ADC conversion flow control mode “Restart Mode” with a Restart Event in progress it is not allowed that a Trigger Event occurs before the background command load phase has finished (Restart Event has been executed) else the error flag TRIG_EIF is set
- In ADC conversion flow control mode “Trigger Mode” a Restart Event causes bit TRIG being set automatically. Bit TRIG is set when no conversion or conversion sequence is ongoing (ADC idle) and the RVL done condition is reached by one of the following:
* A “End Of List” command type has been executed
* A Sequence Abort Event is in progress or has been executed
The ADC executes the Restart Event followed by the Trigger Event.
- In ADC conversion flow control mode “Trigger Mode” a Restart Event and a simultaneous Trigger Event via internal interface or data bus causes the TRIG_EIF bit being set and ADC cease operation.

• **Restart Event** (with current active CSL)
Internal Interface Signal: Restart
Corresponding Bit Name: RSTA

– *Function:*
- Go to top of active CSL (clear index register for CSL)
- Load one background command register and wait for Trigger (CSL offset register is not switched independent of bit CSL_BMOD)
- Set error flag RSTA_EIF when a Restart Request occurs before one of the following conditions was reached:
* The "End Of List" command type has been executed
* Depending on bit STR_SEQA if the "End Of List" command type is about to be executed
* The current CSL has been aborted or is about to be aborted due to a Sequence Abort Request.

– *Requested by:*
- Positive edge of internal interface signal Restart
- Write Access via data bus to set control bit RSTA

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-19. MSCAN Transmit Error Counter (CANTXERR)

1. Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
   Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

13.3.2.17 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 13.3.3.1, “Identifier Registers (IDR0–IDR3)”) of incoming messages in a bit by bit manner (see Section 13.4.3, “Identifier Acceptance Filter”).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 to Module Base + 0x0013 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 13-20. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

15.3.2.31 PMF Counter C Register (PMFCNTC)

Address: Module Base + 0x0032 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFCNTC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-36. PMF Counter C Register (PMFCNTC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Never

This register displays the state of the 15-bit PWM C counter.

15.3.2.32 PMF Counter Modulo C Register (PMFMODC)

Address: Module Base + 0x0034 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFMODC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-37. PMF Counter Modulo C Register (PMFMODC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKC bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODC returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

15.3.2.33 PMF Deadtime C Register (PMFDTMC)

Address: Module Base + 0x0036 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMC											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 15-38. PMF Deadtime C Register (PMFDTMC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.This register cannot be modified after the WP bit is set.

16.4.6 Receiver

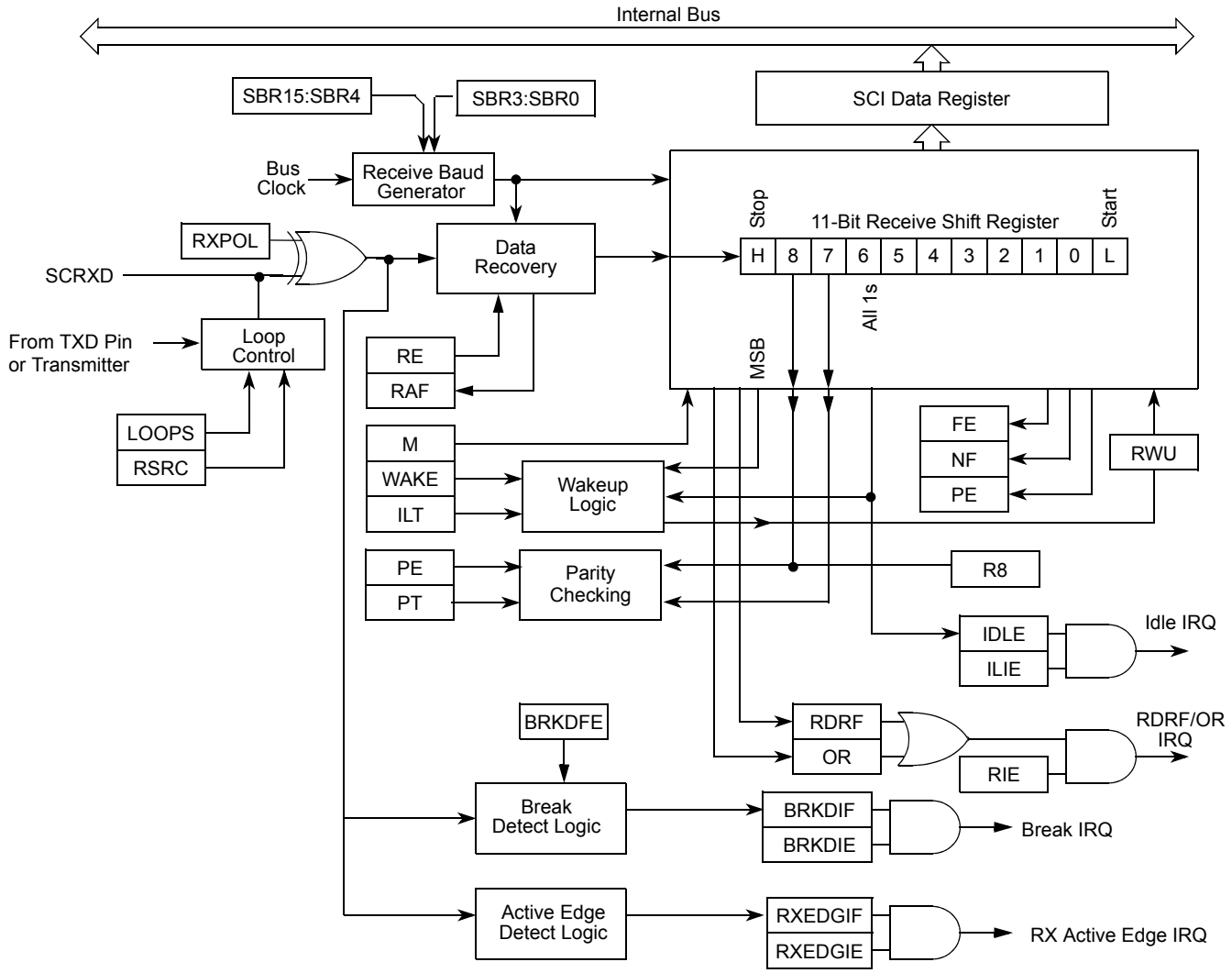


Figure 16-20. SCI Receiver Block Diagram

16.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

16.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

To re-enable the transmitter then, the LPDTIF flag must be cleared (by writing a 1).

NOTE

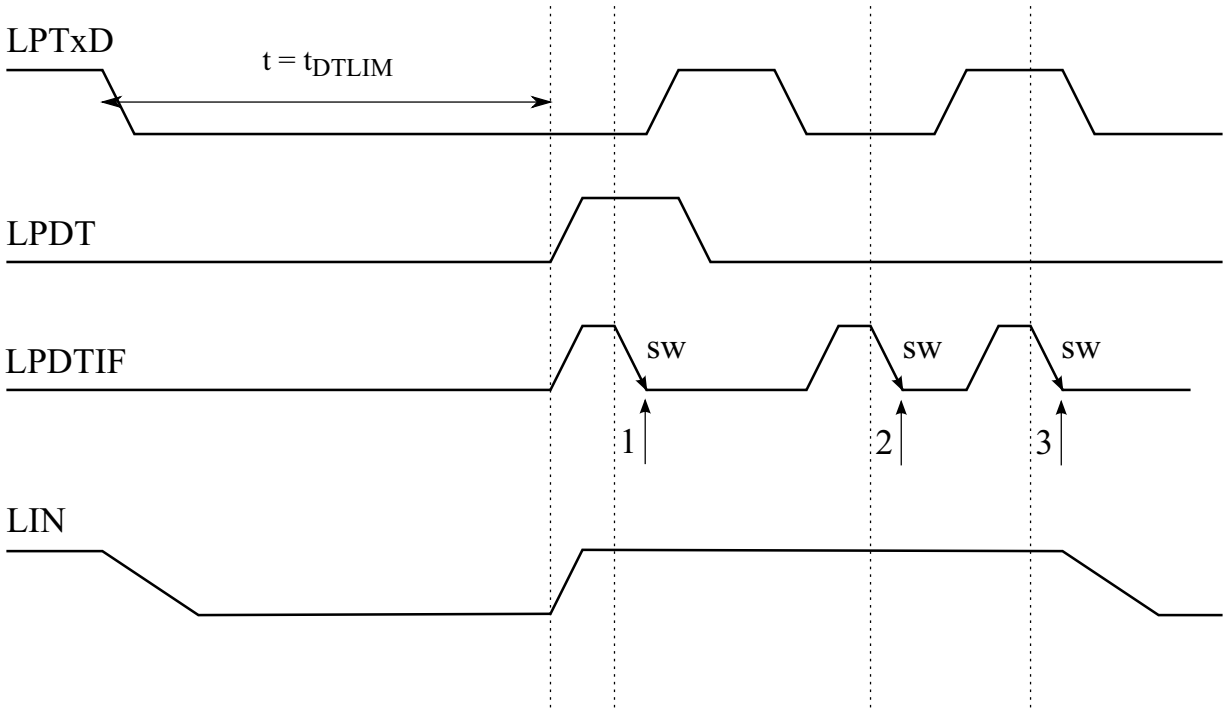
Please make sure that LPDTIF=1 before trying to clear it. It is not allowed to try to clear LPDTIF if LPDTIF=0 already.

After clearing LPDTIF, if the TxD-dominant timeout condition is still present or the LPTxD pin is dominant while being in normal mode, the transmitter remains disabled and the LPDTIF flag is set after a time again to indicate that the attempt to re-enable has failed. This time is equal to:

- minimum 1 IRC period (1 us) + 2 bus periods
- maximum 2 IRC periods (2 us) + 3 bus periods

If the bit LPDTIE is set in the LPIE register, an interrupt is requested.

Figure 19-13 shows the different scenarios of TxD-dominant timeout interrupt handling.



1: Flag cleared, transmitter re-enable not successful because TxD-dominant timeout condition is still present
2: Flag cleared, transmitter re-enable not successful because LPTxD is dominant
3: Flag cleared, transmitter re-enable successful

Figure 19-13. TxD-dominant timeout interrupt handling

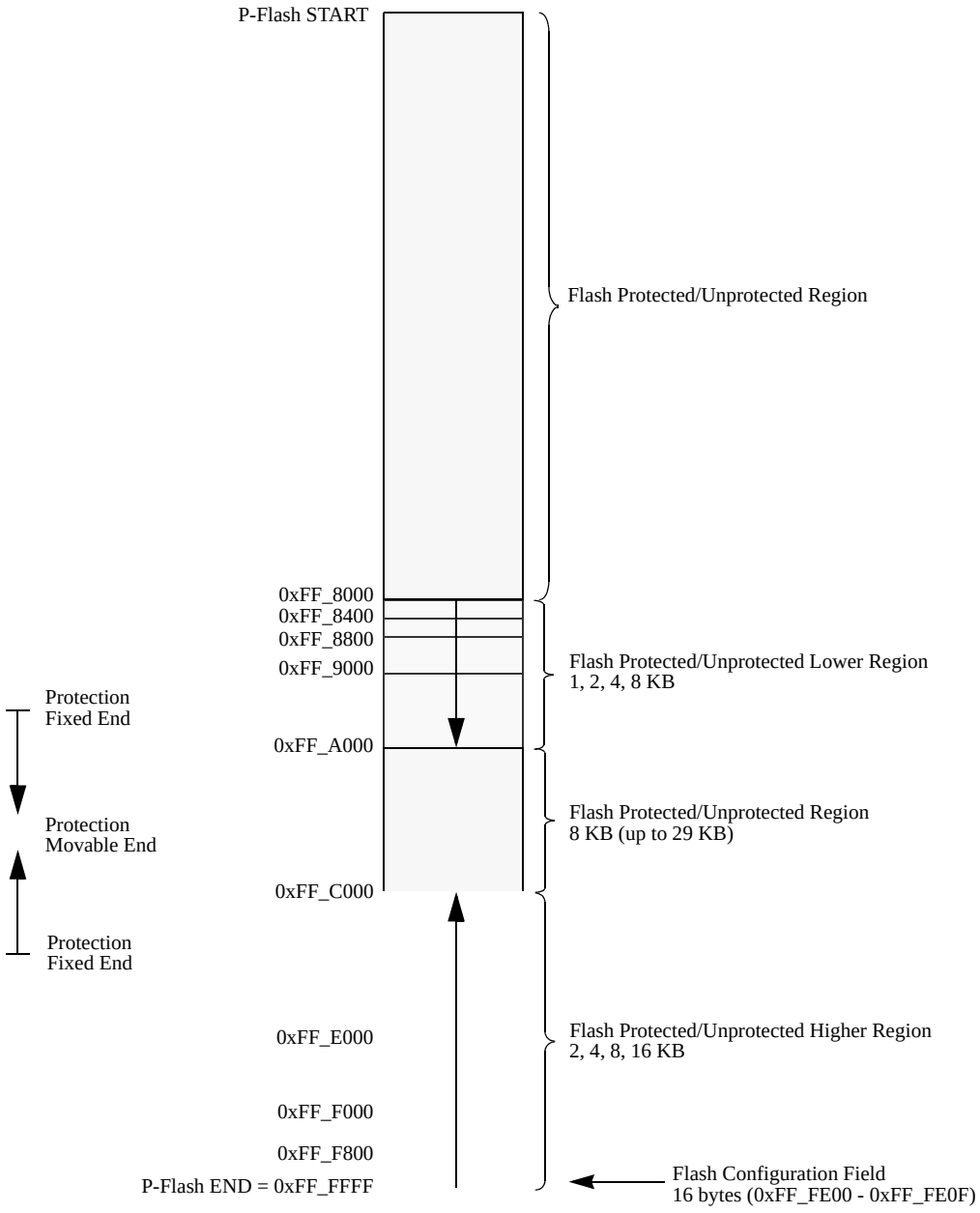


Figure 20-2. P-Flash Memory Map With Protection Alignment

Table 20-27. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
011	FCCOB3	HI	Data 1 [15:8]
		LO	Data 1 [7:0]
100	FCCOB4	HI	Data 2 [15:8]
		LO	Data 2 [7:0]
101	FCCOB5	HI	Data 3 [15:8]
		LO	Data 3 [7:0]

20.4 Functional Description

20.4.1 Modes of Operation

The module provides the modes of operation normal and special. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and DFPROT registers (see Table 20-29).

20.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x1F_C0B6. The contents of the word are defined in Table 20-28.

Table 20-28. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

20.4.3 Flash Block Read Access

If data read from the Flash block results in a double-bit fault ECC error (meaning that data is detected to be in error and cannot be corrected), the read data will be tagged as invalid during that access (please look

Table 20-61. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

20.4.7.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

Table 20-62. Erase Verify EEPROM Section Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x10	Global address [23:16] to identify the EEPROM block
FCCOB1	Global address [15:0] of the first word to be verified	
FCCOB2	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table F-4. FTMRZ32K128 NVM Timing Characteristics (Junction Temperature From 150°C To +175°C)

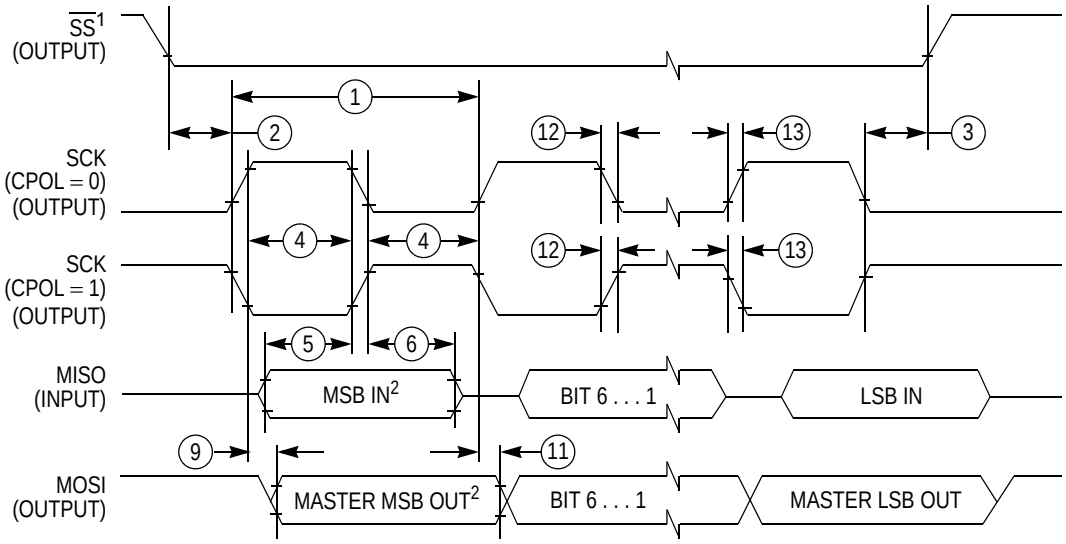
Derivatives ZVML31, ZVM32, ZVM16									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	40	40	40	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	8992	t_{RD1ALL}	0.22	0.22	0.45	17.98	ms
4	Erase Verify Block (Pflash)	0	8750	t_{RD1BLK_P}	0.22	0.22	0.44	17.50	ms
5	Erase Verify Block (EEPROM)	0	631	t_{RD1BLK_D}	0.02	0.02	0.03	1.26	ms
6	Erase Verify P-Flash Section	0	511	t_{RD1SEC}	0.01	0.01	0.03	1.02	ms
7	Read Once	0	481	t_{RDONCE}	12.03	12.03	12.03	481.00	us
8	Program P-Flash (4 Word)	164	3136	t_{PGM_4}	0.23	0.24	0.48	12.75	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.23	0.24	0.24	3.31	ms
10	Erase All Blocks	100066	9455	t_{ERSALL}	95.54	100.30	100.54	143.99	ms
11	Erase Flash Block (Pflash)	100060	9119	t_{ERSBLK_P}	95.52	100.29	100.52	143.31	ms
12	Erase Flash Block (EEPROM)	100060	970	t_{ERSBLK_D}	95.32	100.08	100.11	127.02	ms
13	Erase P-Flash Sector	20015	927	t_{ERSPG}	19.09	20.04	20.06	26.87	ms
14	Unsecure Flash	100066	9533	t_{UNSECU}	95.54	100.30	100.54	144.15	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	12.33	12.33	12.33	493.00	us
16	Set User Margin Level	0	439	t_{MLOADU}	10.98	10.98	10.98	439.00	us
17	Set Factory Margin Level	0	448	t_{MLOADF}	11.20	11.20	11.20	448.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.03	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.11	0.11	0.24	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.20	0.20	0.41	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.29	0.30	0.58	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.38	0.39	0.75	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.80	5.04	20.41	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	11.88	11.88	11.88	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging



1. If enabled.

2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-3. SPI Master Timing (CPHA=1)

Table I-1. SPI Master Mode Timing Characteristics (Junction Temperature From -40°C To +175°C)

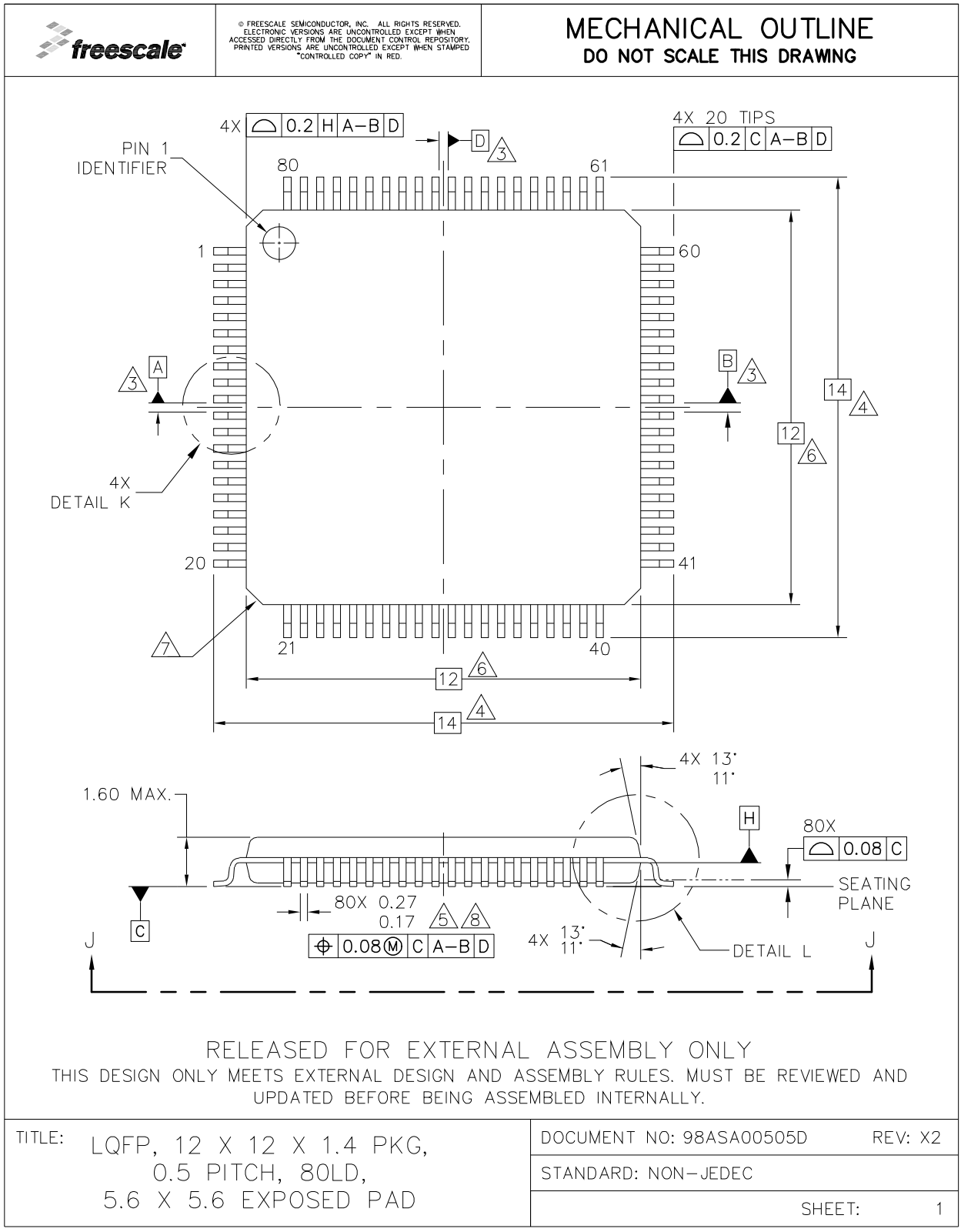
Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1		SCK Frequency	f_{sck}	1/2048	—	$1/2^{(1)(2)}$	f_{bus}
1		SCK Period	t_{sck}	2	—	2048	t_{bus}
2		Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3		Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4		Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5		Data Setup Time (Inputs)	t_{su}	4	—	—	ns
6		Data Hold Time (Inputs)	t_{hi}	5	—	—	ns
9		Data Valid after SCK Edge	t_{vsck}	—	—	10	ns
10		Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	9	ns
11		Data Hold Time (Outputs)	t_{ho}	-1.2	—	—	ns
12		Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13		Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1. See **Figure I-4.**

2. f_{bus} max is 40MHz at temperatures above 150°C

K.4 80LQFP-EP Mechanical Information

Figure K-4. 80LQFP-EP



M.15 0x06A0-0x06BF GDU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06A0	GDUE	R	GWP	0	0	GCS1E	GBOE	GCS0E	GCPE	GFDE
		W								
0x06A1	GDUCTR	R	GHHDLVL	GVLSLVL (1)	GBKTIM2[3:0]				GBKTIM1[1:0]	
		W								
0x06A2	GDUIE	R	0	0	0	GOCIE[1:0]		GDSEIE	GHHDIE	GLVLSIE
		W								
0x06A3	GDUDSE	R	0	GDHSIF[2:0]			0	GDLSIF[2:0]		
		W								
0x06A4	GDUSTAT	R	GPHS[2:0]			GOCS[1:0]			GHHDS	GLVLSS
		W								
0x06A5	GDUSRC	R	0	GSRCHS[2:0]			0	GSRCLS[2:0]		
		W								
0x06A6	GDUF	R	GSUF	GHHDF	GLVLSF	GOCIF[1:0]		0	GHHDIF	GLVLSIF
		W								
0x06A7	GDUCLK1	R	0	GBOCD[4:0]					GBODC[1:0]	
		W								
0x06A8	GDUBCL	R	0	0	0	0	GBCL[3:0]			
		W								
0x06A9	GDUPHMUX	R	0	0	0	0	0	0	GPHMX[1:0]	
		W								
0x06AA	GDUCSO	R	0	GCSO1[2:0]			0	GCSO0[2:0]		
		W								
0x06AB	GDUDSLVL	R	GDSFHS[1]	GDSLHS[2:0]			GDSFLS[1]	GDSLLS[2:0]		
		W								
0x06AC	GDUPHL	R	0	0	0	0	0	GPHL[2:0]		
		W								
0x06AD	GDUCLK2	R	0	0	0	0	GCPCD[3:0]			
		W								
0x06AE	GDUOC0	R	GOCA0	GOCE0	0	GOCT0[4:0](2)				
		W								
0x06AF	GDUOC1	R	GOCA1	GOCE1	0	GOCT1[4:0](3)				
		W								
0x06B0	GDUCTR1(4)	R	GSRMOD[1:0]		0	0	0	0	0	TDEL
		W								