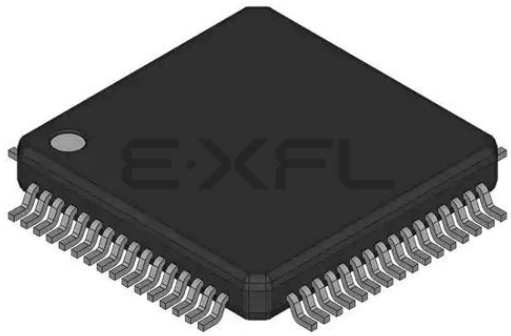

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Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912zvmc12f1mkh

the capacitor C_{BS} is first charged to VLS_OUT via an external diode (GDUV4) or internal transistor (GDUV5), when the low side driver is active Figure 1-20. When the high side driver switches on, the charge on this capacitor, supplies the FET-predriver via the VBSx pin. The C_{BS} capacitor can only be charged if the low side driver is active, so after a long period of inactivity of the low side driver, the C_{BS} capacitor becomes discharged. In this case, the low side driver must be switched on to charge C_{BS} before commencing high side driving. The time it takes to discharge the bootstrap capacitor C_{BS} can be calculated from the size of the bootstrap capacitor C_{BS} and the current on VBSx pin in the high side inactive phase.

The bootstrap capacitors must be precharged before turning on the high-side drivers for the first time. This can be done by using the PMF software output control mechanism:

```
PMFOUTC = 0x3F;                         // SW control on all outputs
PMFOUTB = 0x2A;                         // All high-sides off, all low-sides on
```

The PWM0 signals should be configured to start with turning on the low-side before the high-side drivers in order to assure precharged bootstraps. Therefore invert the PWM0 signals:

```
PMFCINV = 0x3F;                         // Invert all channels to precharge bootstraps
```

1.13.8.2.2 High Side Charge Pump

A charge pump voltage is used to supply the high side FET-predriver with enough current to maintain the gate source voltage. To generate this voltage an external charge pump is driven by the pin CP, switching between 0V and 11V. The pumped voltage is then applied to the pin VCP.

At 100% duty cycle operation the low-side turn on time is zero during a masked commutation cycle before the attempting to turn on the high side drivers. This can cause bootstrap charge to decay.

In order to speed-up the high-side gate voltage level directly after commutation, the software should drive the first PWM cycle with a duty cycle meeting an on-time of at least $t_{minpulse}$ for the low-side drivers and then switch back to 100% again.

The recommended procedure for BLDC applications is to use the manual correction method (PMFCCTL[ISENS]) as described below:

Set odd PMF values to alternative duty cycle. At commutation event when one of the three high-side drivers is turned on (every 120°) set the PMFCCTL[IPOLx] bits and clear them at the next PWM reload event.

Given unipolar switching mode:

```
// TIM OC0 ISR:
if ((PMFOUTC == 0x1c) || (PMFOUTC == 0x07) || (PMFOUTC == 0x31)) // all high-side turn-on sectors
         PMFCCTL = 0x17; // select odd PMF values

// PMF reload ISR:
         PMFCCTL = 0x10; // select even PMF values
```

The GDU high side drain voltage, pin HD, is supplied from VBAT through a reverse battery protection circuit. In a typical application the charge pump is used to switch on an external NMOS, N1, with source connected to VBAT, by generating a voltage of VBAT+VLS-(2xVdiode). In a reverse battery scenario, the external bipolar turns on, ensuring that the HD pin is isolated from VBAT by the external NMOS, N1.

2.3.3.6 Port Interrupt Enable Register

Address 0x028C PIEADH
0x028D PIEADL
0x02D6 PIES
0x0336 PIEL

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIEx7	PIEx6	PIEx5	PIEx4	PIEx3	PIEx2	PIEx1	PIEx0
Reset	0	0	0	0	0	0	0	0

Figure 2-17. Port Interrupt Enable Register

1. Read: Anytime
   Write: Anytime

This is a generic description of the standard port interrupt enable registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-22. Port Interrupt Enable Register Field Descriptions

Field	Description
7-0 PIEx7-0	**Port Interrupt Enable** — Activate pin interrupt (KWU) This bit enables or disables the edge sensitive pin interrupt on the associated pin. An interrupt can be generated if the pin is operating in input or output mode when in use with the general-purpose or related peripheral function. 1 Interrupt is enabled 0 Interrupt is disabled (interrupt flag masked)

2.3.3.7 Port Interrupt Flag Register

Address 0x028E PIFADH
0x028F PIFADL
0x02D7 PIFS
0x0337 PIFL

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIFx7	PIFx6	PIFx5	PIFx4	PIFx3	PIFx2	PIFx1	PIFx0
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port Interrupt Flag Register

1. Read: Anytime
   Write: Anytime, write 1 to clear

This is a generic description of the standard port interrupt flag registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

3.1.4 Modes of Operation

3.1.4.1 Chip configuration modes

The S12ZMMC determines the chip configuration mode of the device. It captures the state of the MODC pin at reset and provides the ability to switch from special-single chip mode to normal single chip-mode.

3.1.4.2 Power modes

The S12ZMMC module is only active in run and wait mode.There is no bus activity in stop mode.

3.1.5 Block Diagram

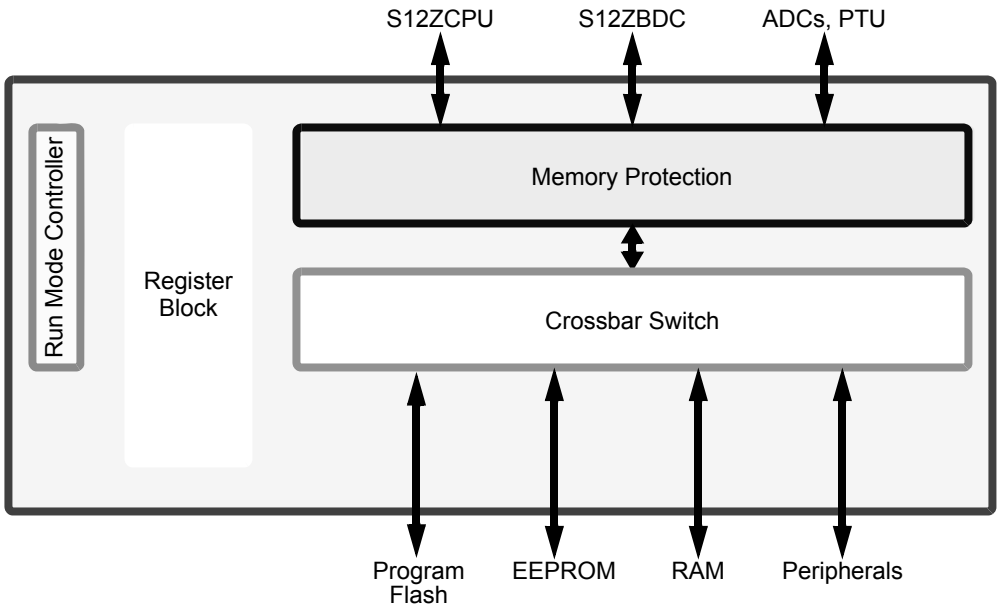


Figure 3-1. S12ZMMC Block Diagram

3.2 External Signal Description

The S12ZMMC uses two external pins to determine the devices operating mode: RESET and MODC (Table 3-3)
See device overview for the mapping of these signals to device pins.

Table 3-3. External System Pins Associated With S12ZMMC

Pin Name	Description
$\overline{\text{RESET}}$	External reset signal. The $\overline{\text{RESET}}$ signal is active low.
MODC	This input is captured in bit MODC of the MODE register when the external $\overline{\text{RESET}}$ pin deasserts.

3.3 Memory Map and Register Definition

3.3.1 Memory Map

A summary of the registers associated with the MMC block is shown in Figure 3-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0070	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0071-0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0080	MMCECH	R	ITR[3:0]				TGT[3:0]			
		W								
0x0081	MMCECL	R	ACC[3:0]				ERR[3:0]			
		W								
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0
		W								
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0
		W								
0x0084	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0085	MMCPCH	R	CPUPC[23:16]							
		W								
0x0086	MMCPCM	R	CPUPC[15:8]							
		W								
0x0087	MMCPCL	R	CPUPC[7:0]							
		W								
0x0088-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 3-2. S12ZMMC Register Summary

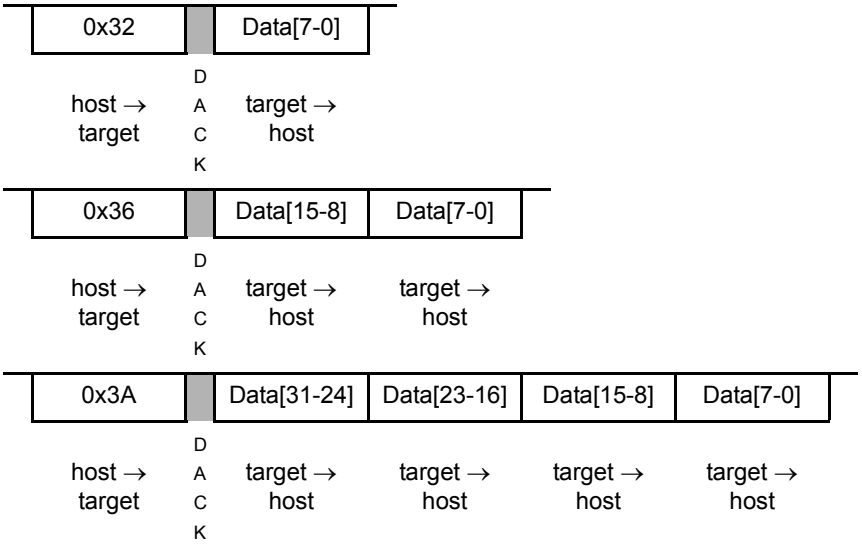
3.3.2 Register Descriptions

This section consists of the S12ZMMC control and status register descriptions in address order.

5.4.4.5 DUMP_MEM.sz, DUMP_MEM.sz_WS

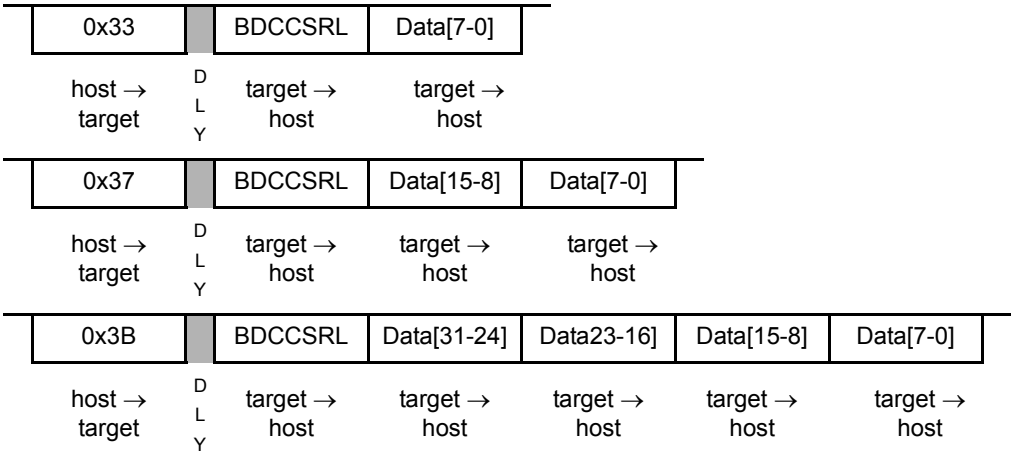
DUMP_MEM.sz

Read memory specified by debug address register, then increment address **Non-intrusive**



DUMP_MEM.sz_WS

Read memory specified by debug address register with status, then increment address **Non-intrusive**



DUMP_MEM{_WS} is used with the READ_MEM{_WS} command to access large blocks of memory. An initial READ_MEM{_WS} is executed to set-up the starting address of the block and to retrieve the first result. The DUMP_MEM{_WS} command retrieves subsequent operands. The initial address is incremented by the operand size (1, 2, or 4) and saved in a temporary register. Subsequent DUMP_MEM{_WS} commands use this address, perform the memory read, increment it by the current operand size, and store the updated address in the temporary register. If the with-status option is specified,

8.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit (S12_CPMU_UHV_V10 and S12CPMU_UHV_V6).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators.
- The Voltage regulator (VREGAUTO) operates from the range 6V to 18V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.
- The Internal Reference Clock (IRC1M) provides a 1MHz internal clock.

This supply domain is monitored by the Low Voltage Reset circuit.

VDDX has to be connected externally to VDDA.

8.2.6 VDDC— CAN Supply Pin

VDDC is the supply domain for the CAN module.

An off-chip decoupling capacitor (10µF plus 220 nF(X7R ceramic)) between VDDC and VSSX is required.

This supply domain is monitored by the Low Voltage Reset circuit.

8.2.7 VDDS1— Sensor Supply1 Pin

VDDS1 is a short circuit protected supply domain which is suitable for sensors (which connect externally to the PCB).

An off-chip decoupling capacitor (4.7µF plus 220 nF(X7R ceramic)) between VDDS1 and VSSX is required.

This supply domain is monitored by a Low Voltage Detect (LVDS1) circuit.

8.2.8 VDDS2— Sensor Supply2 Pin

VDDS2 is a short circuit protected supply domain which is suitable for sensors (which connect externally to the PCB).

An off-chip decoupling capacitor (4.7µF plus 220 nF(X7R ceramic)) between VDDS2 and VSSX is required.

This supply domain is monitored by a Low Voltage Detect (LVDS2) circuit.

8.2.9 BCTL— Base Control Pin for external PNP

BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external BJT (PNP) of the VDDX and VDDA supplies. An additional 1KΩ resistor between emitter and base of the BJT is required.

Figure 8-3 shows an application example for the external BCTL pin.

Several examples of PLL divider settings are shown in Table 8-34. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 8-34. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.

Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

Table 9-11. Summary of Conversion Flow Control Bit Scenarios

RSTA	TRIG	SEQA	LDOK	Conversion Flow Control Mode	Conversion Flow Control Scenario
0	0	0	0	Both Modes	Valid
0	0	0	1	Both Modes	Can Not Occur
0	0	1	0	Both Modes	Valid[5.]
0	0	1	1	Both Modes	Can Not Occur
0	1	0	0	Both Modes	Valid[2.]
0	1	0	1	Both Modes	Can Not Occur
0	1	1	0	Both Modes	Can Not Occur
0	1	1	1	Both Modes	Can Not Occur
1	0	0	0	Both Modes	Valid[4.]
1	0	0	1	Both Modes	Valid[1. 4.]
1	0	1	0	Both Modes	Valid[3. 4. 5.]
1	0	1	1	Both Modes	Valid[1. 3. 4. 5.]
1	1	0	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2. 4. 6.]
1	1	0	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[1. 2. 4. 6.]
1	1	1	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2. 3. 4. 5. 6.]
1	1	1	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[(1) (2) (3) (4) (5) (6)]

1. Swap CSL buffer

2. Start conversion sequence

3. Prevent RSTA_EIF and LDOK_EIF

4. Load conversion command from top of CSL

5. Abort any ongoing conversion, conversion sequence and CSL

6. Bit TRIG set automatically in Trigger Mode

For a detailed description of all conversion flow control bit scenarios please see also Section 9.6.3.2.4, “The two conversion flow control Mode Configurations, Section 9.6.3.2.5, “The four ADC conversion flow control bits and Section 9.6.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios

9.6.3.2.4 The two conversion flow control Mode Configurations

The ADC provides two modes (“Trigger Mode” and “Restart Mode”) which are different in the conversion control flow. The “Restart Mode” provides precise timing control about the sample start point but is more complex from the flow control perspective, while the “Trigger Mode” is more simple from flow control point of view but is less controllable regarding conversion sample start.

Following are the key differences:

In “Trigger Mode” configuration, when conversion flow control bit RSTA gets set the bit TRIG gets set automatically. Hence in “Trigger Mode” the applications should not set the bit TRIG and bit RSTA simultaneously (via data bus or internal interface), because it is a flow control failure and the ADC will cease operation.

In “Trigger Mode” configuration, after the execution of the initial Restart Event the current CSL can be executed and controlled via Trigger Events only. Hence, if the “End Of List” command is reached a restart of conversion flow from top of current CSL does not require to set bit RSTA because returning to the top of current CSL is done automatically. Therefore the current CSL can be executed again after the “End Of List” command type is executed by a Trigger Event only.

In “Restart Mode” configuration, the execution of a CSL is controlled via Trigger Events and Restart Events. After execution of the “End Of List” command the conversion flow must be continued by a Restart Event followed by a Trigger Event and the Trigger Event must not occur before the Restart Event has finished.

For more details and examples regarding flow control and application use cases please see following section and Section 9.9.7, “Conversion flow control application information.

9.6.3.2.5 The four ADC conversion flow control bits

There are four bits to control conversion flow (execution of a CSL and CSL exchange in double buffer mode). Each bit is controllable via the data bus and internal interface depending on the setting of ACC_CFG[1:0] bits (see also Figure 9-2). In the following the conversion control event to control the conversion flow is given with the related internal interface signal and corresponding register bit name together with information regarding:

- Function of the conversion control event
- How to request the event
- When is the event finished
- Mandatory requirements to executed the event

A summary of all event combinations is provided by Table 9-11.

- **Trigger Event**
  Internal Interface Signal: Trigger
  Corresponding Bit Name: TRIG

9.7 Resets

At reset the ADC12B_LBA is disabled and in a power down state. The reset state of each individual bit is listed within Section 9.5.2, “Register Descriptions” which details the registers and their bit-fields.

9.8 Interrupts

The ADC supports three types of interrupts:

- Conversion Interrupt
- Sequence Abort Interrupt
- Error and Conversion Flow Control Issue Interrupt

Each of the interrupt types is associated with individual interrupt enable bits and interrupt flags.

9.8.1 ADC Conversion Interrupt

The ADC provides one conversion interrupt associated to 16 interrupt enable bits with dedicated interrupt flags. The 16 interrupt flags consist of:

- 15 conversion interrupt flags which can be associated to any conversion completion.
- One additional interrupt flag which is fixed to the “End Of List” conversion command type within the active CSL.

The association of the conversion number with the interrupt flag number is done in the conversion command.

9.8.2 ADC Sequence Abort Done Interrupt

The ADC provides one sequence abort done interrupt associated with the sequence abort request for conversion flow control. Hence, there is only one dedicated interrupt flag and interrupt enable bit for conversion sequence abort and it occurs when the sequence abort is done.

9.9.7 Conversion flow control application information

The ADC12B_LBA provides various conversion control scenarios to the user accomplished by the following features.

The ADC conversion flow control can be realized via the data bus only, the internal interface only, or by both access methods. The method used is software configurable via bits ACC_CFG[1:0].

The conversion flow is controlled via the four conversion flow control bits: SEQA, TRIG, RSTA, and LDOK.

Two different conversion flow control modes can be configured: Trigger Mode or Restart Mode

Single or double buffer configuration of CSL and RVL.

9.9.7.1 Initial Start of a Command Sequence List

At the initial start of a Command Sequence List after device reset all entries for at least one of the two CSL must have been completed and data must be valid. Depending on if the CSL_0 or the CSL_1 should be executed at the initial start of a Command Sequence List the following conversion control sequence must be applied:

If CSL_0 should be executed at the initial conversion start after device reset:
A Restart Event and a Trigger Event must occur (depending to the selected conversion flow control mode the events must occur one after the other or simultaneously) which causes the ADC to start conversion with commands loaded from CSL_0.

If CSL_1 should be executed at the initial conversion start after device reset:
Bit LDOK must be set simultaneously with the Restart Event followed by a Trigger Event (depending on the selected conversion flow control mode the Trigger events must occur simultaneously or after the Restart Event is finished). As soon as the Trigger Event gets executed the ADC starts conversion with commands loaded from CSL_1.

As soon as a new valid Restart Event occurs the flow for ADC register load at conversion sequence start as described in Section 9.6.3.3, “ADC List Usage and Conversion/Conversion Sequence Flow Description applies.

9.9.7.2 Restart CSL execution with currently active CSL

To restart a Command Sequence List execution it is mandatory that the ADC is idle (no conversion or conversion sequence is ongoing).

If necessary, a possible ongoing conversion sequence can be aborted by the Sequence Abort Event (setting bit SEQA). As soon as bit SEQA is cleared by the ADC, the current conversion sequence has been aborted and the ADC is idle (no conversion sequence or conversion ongoing).

After a conversion sequence abort is executed it is mandatory to request a Restart Event (bit RSTA set). After the Restart Event is finished (bit RSTA is cleared), the ADC accepts a new Trigger Event (bit TRIG can be set) and begins conversion from the top of the currently active CSL. In conversion flow control

13.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the MSCAN.

13.3.1 Module Memory Map

Figure 13-3 gives an overview on all registers and their individual bits in the MSCAN memory map. The *register address* results from the addition of *base address* and *address offset*. The *base address* is determined at the MCU level and can be found in the MCU memory map description. The *address offset* is defined at the module level.

The MSCAN occupies 64 bytes in the memory space. The base address of the MSCAN module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset.

The detailed register descriptions follow in the order they appear in the register map.

14.3.2.11 Trigger Generator 1 Trigger Number Register (TG1TNUM)

Module Base + 0x000B — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	TG1TNUM[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-13. Trigger Generator 1 Trigger Number Register (TG1TNUM)

1. Read: Anytime
   Write: Never

Table 14-13. TG1TNUM Register Field Descriptions

Field	Description
4:0 TG1TNUM[4:0]	Trigger Generator 1 Trigger Number — This register shows the number of generated triggers since the last reload event. After the generation of 32 triggers this register shows zero. The next reload event clears this register. See also Figure 14-22.

14.3.2.12 Trigger Generator 1 Trigger Value (TG1TVH, TG1TVL)

Module Base + 0x000C — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	TG1TV[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read only

	7	6	5	4	3	2	1	0
R	TG1TV[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-14. Trigger Generator 1 Trigger Value Register (TG1TVH, TG1TVL)

1. Read: Anytime
   Write: Never

Table 18-3. GDUE Register Field Description

Field	Description
1 GCPE	**GDU Charge Pump Enable** — This bit enables the charge pump. This bit cannot be modified after GWP bit is set. See Section 18.4.4, “Charge Pump 0 Charge pump is disabled 1 Charge pump is enabled
0 GFDE	**GDU FET Pre-Driver Enable** — This bit enables the low-side and high-side FET pre-drivers. It must also be set in order to use the boost converter and the current sense amplifiers. This bit cannot be modified after GWP bit is set.See Section 18.4.2, “Low-Side FET Pre-Drivers and Section 18.4.3, “High-Side FET Pre-Driver. 0 Low-side and high-side drivers are disabled 1 Low-side and high-side drivers are enabled **NOTE** It is not allowed to set and clear GFDE bit periodically in order to switch on and off the FET pre-drivers. In order to switch on and off the FET pre-drivers the PMF module has to be used to mask and un-mask the PWM channels.

Table 18-11. Boost Option Clock Divider Factors k = f_{BUS} / f_{BOOST}

GBOCD[4:0]	f_{BOOST}
11011	f_{BUS} / 384
11100	f_{BUS} / 400
11101	f_{BUS} / 512
11110	f_{BUS} / 768
11111	f_{BUS} / 800

22.2.1 PWM7 - PWM0 — PWM Channel 7 - 0

Those pins serve as waveform output of PWM channel 7 - 0.

22.3 Memory Map and Register Definition

22.3.1 Module Memory Map

This section describes the content of the registers in the scalable PWM module. The base address of the scalable PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated with the scalable PWM and their relative offset from the base address. The register detail description follows the order they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

22.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the scalable PWM module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PWME(1)	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
	W								
0x0001 PWMPOL1	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
	W								
0x0002 PWMCLK1	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
	W								
0x0003 PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
0x0004 PWMCAE1	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
	W								
0x0005 PWMCTL1	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
	W								

= Unimplemented or Reserved

Figure 22-2. The scalable PWM Register Summary (Sheet 1 of 4)

Table A-16. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUACLKTR	trimmed to >=20Khz
CPMUAPIRH/RL	set to 0xFFFF

Table A-17. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
SCI	Continuously transmit data (0x55) at speed of 19200 baud
SPI	Configured to master mode, continuously transmit data (0x55) at 1Mbit/s
ADC	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on a single input channel
MSCAN	Configured in loop back mode with a bit rate of 500kbit/s.
DBG	The module is disabled, as in typical final applications
PTU	The module is enabled, bits TG1EN and TG0EN are set. PTUFRE is also set to generate automatic reload events.
PMF	The module is configured with a modulus rate of 10 kHz
TIM	The peripheral is configured to output compare mode,
GDU	LDO enabled. Charge pump enabled. Current sense0 enabled. Boost disabled. No output activity (too load dependent)
COP & RTI	Enabled
BATS	Enabled
LINPHY	Connected to SCI and continuously transmit data (0x55) at speed of 19200 baud
CANPHY (ZVMC256)	Enabled and connected to MSCAN module

Appendix I
SPI Electrical Specifications

This section provides electrical parametrics and ratings for the SPI.

In **Figure I-1.** the measurement conditions are listed.

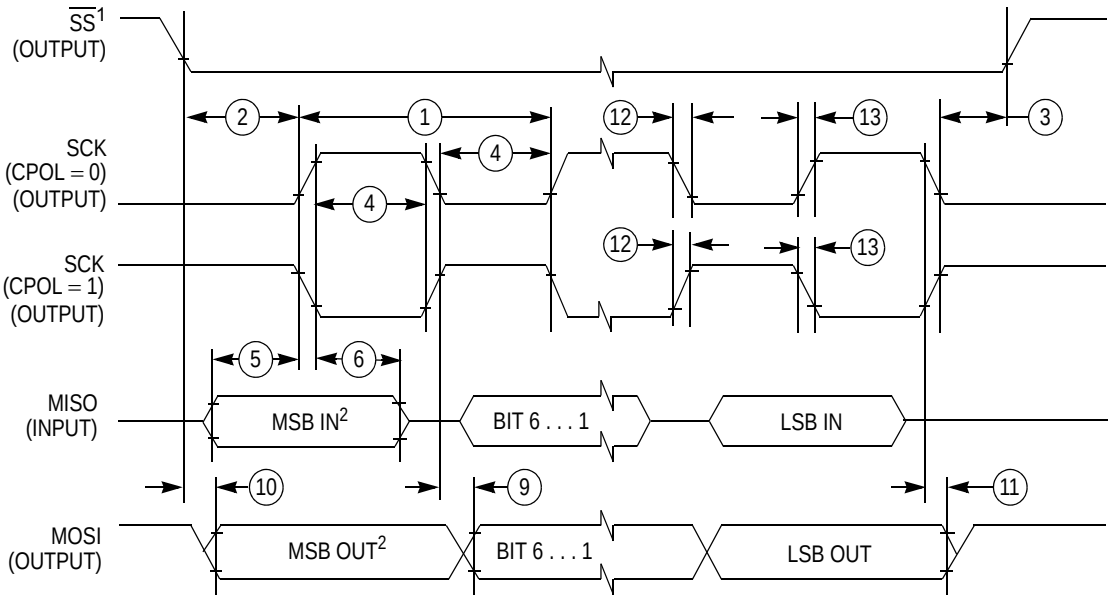
Figure I-1. Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}[(1)], on all outputs	50	pF
Thresholds for delay measurement points	(35% / 65%) VDDX	V

1. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

I.1 Master Mode

In **Figure I-2.** the timing diagram for master mode with transmission format CPHA=0 is depicted.



1. If enabled.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-2. SPI Master Timing (CPHA=0)

In **Figure I-3.** the timing diagram for master mode with transmission format CPHA=1 is depicted.

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x053A	PMFDMP2	R	DMP25		DMP24		DMP23	DMP22	DMP21	DMP20
		W								
0x053B	PMFDMP3	R	DMP35		DMP34		DMP33	DMP32	DMP31	DMP30
		W								
0x053C	PMFDMP4	R	DMP45		DMP44		DMP43	DMP42	DMP41	DMP40
		W								
0x053D	PMFDMP5	R	DMP55		DMP54		DMP53	DMP52	DMP51	DMP50
		W								
0x053E	PMFOUTF	R	0	0	OUTF5	OUTF4	OUTF3	OUTF2	OUTF1	OUTF0
		W								
0x053F	Reserved	R	0	0	0	0	0	0	0	0
		W								

M.11 0x0580-0x059F PTU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0580	PTUE	R	0	PTUFRZ	0	0	0	0	TG1EN	TG0EN
		W								
0x0581	PTUC	R	0	0	0	0	0	0	0	PTULDOK
		W								
0x0582	PTUIEH	R	0	0	0	0	0	0	0	PTUROIE
		W								
0x0583	PTUIEL	R	TG1AEIE	TG1REIE	TG1TEIE	TG1DIE	TG0AEIE	TG0REIE	TG0TEIE	TG0DIE
		W								
0x0584	PTUIFH	R	0	0	0	0	0	0	PTUDEEF	PTUROIF
		W								
0x0585	PTUIFL	R	TG1AEIF	TG1REIF	TG1TEIF	TG1DIF	TG0AEIF	TG0REIF	TG0TEIF	TG0DIF
		W								
0x0586	TG0LIST	R	0	0	0	0	0	0	0	TG0LIST
		W								
0x0587	TG0TNUM	R	0	0	0	TG0TNUM[4:0]				
		W								
0x0588	TG0TVH	R	TG0TV[15:8]							
		W								