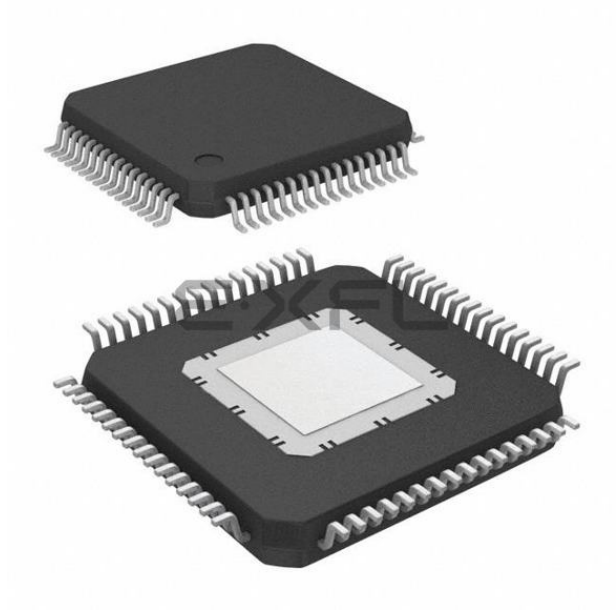


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc12f1mkhr

NOTE

This document shows the superset of all available features offered by the S12ZVM device family. Refer to the package and pinout section in the device overview for functions not available for a particular device or package option.

2.1.2 Features

The PIM includes these distinctive registers:

- Data registers and data direction registers for ports E, T, S, P and AD when used as general-purpose I/O
- Control registers to enable pull devices and select pullups/pulldowns on ports E, T, S, P and AD
- Control register to enable open-drain (wired-or) mode on port S
- Control register to enable digital input buffers on port AD and L[1]
- Interrupt enable register for pin interrupts and key-wakeup (KWU) on port S, P, AD, and L[1]
- Interrupt flag register for pin interrupts andkey-wakeup (KWU) on port S, P, AD, and L[1]
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Control register to enable ECLK output
- Routing registers to support signal relocation on external pins and control internal routings:
  - SPI0 to alternative pins
  - Various SCI0-LINPHY0 routing options supporting standalone use and conformance testing[2]
  - Various MSCAN0-CANPHY0 routing options for standalone use and conformance testing[1]
  - Internal RXD0 and RXD1 link to TIM0 input capture channel (IC0_3) for baud rate detection
  - Internal ACLK link to TIM0 input capture channel
  - 3 pin input mux to one TIM0 IC channel
  - 2 TIM0 channels to alternative pins[3]
  - PMF channels to GDU and/or pins

A standard port pin has the following minimum features:

- Input/output selection
- 5V output drive
- 5V digital and analog input
- Input with selectable pullup or pulldown device

Optional features supported on dedicated pins:

- Open drain for wired-or connections
- Interrupt input with glitch filtering
- High current drive strength from VDDX with over-current protection

1. Only available for ZVMC256
2. Only available for ZVML128, ZVML64, ZVML32, and ZVML31
3. Only available for S12ZVMC256, S12ZVML31, S12ZVM32, and S12ZVM16

2.3.4.8 Port L ADC Direct Register (PTADIRL)

Address 0x033B Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTADIRL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-30. Port L ADC Direct Register (PTADIRL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-34. PTADIRL Register Field Descriptions

Field	Description
1-0 PTADIRL0	**Port L ADC Direct Connection** — This bit connects the analog input signal directly to the ADC channel bypassing the voltage divider. This bit takes effect only in analog mode (PTAENL=1). 1 Input pin directly connected to ADC channel 0 Input voltage divider active on analog input to ADC channel

2.3.4.9 Port L Digital Input Enable Register (DIENL)

Address 0x33C Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	DIENL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-31. Port L Digital Input Enable Register (DIENL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-35. DIENL Register Field Descriptions

Field	Description
0 DIENL0	**Digital Input Enable Port L** — Input buffer control This bit controls the HVI digital input function. If set to 1 the input buffers are enabled and the pin can be used with the digital function. If the analog input function is enabled (PTAENL[PTAENL0]=1) the input buffer of the selected HVI pin is forced off[1] in run mode and is released to be active in stop mode only if DIENL=1. 1 Associated pin digital input is enabled if not used as analog input in run mode[1] 0 Associated pin digital input is disabled[1]

1. Refer to PTTEL bit description in Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL) for an override condition.

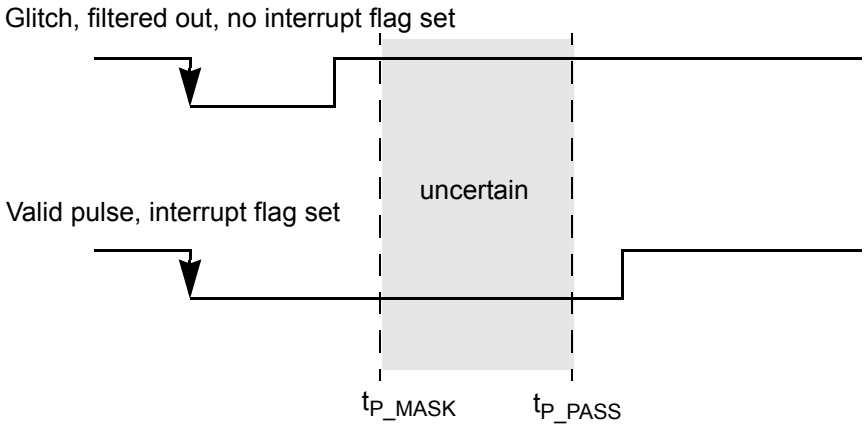


Figure 2-36. Interrupt Glitch Filter (here: active low level selected)

2.4.5 Over-Current Interrupt

In case of an over-current condition on PP0 (see Section 2.5.2, “Open Input Detection on HVI”) the over-current interrupt flag PIFP[OCIF1] asserts. This flag generates an interrupt if the enable bit PIEP[OCIE1] is set.

An asserted flag immediately forces the output pin low to protect the device. The flag must be cleared to re-enable the driver.

2.4.6 High-Voltage Input

A high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to V_{HVI}
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wakeup from stop (pin interrupts in run mode not available). Open input detection.

Figure 2-37 shows a block diagram of the HVI.

NOTE

The term stop mode (STOP) is limited to voltage regulator operating in reduced performance mode (RPM). Refer to “Low Power Modes” section in device overview.

Chapter 3
Memory Mapping Control (S12ZMMCV1)

Table 3-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	27 Jul 2012		Corrected Table 3-9
V01.04	27 Jul 2012		Added feature tags
V01.05	6 Aug 2012		Fixed wording
V01.06	12 Feb 2013	Figure 3-8 3.3.2.2/3-162	• Changed “KByte:to “KB” • Corrected the description of the MMCECH/L register

3.1 Introduction

The S12ZMMC module controls the access to all internal memories and peripherals for the S12ZCPU, and the S12ZBDC module. It also provides access to the RAM for ADCs and the PTU module. The S12ZMMC determines the address mapping of the on-chip resources, regulates access priorities and enforces memory protection. Figure 3-1 shows a block diagram of the S12ZMMC module.

to start the bit up to one target clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 5-6 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later than eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.

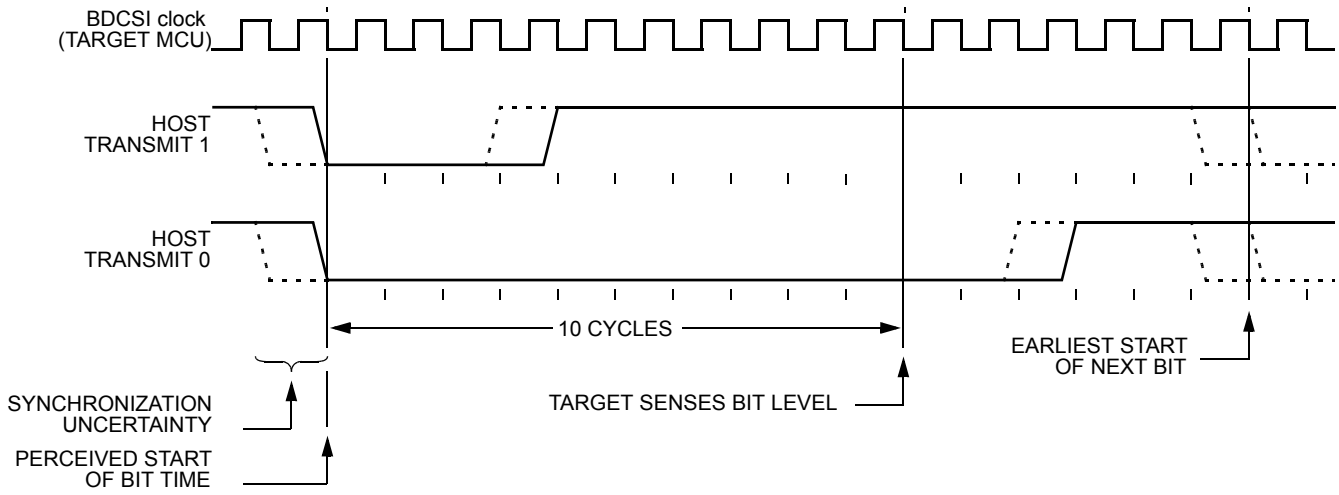


Figure 5-6. BDC Host-to-Target Serial Bit Timing

Figure 5-7 shows the host receiving a logic 1 from the target system. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

Table 8-35. Reset Summary

Reset Source	Local Enable
Oscillator Clock Monitor Reset	OSCE Bit in CPMUOSC register and OMRE Bit in CPMUOSC2 register
COP Reset	CR[2:0] in CPMUCOP register

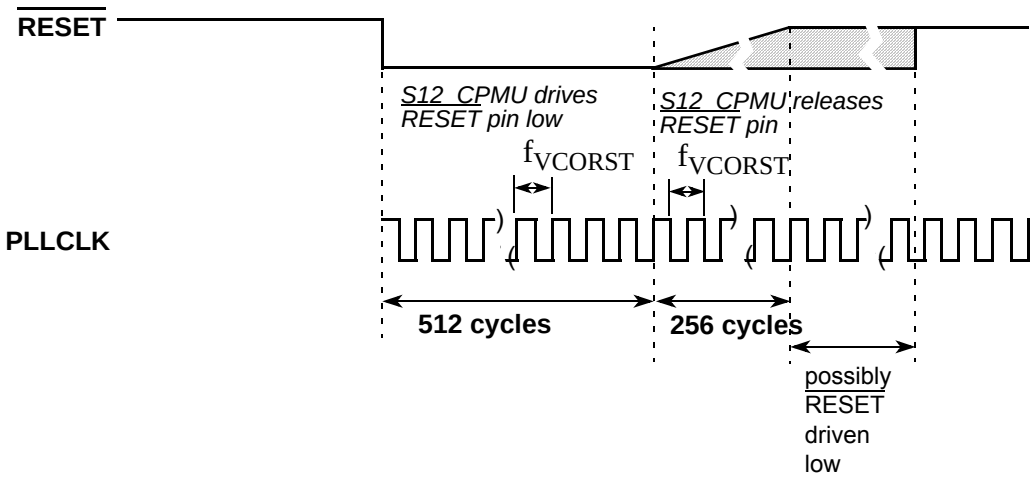
8.5.2 Description of Reset Operation

Upon detection of any reset of Table 8-35, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the $\overline{\text{RESET}}$ pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence.In case the $\overline{\text{RESET}}$ pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

NOTE

While System Reset is asserted the PLLCLK runs with the frequency f_{VCORST}.

Figure 8-45. RESET Timing



8.5.3 Oscillator Clock Monitor Reset

If the external oscillator is enabled (OSCE=1)and the oscillator clock monitor reset is enabled (OMRE=1), then in case of loss of oscillation or the oscillator frequency drops below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates an Oscillator Clock Monitor Reset. In Full Stop Mode the external oscillator and the oscillator clock monitor are disabled.

9.4 Signal Description

This section lists all inputs to the ADC12B_LBA block.

9.4.1 Detailed Signal Descriptions

9.4.1.1 AN*x* (*x* = *n*,..., 2, 1, 0)

This pin serves as the analog input Channel *x*. The maximum input channel number is *n*. Please refer to the device reference manual for the maximum number of input channels.

9.4.1.2 VRH_0, VRH_1, VRH_2, VRL_0, VRL_1

VRH_0/1/2 are the high reference voltages, VRL0/1 are the low reference voltages for a ADC conversion selectable on a conversion command basis. Please refer to the device overview information for availability and connectivity of these pins.

VRH_2 is only available on ADC12B_LBA V3.

VRL_1 is only available on ADC12B_LBA V1 and V2.

See also Table 9-2.

9.4.1.3 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B_LBA block.

NOTE

The register ADCIMDRI is updated and simultaneously a conversion interrupt flag CON_IF[15:1] occurs when the corresponding conversion command (conversion command with INTFLG_SEL[3:0] set) has been processed and related data has been stored to RAM.

9.6.3.2.6 Conversion flow control in case of conversion sequence control bit overrun scenarios

Restart Request Overrun:
If a legal Restart Request is detected and no Restart Event is in progress, the RSTA bit is set due to the request. The set RSTA bit indicates that a Restart Request was detected and the Restart Event is in process. In case further Restart Requests occur while the RSTA bit is set, this is defined a overrun situation. This scenario is likely to occur when bit STR_SEQA is set or when a Restart Event causes a Sequence Abort Event. The request overrun is captured in a background register that always stores the last detected overrun request. Hence if the overrun situation occurs more than once while a Restart Event is in progress, only the latest overrun request is pending. When the RSTA bit is cleared, the latest overrun request is processed and RSTA is set again one cycle later.

LoadOK Overrun:
Simultaneously at any Restart Request overrun situation the LoadOK input is evaluated and the status is captured in a background register which is alternated anytime a Restart Request Overrun occurs while Load OK Request is asserted. The Load OK background register is cleared as soon as the pending Restart Request gets processed.

Trigger Overrun:
If a Trigger occurs whilst bit TRIG is already set, this is defined as a Trigger overrun situation and causes the ADC to cease conversion at the next conversion boundary and to set bit TRIG_EIF. A overrun is also detected if the Trigger Event occurs automatically generated by hardware in “Trigger Mode” due to a Restart Event and simultaneously a Trigger Event is generated via data bus or internal interface. In this case the ADC ceases operation before conversion begins to sample. In “Trigger Mode” a Restart Request Overrun does not cause a Trigger Overrun (bit TRIG_EIF not set).

Sequence Abort Request Overrun:
If a Sequence Abort Request occurs whilst bit SEQA is already set, this is defined as a Sequence Abort Request Overrun situation and the overrun request is ignored.

10.3.2.3 BATS Interrupt Enable Register (BATIE)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	BVHIE	BVLIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-6. BATS Interrupt Enable Register (BATIE)

1. Read: Anytime
   Write: Anytime

Table 10-4. BATIE Register Field Descriptions

Field	Description
1 BVHIE	BATS Interrupt Enable High — Enables High Voltage Interrupt . 0 No interrupt will be requested whenever BVHIF flag is set . 1 Interrupt will be requested whenever BVHIF flag is set
0 BVLIE	BATS Interrupt Enable Low — Enables Low Voltage Interrupt . 0 No interrupt will be requested whenever BVLIF flag is set . 1 Interrupt will be requested whenever BVLIF flag is set .

10.3.2.4 BATS Interrupt Flag Register (BATIF)

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	BVHIF	BVLIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-7. BATS Interrupt Flag Register (BATIF)

1. Read: Anytime
   Write: Anytime, write 1 to clear

Figure 13-24. Receive/Transmit Message Buffer — Extended Identifier Mapping

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X0 IDR0	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	W								
0x00X1 IDR1	R	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
	W								
0x00X2 IDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	W								
0x00X3 IDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	W								
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

Table 15-4. Modes When PWM Operation is Restricted

Mode	Description
STOP	PWM outputs are disabled
WAIT	PWM outputs are disabled as a function of the PMFWAI bit
FREEZE	PWM outputs are disabled as a function of the PMFFRZ bit

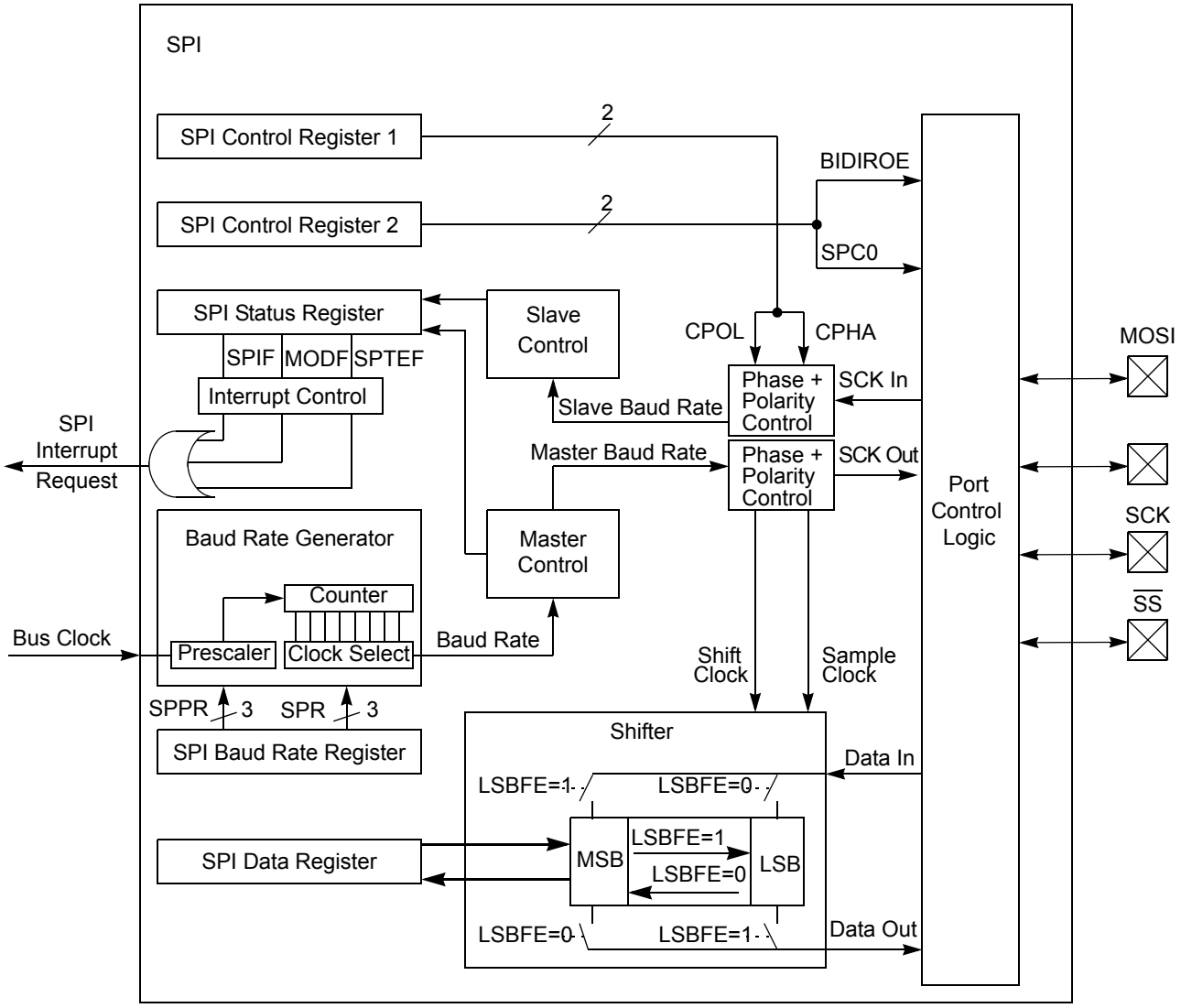


Figure 17-1. SPI Block Diagram

17.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

17.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

18.3.2.16 GDU Overcurrent Register 1 (GDUOC1)

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GOCA1	GOCE1	0	GOCT1[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-18. GDU Overcurrent Register 1 (GDUOC1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-20. GDUOC1 Register Field Descriptions

Field	Description
7 GOCA1	GDU Overcurrent Action — This bit cannot be modified after GWP bit is set. This bit controls the action in case of an overcurrent event or overvoltage event. See Table 18-24 and Table 18-23
6 GOCE1	GDU Overcurrent Enable — This bit cannot be modified after GWP bit is set. 0 Overcurrent Comparator 1 is disabled 1 Overcurrent Comparator 1 is enabled
GDUV4 (includes GOCT1 bits 3:0)	
3:0 GOCT1[3:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper two bits of the digital inputs are tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (48 + GOCT1) \cdot \frac{VDDA}{64}$$
GDUV5 and V6 (includes GOCT1 bits 4:0)	
4:0 GOCT1[4:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper bit of the digital inputs is tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (32 + GOCT1) \cdot \frac{VDDA}{64}$$

Address & Name		7	6	5	4	3	2	1	0
0x0011 FCCOB2LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0012 FCCOB3HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0013 FCCOB3LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0014 FCCOB4HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0015 FCCOB4LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0016 FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0017 FCCOB5LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								

= Unimplemented or Reserved

Figure 20-4. FTMRZ128K512 Register Summary (continued)

1. Number of implemented DPS bits depends on EEPROM memory size.

20.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Offset Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIVLCK	FDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-hi and controls the writability of the FDIV field in normal mode. In special mode, bits 6-0 are writable any number of times but bit 7 remains unwritable.

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 20-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 20-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 20.4.5, “Flash Command Operations,” for more information.

Table 20-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN(1)	MAX(2)		MIN[1]	MAX[2]	
1.0	1.6	0x00	26.6	27.6	0x1A
1.6	2.6	0x01	27.6	28.6	0x1B
2.6	3.6	0x02	28.6	29.6	0x1C
3.6	4.6	0x03	29.6	30.6	0x1D
4.6	5.6	0x04	30.6	31.6	0x1E
5.6	6.6	0x05	31.6	32.6	0x1F
6.6	7.6	0x06	32.6	33.6	0x20
7.6	8.6	0x07	33.6	34.6	0x21
8.6	9.6	0x08	34.6	35.6	0x22
9.6	10.6	0x09	35.6	36.6	0x23
10.6	11.6	0x0A	36.6	37.6	0x24
11.6	12.6	0x0B	37.6	38.6	0x25
12.6	13.6	0x0C	38.6	39.6	0x26
13.6	14.6	0x0D	39.6	40.6	0x27
14.6	15.6	0x0E	40.6	41.6	0x28
15.6	16.6	0x0F	41.6	42.6	0x29
16.6	17.6	0x10	42.6	43.6	0x2A
17.6	18.6	0x11	43.6	44.6	0x2B

The number of DPS bits depends on the size of the implemented EEPROM. The whole implemented EEPROM range can always be protected. Each DPS value increment increases the size of the protected range by 32-bytes. Thus to protect a 1 KB range DPS[4:0] must be set (protected range of 32 x 32 bytes).

20.3.2.11 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F(1)	F1	F1	F1	F1	F1	F1	F1

= Unimplemented or Reserved

Figure 20-16. Flash Option Register (FOPT)

1. Loaded from Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but can only be written in special mode.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0xFF_FE0E located in P-Flash memory (see Table 20-4) as indicated by reset condition F in Figure 20-16. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 20-26. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device overview for proper use of the NV bits.

20.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-17. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

Clock Source = bus clock, where bus clock= 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/8 = 1.25 MHz

PWMx Period = 800 ns

PWMx Duty Cycle = 3/4 *100% = 75%

Shown in Figure 22-20 is the output waveform generated.

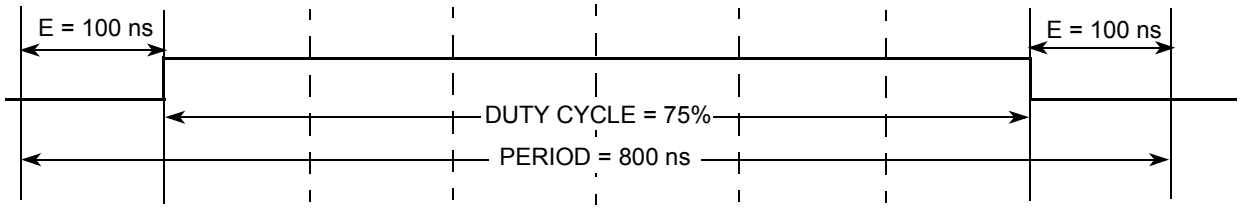


Figure 22-20. PWM Center Aligned Output Example Waveform

22.4.2.7 PWM 16-Bit Functions

The scalable PWM timer also has the option of generating up to 8-channels of 8-bits or 4-channels of 16-bits for greater PWM resolution. This 16-bit channel option is achieved through the concatenation of two 8-bit channels.

The PWMCTL register contains four control bits, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. Channels 6 and 7 are concatenated with the CON67 bit, channels 4 and 5 are concatenated with the CON45 bit, channels 2 and 3 are concatenated with the CON23 bit, and channels 0 and 1 are concatenated with the CON01 bit.

NOTE

Change these bits only when both corresponding channels are disabled.

When channels 6 and 7 are concatenated, channel 6 registers become the high order bytes of the double byte channel, as shown in Figure 22-21. Similarly, when channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

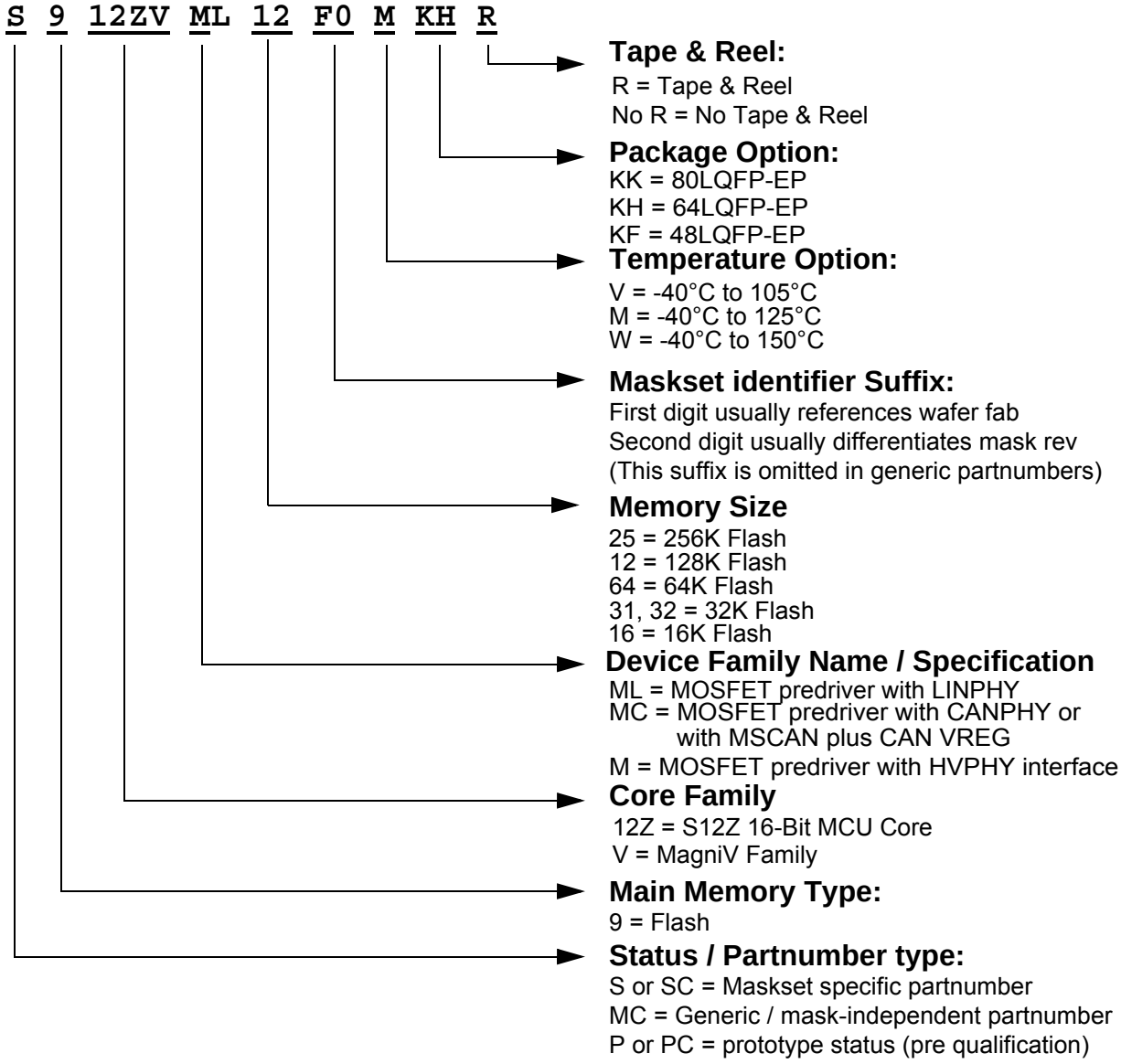
When using the 16-bit concatenated mode, the clock source is determined by the low order 8-bit channel clock select control bits. That is channel 7 when channels 6 and 7 are concatenated, channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low order 8-bit channel as also shown in Figure 22-21. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low order 8-bit channel as well.

Appendix L
Ordering Information

Customers can choose either the mask-specific partnumber or the generic, mask-independent partnumber. Ordering a mask-specific partnumber enables the customer to specify which particular maskset they receive whereas ordering the generic partnumber means that the currently preferred maskset (which may change over time) is shipped. In either case, the marking on the device always shows the generic, mask-independent partnumber and the mask set number. The below figure illustrates the structure of a typical mask-specific ordering number.

NOTES

Not every combination is offered. Table 1.2.1 lists available derivatives.
The mask identifier suffix and the Tape & Reel suffix are always both omitted from the partnumber which is actually marked on the device.



Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0338–0x0339	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x033A	PTABYPL[2]	R	0	0	0	0	0	0	0	PTABYPL0
		W								
0x033B	PTADIRL[2]	R	0	0	0	0	0	0	0	PTADIRL0
		W								
0x033C	DIENL[2]	R	0	0	0	0	0	0	0	DIENL0
		W								
0x033D	PTAENL[2]	R	0	0	0	0	0	0	0	PTAENL0
		W								
0x033E	PIRL[2]	R	0	0	0	0	0	0	0	PIRL0
		W								
0x033F	PTTEL[2]	R	0	0	0	0	0	0	0	PTTEL0
		W								

1. Only available for ZVML128, ZVML64, ZVML32, and ZVML31

2. Only available for ZVMC256

3. PWMPRR[1] only writable for ZVMC256

4. Only available for ZVMC256, ZVML31, ZVM32, ZVM16

5. Not available for ZVMC256

M.6 0x0380-0x039F FTMRZ128K512

Address	Name		7	6	5	4	3	2	1	0
0x0380	FCLKDIV	R	FDIVLD	FDIVLCK	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		W								
0x0381	FSEC	R	KEYEN1	KEYEN0	RNV5	RNV4	RNV3	RNV2	SEC1	SEC0
		W								
0x0382	FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
		W								
0x0383	FPSTAT	R	FPOVRD	0	0	0	0	0	0	WSTAT ACK
		W								