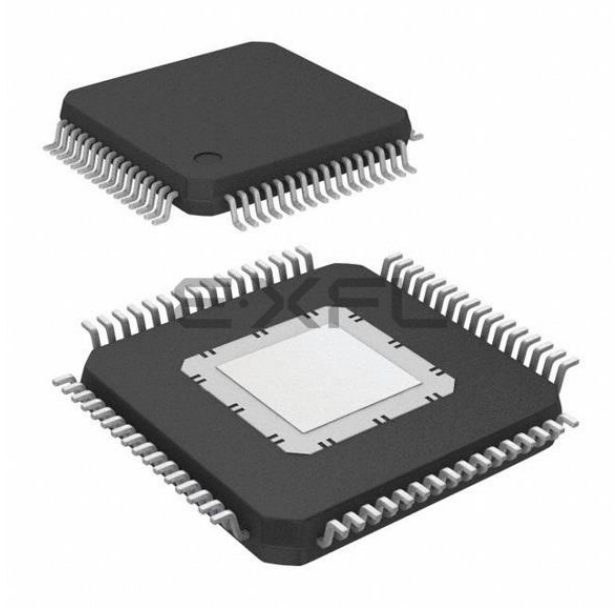

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc12f1vkh

2.3.3.2 Port Input Register

Address 0x0262 PTIE
0x0282 PTIADH
0x0283 PTIADL
0x02C1 PTIT
0x02D1 PTIS
0x02F1 PTIP

Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIx7	PTIx6	PTIx5	PTIx4	PTIx3	PTIx2	PTIx1	PTIx0
W								
Reset	-	-	-	-	-	-	-	-

Figure 2-13. Port Input Register

1. Read: Anytime
Write:Never

This is a generic description of the standard port input registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-18. Port Input Register Field Descriptions

Field	Description
7-0 PTIx7-0	**Port Input** — Data input A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.3.3 Data Direction Register

Address 0x0264 DDRE
0x0284 DDRADH
0x0285 DDRADL
0x02C2 DDRT
0x02D2 DDRS
0x02F2 DDRP

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRx7	DDRx6	DDRx5	DDRx4	DDRx3	DDRx2	DDRx1	DDRx0
Reset	0	0	0	0	0	0	0	0

Figure 2-14. Data Direction Register

1. Read: Anytime
Write: Anytime

This is a generic description of the standard data direction registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Chapter 3
Memory Mapping Control (S12ZMMCV1)

Table 3-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	27 Jul 2012		Corrected Table 3-9
V01.04	27 Jul 2012		Added feature tags
V01.05	6 Aug 2012		Fixed wording
V01.06	12 Feb 2013	Figure 3-8 3.3.2.2/3-162	• Changed “KByte:to “KB” • Corrected the description of the MMCECH/L register

3.1 Introduction

The S12ZMMC module controls the access to all internal memories and peripherals for the S12ZCPU, and the S12ZBDC module. It also provides access to the RAM for ADCs and the PTU module. The S12ZMMC determines the address mapping of the on-chip resources, regulates access priorities and enforces memory protection. Figure 3-1 shows a block diagram of the S12ZMMC module.

- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)
- Trace control
  - Tracing session triggered by state sequencer
  - Begin, End, and Mid alignment of tracing to trigger
- Four trace modes
  - Normal: change of flow (COF) PC information is stored (see Section 6.4.5.2.1) for change of flow definition.
  - Loop1: same as Normal but inhibits consecutive duplicate source address entries
  - Detail: address and data for all read/write access cycles are stored
  - Pure PC: All program counter addresses are stored.
- 2 Pin (data and clock) profiling interface
  - Output of code flow information

6.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

The DBG module can issue breakpoint requests to force the device to enter active BDM or an SWI ISR. The BDC BACKGROUND command is also handled by the DBG to force the device to enter active BDM. When the device enters active BDM through a BACKGROUND command with the DBG module armed, the DBG remains armed.

8.3.2.29 VDDS Status Register (CPMUVDDS)

This register is only available in V10.

The CPMUVDDS register contains the status and flag bits for VDDS1 and VDDS2 to indicate integrity fails. Monitoring of VDDS1 and VDDS2 domain is only active in full performance mode (FPM) and if the respective supply is enabled in CPMUVREGCTL register. It is disabled in reduced performance mode (RPM).

Module Base + 0x001F

	7	6	5	4	3	2	1	0
R	SCS2	SCS1	LVDS2	LVDS1	SCS2IF	SCS1IF	LVS2IF	LVS1IF
W								
Reset	0	0	U	U	0	0	U	U

The Reset state of LVDS and LVIF depends on the external supplied VDDA level
"U" = Unknown, either 0 or 1

= Unimplemented or Reserved

Figure 8-40. VDDS Status Register (CPMUVDDS)

Read: Anytime

Write: SCS2IF, SCS1IF, LVS2IF and LVS1IF are write anytime,
SCS2, SCS, LVS2 and LVS1 are read only

Table 8-33. CPMUVDDS Field Descriptions

Field	Description
7 SCS2	Short circuit on VDDS2 Status Bit —This read-only status bit reflects short circuit status on VDDS2 supply. This feature only makes sense if the VDDS2 supply is enabled (EXT2SON=1). 0 VRH2EN=0 or RPM or VDDS2 voltage level is less than or equal to VDDA supply. 1 VRH2EN=1and FPM and the voltage level on VDDS2 is greater than on VDDA supply.
6 SCS1	Short circuit on VDDS1 Status Bit —This read-only status bit reflects short circuit status on VDDS1 supply. This feature only makes sense if the VDDS1 supply is enabled (EXT1SON=1). 0 VRH1EN=0 or RPM or VDDS1 voltage level is less than or equal to VDDA supply. 1 VRH1EN=1and FPM and the voltage level on VDDS1 is greater than on VDDA supply.
5 LVDS2	Low Voltage on VDDS2 Status Bit —This read-only status bit reflects the voltage level on VDDS2 supply. If VDDS2 is enabled (EXTS2ON=1 in CPMUVREGCTL register), it is monitored that VDDS2 does not drop below a voltage threshold V_{DDSM}. 0 VDDS2 voltage is above V_{DDSM} threshold or VDDS2 is disabled or RPM. 1 EXTS2ON =1 and VDDS2 voltage is below V_{DDSM} threshold and FPM.
4 LVDS1	Low Voltage on VDDS1 Status Bit —This read-only status bit reflects the voltage level on VDDS1 supply. If VDDS1 is enabled (EXTS1ON=1 in CPMUVREGCTL register), it is monitored that VDDS1 does not drop below a voltage threshold V_{DDSM}. 0 VDDS1 voltage is above V_{DDSM} threshold or VDDS1 is disabled or RPM. 1 EXTS1ON =1 and VDDS1 voltage is below V_{DDSM} threshold and FPM.

```
/* put your code to loop and wait for the LOCKIF or */
/* poll CPMUIFLG register until both LOCK status is “1” */
/* that is CPMUIFLG == 0x18 */

/*..............continue to your main code execution here..............*/
```

11.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

11.3.2.12 Timer Input Capture/Output Compare Registers High and Low 0–3(TCxH and TCxL)

Module Base + 0x0010 = TC0H 0x0018=RESERVD
0x0012 = TC1H 0x001A=RESERVD
0x0014=TC2H 0x001C=RESERVD
0x0016=TC3H 0x001E=RESERVD

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 11-18. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L 0x0019 =RESERVD
0x0013 = TC1L 0x001B=RESERVD
0x0015 =TC2L 0x001D=RESERVD
0x0017=TC3L 0x001F=RESERVD

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 11-19. Timer Input Capture/Output Compare Register x Low (TCxL)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should take place before low byte otherwise it will give a different result.

12.3.2.8 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 12-14. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 12-10. TIE Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
1:0 C1I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

12.3.2.9 Timer System Control Register 2 (TSCR2)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	TOI	0	0	0	RESERVED	PR2	PR1	PR0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-15. Timer System Control Register 2 (TSCR2)

Read: Anytime

Write: Anytime.

Table 12-11. TSCR2 Field Descriptions

Field	Description
7 TOI	Timer Overflow Interrupt Enable 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
2:0 PR[2:0]	**Timer Prescaler Select** — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 12-12.

Chapter 15
Pulse Width Modulator with Fault Protection (PMF15B6CV4)

Table 15-1. Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V03.22	02 Sep 2013	15.3.2.4/15-574 15.3.2.11/15-579	• Corrected PINVx bit descriptions • Improved read description of PMFOUTB
V03.23	10 Oct 2013	15.2.8/15-565 15.3.2.18/15-585 15.3.2.22/15-589 15.8.1.1/15-629	• Corrected pmf_reload_is_async signal description • Enhanced note at PMFCINV register • Corrected write value limitations for PMFMODx registers • Corrected register write protection bit names • Orthographical corrections after review
V03.24	08 Nov 2013	15.3.2.8/15-577 Table 15-15 15.4.7/15-613	• Updated PMFFIF bit description • Updated note to QSMP table • Updated Asymmetric PWM output description • Replaced ‘fault clearing’ with ‘fault recovery’ to avoid ambiguity with flags • Various minor corrections. •
V03.25	03 Dec 2013	15.3.2.18/15-585	• Updated note at PMFCINV register
V04.00	03 Dec 2013	15.3.2.3/15-573 15.3.2.11/15-579 15.3.2.18/15-585	• Added write protection to REV1-0 bits (WP) • Added PWM read through PMFOUTB (generator output read option) • Updated note at CINV*n* bits
V04.1	05 Nov 2015	Figure 15-51./15-606 Figure 15-52./15-607Figure 15-53./15-607	• correct figure Figure 15-51./15-606, Figure 15-52./15-607,Figure 15-53./15-607 • update DMPx register description

Glossary

Table 15-2. Glossary of Terms

Term	Definition
Set	Discrete signal is in active logic state.
Clear	A discrete signal is in inactive logic state.
Pin	External physical connection.
Signal	Electronic construct whose state or change in state conveys information.

Table 15-4. Modes When PWM Operation is Restricted

Mode	Description
STOP	PWM outputs are disabled
WAIT	PWM outputs are disabled as a function of the PMFWAI bit
FREEZE	PWM outputs are disabled as a function of the PMFFRZ bit

Table 15-6. PMFCFG0 Field Descriptions (continued)

Field	Description
1 INDEPB	**Independent or Complementary Operation for Pair B**— This bit determines if the PWM channels 2 and 3 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are complementary PWM pair 1 PWM2 and PWM3 are independent PWMs
0 INDEPA	**Independent or Complementary Operation for Pair A**— This bit determines if the PWM channels 0 and 1 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are complementary PWM pair 1 PWM0 and PWM1 are independent PWMs

15.3.2.2 PMF Configure 1 Register (PMFCFG1)

Address: Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-4. PMF Configure 1 Register (PMFCFG1)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

A normal PWM output or positive polarity means that the PWM channel outputs high when the counter value is smaller than or equal to the pulse width value and outputs low otherwise. An inverted output or negative polarity means that the PWM channel outputs low when the counter value is smaller than or equal to the pulse width value and outputs high otherwise.

NOTE

The TOPNEGx and BOTNEGx are intended for adapting to the polarity of external predrivers on devices driving the PWM output directly to pins. If an integrated GDU is driven it must be made sure to keep the reset values of these bits in order not to violate the deadtime insertion.

Table 15-7. PMFCFG1 Field Descriptions

Field	Description
6 ENCE	**Enable Commutation Event —** This bit enables the commutation event input and activates buffering of registers PMFOUTC and PMFOUTB and MSKx bits.This bit cannot be modified after the WP bit is set.If set to zero the commutation event input is ignored and writes to the above registers and bits will take effect immediately. If set to one, the commutation event input is enabled and the value written to the above registers and bits does not take effect until the next commutation event occurs. 0 Commutation event input disabled and PMFOUTC, PMFOUTB and MSK*n* not buffered 1 Commutation event input enabled and PMFOUTC, PMFOUTB and MSK*n* buffered
5 BOTNEGC	**Pair C Bottom-Side PWM Polarity** — This bit determines the polarity for Pair C bottom-side PWM (PWM5). This bit cannot be modified after the WP bit is set. 0 Positive PWM5 polarity 1 Negative PWM5 polarity

17.4.7.5.2 SPIF

SPIF occurs when new data has been received and copied to the SPI data register. After SPIF is set, it does not clear until it is serviced. SPIF has an automatic clearing process, which is described in Section 17.3.2.4, “SPI Status Register (SPISR)”.

17.4.7.5.3 SPTEF

SPTEF occurs when the SPI data register is ready to accept new data. After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process, which is described in Section 17.3.2.4, “SPI Status Register (SPISR)”.

18.3.2.16 GDU Overcurrent Register 1 (GDUOC1)

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GOCA1	GOCE1	0	GOCT1[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-18. GDU Overcurrent Register 1 (GDUOC1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-20. GDUOC1 Register Field Descriptions

Field	Description
7 GOCA1	GDU Overcurrent Action — This bit cannot be modified after GWP bit is set. This bit controls the action in case of an overcurrent event or overvoltage event. See Table 18-24 and Table 18-23
6 GOCE1	GDU Overcurrent Enable — This bit cannot be modified after GWP bit is set. 0 Overcurrent Comparator 1 is disabled 1 Overcurrent Comparator 1 is enabled
GDUV4 (includes GOCT1 bits 3:0)	
3:0 GOCT1[3:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper two bits of the digital inputs are tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (48 + GOCT1) \cdot \frac{VDDA}{64}$$
GDUV5 and V6 (includes GOCT1 bits 4:0)	
4:0 GOCT1[4:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper bit of the digital inputs is tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (32 + GOCT1) \cdot \frac{VDDA}{64}$$

20.4.7.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 20.4.7.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 20-39. Read Once Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x04	Not Required
FCCOB1	Read Once phrase index (0x0000 - 0x0007)	
FCCOB2	Read Once word 0 value	
FCCOB3	Read Once word 1 value	
FCCOB4	Read Once word 2 value	
FCCOB5	Read Once word 3 value	

Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block will return invalid data.

Table 20-40. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

20.4.7.5 Program P-Flash Command

The Program P-Flash operation will program a previously erased phrase in the P-Flash memory using an embedded algorithm.

A P-Flash phrase must be in the erased state before being programmed.
Cumulative programming of bits within a Flash phrase is not allowed.

Table 20-63. Erase Verify EEPROM Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested section breaches the end of the EEPROM block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

20.4.7.15 Program EEPROM Command

The Program EEPROM operation programs one to four previously erased words in the EEPROM block. The Program EEPROM operation will confirm that the targeted location(s) were successfully programmed upon completion.

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 20-64. Program EEPROM Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x11	Global address [23:16] to identify the EEPROM block
FCCOB1	Global address [15:0] of word to be programmed	
FCCOB2	Word 0 program value	
FCCOB3	Word 1 program value, if desired	
FCCOB4	Word 2 program value, if desired	
FCCOB5	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program EEPROM command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program EEPROM command launch determines how many words will be programmed in the EEPROM block. The CCIF flag is set when the operation has completed.

20.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0xFF_FE00-0xFF_FE07). If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the Verify Backdoor Access Key command (see Section 20.4.7.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 20-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 20.4.7.11
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0xFF_FE0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0xFF_FE00-0xFF_FE07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF_FE00-0xFF_FE07 in the Flash configuration field.

20.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode using an automated procedure described in Section 20.4.7.7.1, “Erase All Pin”.

20.5.3 Mode and Security Effects on Flash Command Availability

The availability of Flash module commands depends on the MCU operating mode and security state as shown in Table 20-29.

- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

See Section 22.4.2.3, “PWM Period and Duty” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)

  PWMx Period = Channel Clock Period * PWMPERx
- Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 22.4.2.8, “PWM Boundary Cases”.

Module Base + 0x0014 = PWMPER0, 0x0015 = PWMPER1, 0x0016 = PWMPER2, 0x0017 = PWMPER3
Module Base + 0x0018 = PWMPER4, 0x0019 = PWMPER5, 0x001A = PWMPER6, 0x001B = PWMPER7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 22-13. PWM Channel Period Registers (PWMPERx)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime

22.3.2.12 PWM Channel Duty Registers (PWMDTYx)

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state.

The duty registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 22.4.2.5, “Left Aligned Outputs” and Section 22.4.2.6, “Center Aligned Outputs” for more details).

Table 22-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

22.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 22-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 22-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 22.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

Appendix B
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

B.1 VREG Electrical Specifications

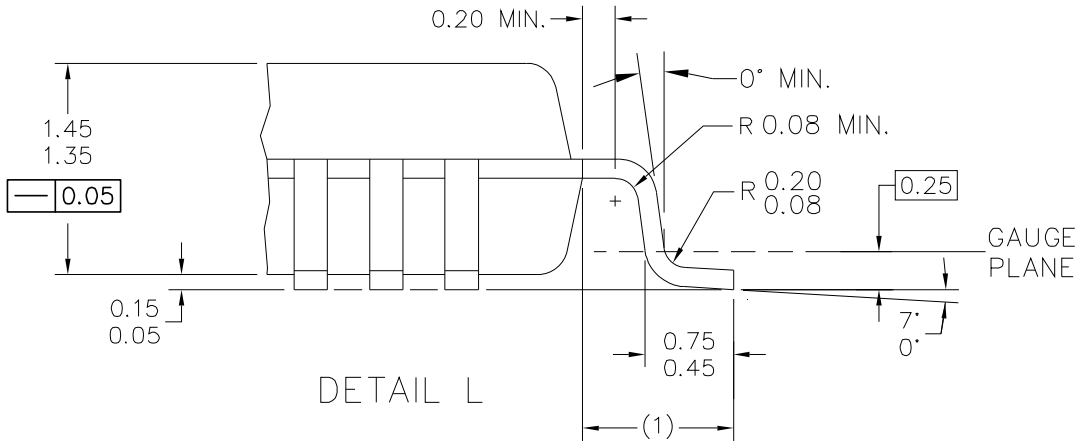
Table B-1. Voltage Regulator Electrical Characteristics
(Junction Temperature From –40°C To +175°C unless otherwise stated)

Note: VDDA and VDDX must be shorted on the application board.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1		Input Voltages	V_{SUP}	3.5	—	40	V
2		Output Voltage Core Full Performance Mode Reduced Power Mode (stop mode)	V_{DD}	 1.72 —	 1.84 1.6	 1.98 —	 V V
3		Output Voltage Flash Full Performance Mode Reduced Power Mode (stop mode)	V_{DDF}	 2.6 —	 2.82 1.6	 2.9 —	 V V
4a		Output Voltage VDDX (with external PNP, ZVMC256) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.90 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.10 5.10 5.10 5.75	 V V V V
4b		Output Voltage VDDX (with external PNP, other parts) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.85 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.15 5.15 5.15 5.75	 V V V V
4c		Output Voltage VDDX (without external PNP)[1] Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.80 4.50 3.13 2.5	 4.95 4.95 — 5.5	 5.10 5.10 5.10 5.75	 V V V V
4d		VDDX dependence on temperature and VSUP input V_{SUP} > 6V. No external PNP.	V_{DDX}	—	50	80	mV
5a		Load Current VDDX[2][3] without external PNP Full Performance Mode, V_{SUP} > 6V, -40°C < T_J < 150°C	I_{DDX}	0	—	70	mA
5b		Load Current VDDX[2][3] without external PNP Full Performance Mode V_{SUP} > 6V Full Performance Mode 3.5V <= V_{SUP} <=6V Reduced Performance Mode (stop) V_{SUP} > =3.5V	I_{DDX}	 0 0 0	 — — —	 55 20 5	 mA mA mA

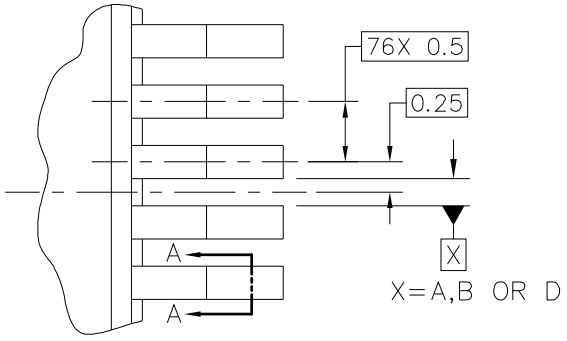
freescale

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING



DETAIL L



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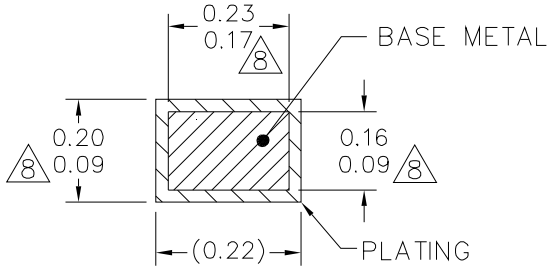

SECTION A–A
100 PLACES
ROTATED 90° CLOCKWISE

TITLE: LQFP, 12 X 12 X 1.4 PKG, 0.5 PITCH, 80LD, 5.6 X 5.6 EXPOSED PAD	DOCUMENT NO: 98ASA00505D	REV: X2
	STANDARD: NON–JEDEC	
	SHEET:	2