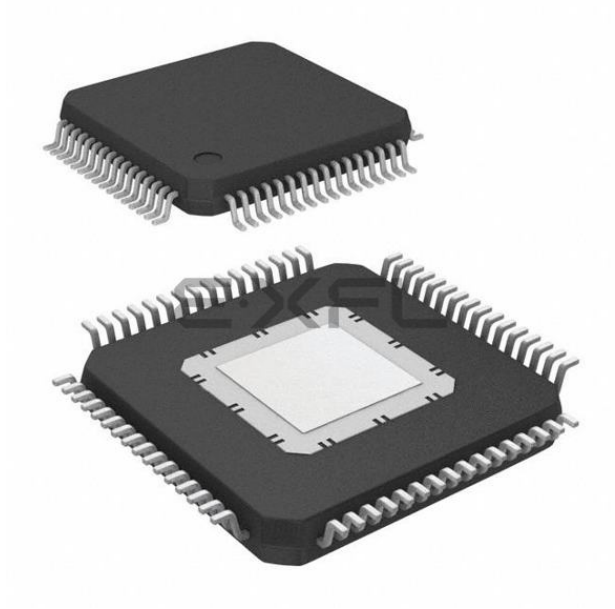

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Product Status	Obsolete
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Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc12f2mkh

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Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x00001D	INT_CFDATA5	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001E	INT_CFDATA6	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

= Unimplemented or Reserved

Figure 4-2. INT Register Summary

4.3.2.1 Interrupt Vector Base Register (IVBR)

Address: 0x000010

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IVB_ADDR[15:1]															0
W																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Figure 4-3. Interrupt Vector Base Register (IVBR)

Read: Anytime

Write: Anytime

Table 4-4. IVBR Field Descriptions

Field	Description
15–1 IVB_ADDR [15:1]	**Interrupt Vector Base Address Bits** — These bits represent the upper 15 bits of all vector addresses. Out of reset these bits are set to 0xFFFE (i.e., vectors are located at 0xFFFE00–0xFFFFFF). **Note:** A system reset will initialize the interrupt vector base register with “0xFFFE” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the reset vector (0xFFFFFC–0xFFFFFF).

4.3.2.2 Interrupt Request Configuration Address Register (INT_CFADDR)

Address: 0x000017

	7	6	5	4	3	2	1	0
R	0	INT_CFADDR[6:3]				0	0	0
W								
Reset	0	0	0	0	1	0	0	0

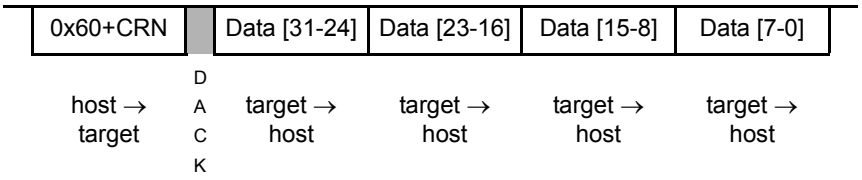
= Unimplemented or Reserved

Figure 4-4. Interrupt Configuration Address Register (INT_CFADDR)

Read: Anytime

5.4.4.10 READ_Rn

Read CPU register **Active Background**



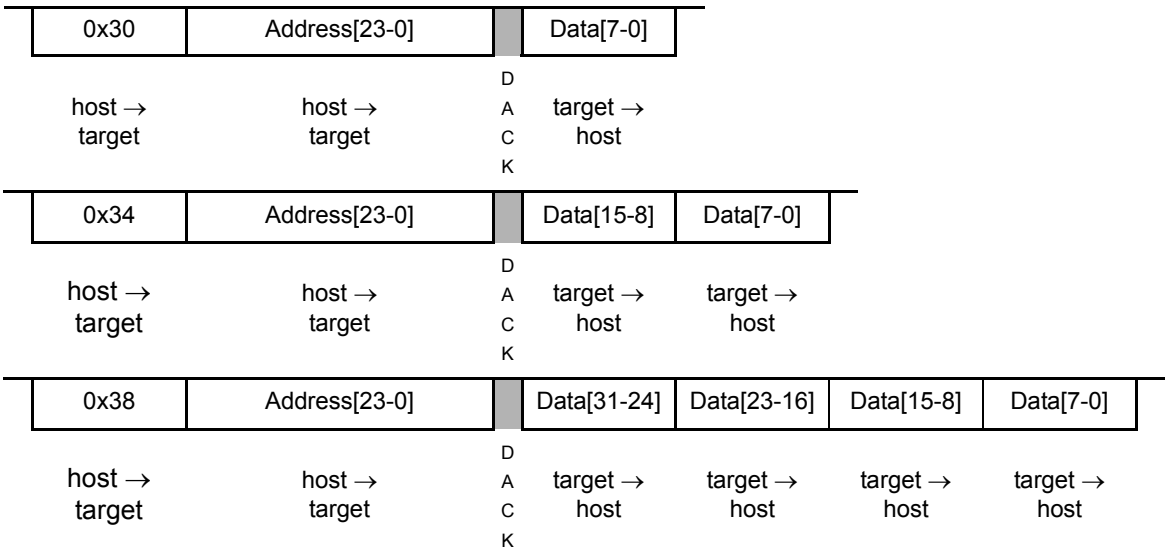
This command reads the selected CPU registers and returns the 32-bit result. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. Bytes that are not implemented return zero. The register is addressed through the CPU register number (CRN). See Section 5.4.5.1 for the CRN address decoding. If enabled, an ACK pulse is driven before the data bytes are transmitted.

If the device is not in active BDM, this command is illegal, the ILLCMD bit is set and no access is performed.

5.4.4.11 READ_MEM.sz, READ_MEM.sz_WS

READ_MEM.sz

Read memory at the specified address **Non-intrusive**



6.4.3.1.2 Data Access Comparator Match

Data access matches are generated when an access occurs at the address contained in the comparator address register. The match can be qualified by the access data and by the access type (read/write). The breakpoint occurs a maximum of 2 instructions after the access in the CPU flow. Note, if a COF occurs between access and breakpoint, the opcode address of the breakpoint can be elsewhere in the memory map.

Opcode fetches are not classed as data accesses. Thus data access matches are not possible on opcode fetches.

6.4.3.2 External Event

The DBGEEV input signal can force a state sequencer transition, independent of internal comparator matches. The DBGEEV is an input signal mapped directly to a device pin and configured by the EEVE field in DBGC1. The external events can change the state sequencer state, or force a trace buffer entry, or gate trace buffer entries.

If configured to change the state sequencer state, then the external match is mapped to DBGSCRx bits C3SC[1:0]. In this configuration, internal comparator channel3 is de-coupled from the state sequencer but can still be used for timestamps. The DBGEFR bit EEVF is set when an external event occurs.

6.4.3.3 Setting The TRIG Bit

Independent of comparator matches it is possible to initiate a tracing session and/or breakpoint by writing the TRIG bit in DBGC1 to a logic “1”. This forces the state sequencer into the Final State. If configured for End aligned tracing or for no tracing, the transition to Final State is followed immediately by a transition to State0. If configured for Begin- or Mid Aligned tracing, the state sequencer remains in Final State until tracing is complete, then it transitions to State0.

Breakpoints, if enabled, are issued on the transition to State0.

6.4.3.4 Profiling Trace Buffer Overflow Event

During code profiling a trace buffer overflow forces the state sequencer into the disarmed State0 and, if breakpoints are enabled, issues a breakpoint request to the CPU.

6.4.3.5 Event Priorities

If simultaneous events occur, the priority is resolved according to Table 6-46. Lower priority events are suppressed. It is thus possible to miss a lower priority event if it occurs simultaneously with an event of a higher priority. The event priorities dictate that in the case of simultaneous matches, the match on the higher comparator channel number (3,2,1,0) has priority.

If a write access to DBGC1 with the ARM bit position set occurs simultaneously to a hardware disarm from an internal event, then the ARM bit is cleared due to the hardware disarm.

Table 6-46. Event Priorities

Priority	Source	Action
Highest	TB Overflow	Immediate force to state 0, generate breakpoint and terminate tracing

8.3.2.10 S12CPMU_UHV_V10_V6 PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 8-15. S12CPMU_UHV_V10_V6 PLL Control Register (CPMUPLL)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

NOTE

Care should be taken to ensure that the bus frequency does not exceed the specified maximum when frequency modulation is enabled.

Table 8-9. CPMUPLL Field Descriptions

Field	Description
5, 4 FM1, FM0	PLL **Frequency Modulation Enable Bits** — FM1 and FM0 enable frequency modulation on the VCOCLK. This is to reduce noise emission. The modulation frequency is f_{ref} divided by 16. See Table 8-10 for coding.

Table 8-10. FM Amplitude selection

FM1	FM0	FM Amplitude / f_{VCO} Variation
0	0	FM off
0	1	±1%
1	0	±2%
1	1	±4%

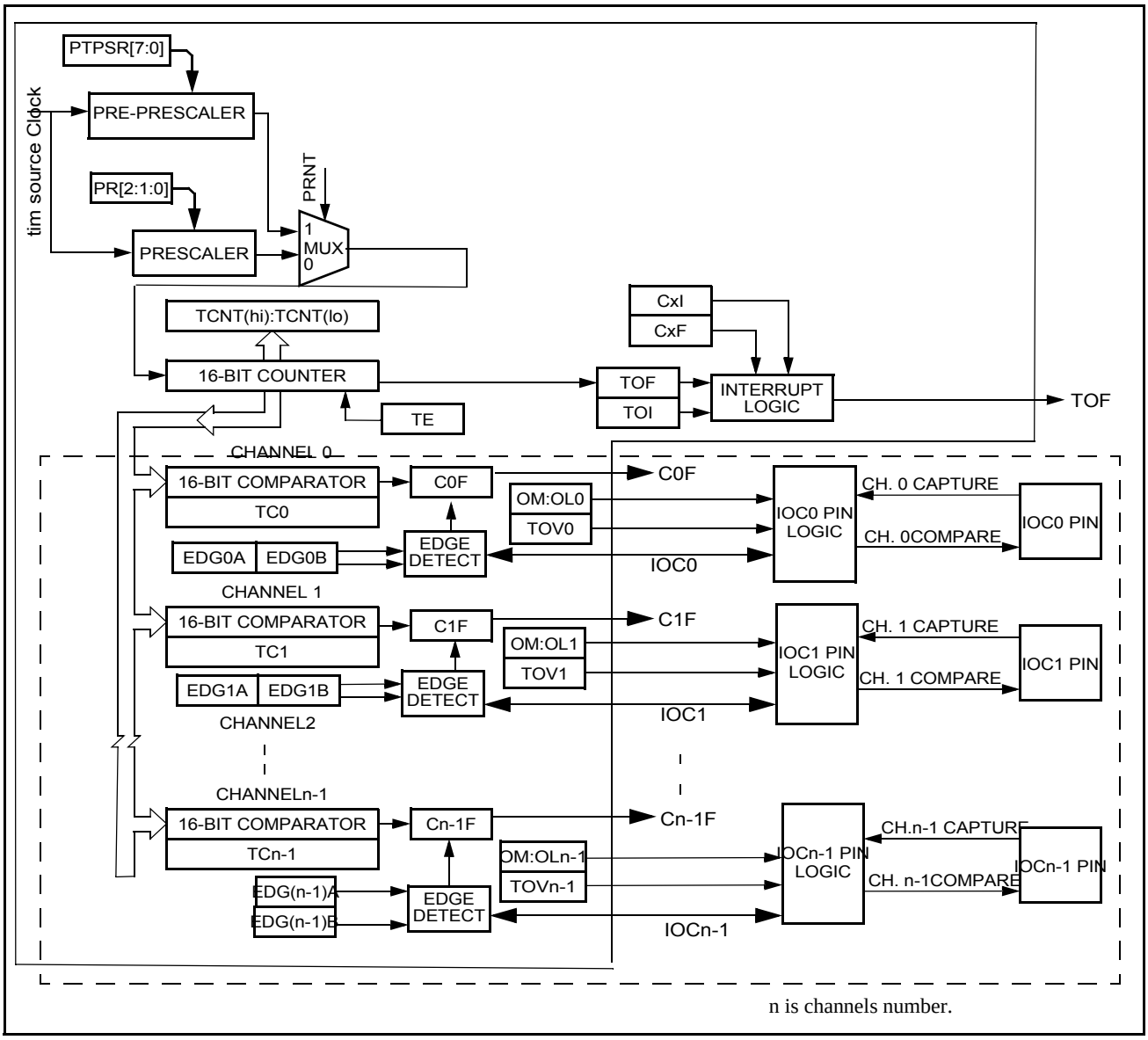


Figure 11-22. Detailed Timer Block Diagram

11.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000C TIE	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
	W								
0x000E TFLG1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL[1]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 12-3. TIM16B2CV3 Register Summary (Sheet 2 of 2)

1. The register is available only if corresponding channel exists.

12.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 12-4. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000E CANRXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
	W								
0x000F CANTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
	W								
0x0010–0x0013 CANIDAR0–3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x0014–0x0017 CANIDMRx	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0018–0x001B CANIDAR4–7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x001C–0x001F CANIDMR4–7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0020–0x002F CANRXFG	R	See Section 13.3.3, “Programmer’s Model of Message Storage”							
	W								
0x0030–0x003F CANTXFG	R	See Section 13.3.3, “Programmer’s Model of Message Storage”							
	W								

= Unimplemented or Reserved

Figure 13-3. MSCAN Register Summary (continued)

13.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.

13.3.2.1 MSCAN Control Register 0 (CANCTL0)

The CANCTL0 register provides various control bits of the MSCAN module as described below.

14.3.2.3 PTU Interrupt Enable Register High (PTUIEH)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTUROIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-5. PTU Interrupt Enable Register High (PTUIEH)

1. Read: Anytime
   Write: Anytime

Table 14-5. PTUIEH Register Field Descriptions

Field	Description
0 PTUROIE	PTU Reload Overrun Interrupt Enable — Enables PTU reload overrun interrupt. 0 No interrupt will be requested whenever PTUROIF is set 1 Interrupt will be requested whenever PTUROIF is set

14.3.2.4 PTU Interrupt Enable Register Low (PTUIEL)

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TG1AEIE	TG1REIE	TG1TEIE	TG1DIE	TG0AEIE	TG0REIE	TG0TEIE	TG0DIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-6. PTU Interrupt Enable Register Low (PTUIEL)

1. Read: Anytime
   Write: Anytime

Table 14-6. PTUIEL Register Field Descriptions

Field	Description
7 TG1AEIE	Trigger Generator 1 Memory Access Error Interrupt Enable — Enables trigger generator memory access error interrupt. 0 No interrupt will be requested whenever TG1AEIF is set 1 Interrupt will be requested whenever TG1AEIF is set
6 TG1REIE	Trigger Generator 1 Reload Error Interrupt Enable — Enables trigger generator reload error interrupt. 0 No interrupt will be requested whenever TG1REIF is set 1 Interrupt will be requested whenever TG1REIF is set

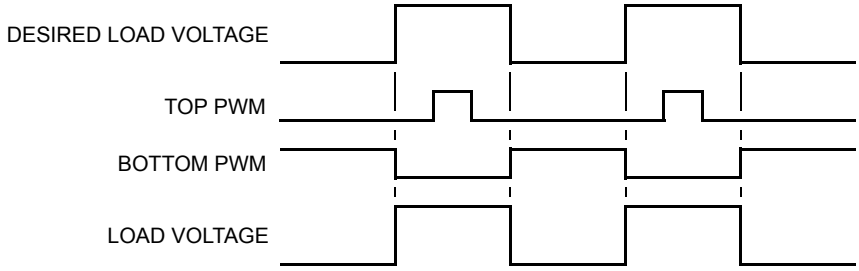


Figure 15-61. Correction with Negative Current

15.4.7 Asymmetric PWM Output

In complementary center-aligned mode, the PWM duty cycle is able to change alternatively at every half cycle. The count direction of the PWM counter selects either the odd or the even PWM value registers to use in the PWM cycle. For counting up, select even PWM value registers to use in the PWM cycle. For counting down, select odd PWM value registers to use in the PWM cycle. The related CINV*n* bits of the PWM pair must select the same polarity for both generators.

Table 15-44. Top/Bottom Corrections Selected by ICC*n* Bits

Bit	Logic State	Output Control
ICCA	0	IPOLA Controls PWM0/PWM1 Pair
	1	PWM Count Direction Controls PWM0/PWM1 Pair
ICCB	0	IPOLB Controls PWM2/PWM3 Pair
	1	PWM Count Direction Controls PWM2/PWM3 Pair
ICCC	0	IPOLC Controls PWM4/PWM5 Pair
	1	PWM Count Direction Controls PWM4/PWM5 Pair

NOTE

If an ICC*x* bit in the PMFICCTL register changes during a PWM period, the new value does not take effect until the next PWM period. ICC*x* bits take effect at the end of each PWM cycle regardless of the state of the related LDOK*x* bit or global load OK.

16.3.2.3 SCI Alternative Status Register 1 (SCIASR1)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-6. SCI Alternative Status Register 1 (SCIASR1)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 16-5. SCIASR1 Field Descriptions

Field	Description
7 RXEDGIF	**Receive Input Active Edge Interrupt Flag** — RXEDGIF is asserted, if an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD input occurs. RXEDGIF bit is cleared by writing a “1” to it. 0 No active receive on the receive input has occurred 1 An active edge on the receive input has occurred
2 BERRV	**Bit Error Value** — BERRV reflects the state of the RXD input when the bit error detect circuitry is enabled and a mismatch to the expected value happened. The value is only meaningful, if BERRIF = 1. 0 A low input was sampled, when a high was expected 1 A high input reassembled, when a low was expected
1 BERRIF	**Bit Error Interrupt Flag** — BERRIF is asserted, when the bit error detect circuitry is enabled and if the value sampled at the RXD input does not match the transmitted value. If the BERRIE interrupt enable bit is set an interrupt will be generated. The BERRIF bit is cleared by writing a “1” to it. 0 No mismatch detected 1 A mismatch has occurred
0 BKDIF	**Break Detect Interrupt Flag** — BKDIF is asserted, if the break detect circuitry is enabled and a break signal is received. If the BKDIE interrupt enable bit is set an interrupt will be generated. The BKDIF bit is cleared by writing a “1” to it. 0 No break signal was received 1 A break signal was received

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register.The transmit driver routine may respond to this flag by writing another byte to the Transmitter buffer (SCIDRH/SCIDRL), while the shift register is still shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
   a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is zero. Writing to the SCIBDH has no effect without also writing to SCIBDL.
   b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS,RSRC,M,WAKE,ILT,PE,PT).
   c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE,TCIE,RIE,ILIE,TE,RE,RWU,SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit Procedure for each byte:
   a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to one.
   b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

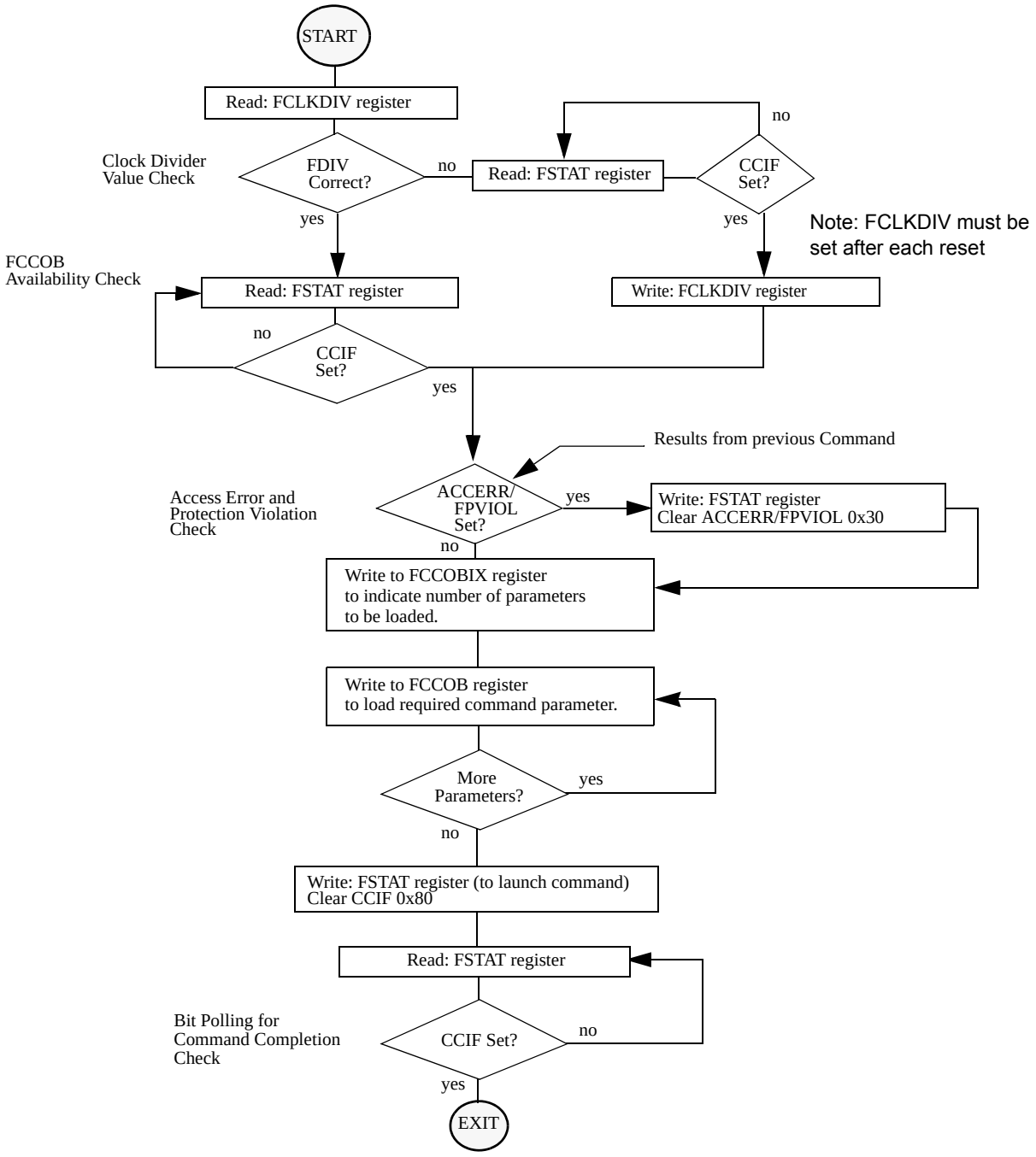


Figure 20-30. Generic Flash Command Write Sequence Flowchart

22.4 Functional Description

22.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of four clocks, clock A, Clock B, clock SA or clock SB.

The block diagram in Figure 22-15 shows the four different clocks and how the scaled clocks are created.

22.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode (freeze mode signal active) the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all available PWM channels are disabled (PWMEx-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

22.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

Appendix A
MCU Electrical Specifications

A.1 General

This section contains the most accurate electrical information available at the time of publication.

A.1.1 Parameter Classification

The electrical parameters shown in the appendices are guaranteed by various methods.

The parameter classification is documented in the PPAP.

The parameter classification columns are for NXP internal use only.

Table A-4. ESD Protection and Latch-up Characteristics

5		Latch-up Current of 5V GPIOs at T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
6		Latch-up Current (VCP, BST, LIN, HD, HS, HG, LG, LS, LD) T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
7		Latch-up Current of 5V GPIOs at 27°C positive negative	I_{LAT}	 +200 -200	-	mA
8		Latch-up Current (VCP, BST, LIN, HD, HS, HG, LG, LS, LD) T= 27°C positive negative	I_{LAT}	 +200 -200	-	mA

A.1.6 Recommended Capacitor Values

Table A-5. Recommended Capacitor Values (nominal component values)

Num	Characteristic	Symbol	Typical	Unit
1	VDDX decoupling capacitor (1) (2)	$C_{VDDX1,2}$	100-220	nF
2	VDDA decoupling capacitor (1)	C_{VDDA}	100-220	nF
3	VDDX stability capacitor (3) (4)	C_{VDD5}	4.7-10	uF
4	VDDC stability capacitor	C_{VDDC}	4.7-10	uF
5	VDDS[2:1] stability capacitor	C_{VDDS}	4.7-10	uF
6	VLS decoupling capacitor (1) (5)	$C_{VLS0,1,2}$	100-220	nF
7	VLS stability capacitor (3) (6)	C_{VLS}	4.7-10	uF
8	VDD decoupling capacitor (1)	C_{VDD}	100-220	nF
9	VDDF decoupling capacitor (1)	C_{VDDF}	100-220	nF
10	LIN decoupling capacitor (1)	C_{LIN}	220	pF

1. X7R ceramic
2. One capacitor per VDDX pin
3. 4.7μF ceramic or 10μF tantalum
4. Can be placed anywhere on the 5V supply node (VDDA, VDDX)
5. One capacitor per each VLS[2:0] pin
6. Can be placed anywhere on the VLS node

A.1.7 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted these conditions apply to the following electrical parameters.

1. Outside of the given V_{HVI} range the error is significant. The ratio can be changed, if outside of the given range.

A.2.2 HV Physical Interface Characteristics

The HV Physical Interface specification is included in the LINPHY electrical section.

A.3 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.3.1 Measurement Conditions

Current is measured on VSUP. VDDX is connected to VDDA. It does not include the current to drive external loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC1M trimmed to 1MHz. For the junction temperature range from -40°C to +150°C the bus frequency is 50MHz. For the temperature range from +150°C to +175°C, the bus frequency is 40MHz. Table A-15, Table A-16 and Table A-17 show the configuration of the CPMU module and the peripherals for Run, Wait and Stop current measurement.

Table A-15. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, CSAD=0, PRE=PCE=RTIOSCSEL=1 COPOSCSEL[1:0]=01
CPMUOSC	OSCE=1, Quartz oscillator f_{EXTAL}=4MHz
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-16. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]= 3,SYNDIV[5:0] = 49
CPMUPOSTDIV	POSTDIV[4:0]=0
CPMUCLKS	PLLSEL=1, CSAD=0
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
CPMUVREGCTL	EXTXON=0, INTXON=1

Appendix D
LIN/HV PHY Electrical Specifications

D.1 Static Electrical Characteristics

Table D-1. Static electrical characteristics of the LIN/HV PHY (Junction Temperature From -40°C To +175°C)

Characteristics noted under conditions 5.5V <= V_{LINSUP} <= 18V unless otherwise noted(1) (2) (3). Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.							
Num	**C**	Ratings	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		V_{LINSUP} range for LIN compliant electrical characteristics	V_{LINSUP_LIN}	5.5[1 2]	12	18	V
2		Current limitation into the LIN pin in dominant state(4) V_{LIN} = $V_{LINSUP\_LIN\_MAX}$	I_{LIN_LIM}	40	—	200	mA
3		Input leakage current in dominant state, driver off, internal pull-up on (V_{LIN} = 0V, V_{LINSUP} = 12V)	$I_{LIN\_PAS\_dom}$	-1	—	—	mA
4		Input leakage current in recessive state, driver off (5V<V_{LINSUP}<18V, 5V<V_{LIN}<18V, V_{LIN} => V_{LINSUP})	$I_{LIN\_PAS\_rec}$	—	—	20	µA
5		Input leakage current when ground disconnected (GND_{Device} = V_{LINSUP}, 0V<V_{LIN}<18V, V_{LINSUP} = 12V)	$I_{LIN\_NO\_GND}$	-1	—	1	mA
6		Input leakage current when battery disconnected (V_{LINSUP} = GND, 0<V_{LIN}<18V)	$I_{LIN\_NO\_BAT}$	—	—	30	µA
7		Receiver dominant state	V_{LINdom}	—	—	0.4	V_{LINSUP}
8		Receiver recessive state	V_{LINrec}	0.6	—	—	V_{LINSUP}
9		V_{LIN_CNT} =(V_{th_dom}+ V_{th_rec})/2	V_{LIN_CNT}	0.475	0.5	0.525	V_{LINSUP}
10		V_{HYS} = V_{th_rec} -V_{th_dom}	V_{HYS}	—	—	0.175	V_{LINSUP}
11		Maximum capacitance allowed on slave node	C_{slave}	—	220	250	pF
12a		Capacitance of LIN pin -40°C < T_J < 150°C, Recessive state	C_{int}	—	20	—	pF
12b		Capacitance of LIN pin -40°C < T_J < 150°C, Recessive state	C_{int}	—	—	45	pF
12c		Capacitance of LIN pin 150°C < T_J < 175°C, Recessive state	C_{int}	—	—	39	pF
13		Internal pull-up (slave)	R_{slave}	27	34	40	kΩ

1. For 3.5V<= V_{LINSUP} <5V, the LIN/HV PHY is still working but with degraded parametrics.

2. For 5V<= V_{LINSUP} <5.5V, characterization showed that all parameters generally stay within the indicated specification, except the duty cycles D2 and D4 which may increase and potentially go beyond their maximum limits for highly loaded buses.

3. The V_{LINSUP} voltage is provided by the VLINSUP supply. This supply mapping is described in device level documentation.

M.3 0x0070-0x00FF S12ZMMC

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0070	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0071-0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0080	MMCECH	R	ITR[3:0]				TGT[3:0]			
		W								
0x0081	MMCECL	R	ACC[3:0]				ERR[3:0]			
		W								
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0
		W								
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0
		W								
0x0084	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0085	MMCPCH	R	CPUPC[23:16]							
		W								
0x0086	MMCPCM	R	CPUPC[15:8]							
		W								
0x0087	MMCPCL	R	CPUPC[7:0]							
		W								
0x0088-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0100	DBGC1	R	ARM	0	reserved	BDMBP	BRKCPU	reserved	EEVE1	EEVE0[2]
		W		TRIG						
0x0101	DBGC2	R	0	0	0	0	CDCM[2]		ABCM	
		W								
0x0102	DBGTCRH[2]	R	reserved	TSOURCE	TRANGE		TRCMOD		TALIGN	
		W								

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F8–0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL[2]	R	0	0	0	0	0	0	0	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL[2]	R	0	0	0	0	0	0	0	PTPSL0
		W								
0x0334	PPSL[2]	R	0	0	0	0	0	0	0	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL[2]	R	0	0	0	0	0	0	0	PIEL0
		W								
0x0337	PIFL[2]	R	0	0	0	0	0	0	0	PIFL0
		W								